3-Dimensional Numerical Analysis of Deep Depletion Buried Channel MOSFETs and CCDs

Man-Ho Kim*

Abstract - The visual analysis of buried channel (BC) devices such as buried channel MOSFETs and CCDs (Charge Coupled Devices) is investigated to give better understanding and insight for their electrical behaviours using a 3-dimensional (3-D) numerical simulation. This paper clearly demonstrates the capability of the numerical simulation of "EVEREST" for characterising the analysis of a depletion mode MOSFET and BC CCD, which is a simulation software package of the semiconductor device. The inverse threshold and punch-through voltages obtained from the simulations showed an excellent agreement with those from the measurement involving errors of within approximately 1.8% and 6%, respectively, leading to the channel implanted doping profile of only approximately 4 ~ 5% error. For simulation of a buried channel CCD an advanced adaptive discretising technique was used to provide more accurate analysis for the potential barrier height between two channels and depletion depth of a deep depletion CCD, thereby reducing the CPU running time and computer storage requirements. The simulated result for the depletion depth also showed good agreement with the measurement. Thus, the results obtained from this simulation can be employed as the input data of a circuit simulator.

Keywords: Buried channel MOSFET, Charge coupled device, Semiconductor numerical simulation, Flat band voltage, Inversion threshold voltage, Deep depletion CCD, Depletion depth, potential maximum.

1. Introduction

Buried channel MOS structures have been used in applications including high-speed MOSFET circuits as a load device [1], buried channel CCDs [2,3] and SOS devices in CMOS technology [4]. However, it is much more difficult to understand its characteristics than the surface channel MOS structure, although the buried channel (BC) device has many applications because of the fewer interactions between the surface states and channel carriers, and the higher mobility.

Potential and charge distributions in the channel region play significant roles for predicting the operating modes of the device since the former characterizes the energy band-bending while the latter provides a measure of the current flow in the channel region and of the location of the neutral channel. It is necessary to analyze them for a fuller understanding of the characteristics of depletion-mode MOSFETs.

For BC MOSFETs, many analytical models have been developed for extracting the doping profile in the channel using a simple assumption of a 'top-hat' profile [5, 6], or a linear profile [7], or using a Gaussian-type doping profile [3] in the buried channel region. However they involve some over-simplifications such as an abrupt depletion approximation and a top-hat doping profile in the channel region. The analysis presented in Reference [3] showed that this is not valid for deep depletion devices with large values of R_p/σ where R_p is the projected range and σ is the straggle depth since this results in some errors in the determination of the junction depth despite the use of well-defined theoretical mathematical analysis [5, 6]. The use of such approximated models does not provide good approximation for deep implants. This means that for accurate analysis of deep depletion devices a further optimizing study needs to be carried out for the doping impurity approximation in the channel. Supporting this analysis, physical modelling should be considered and compared with actual measurements. For BC CCDs the result of the parameter extraction obtained from a BC MOSFET mounted on CCD sensing output circuitry is also valid for the analysis of the CCD if it is fabricated under the same process conditions. In our simulation the physical model and numerical algorithms were based on 3-D analysis [8]. In previous work [8-10], more detailed simulation results obtained

* School of Electronical Engineering, University of Ulsan, Korea. (jamesmhkim@mail.ulsan.ac.kr)
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from BC MOSFETs [8, 9] and CCDs [8, 10] have been shown to be good agreement with measurements.

Some important physical effects such as the narrow channel effects and the variation of potential minimum across the transverse direction due to the field implant dose of a p^+-channel stop region can be, thereby, predicted. Here, we will present a computer analysis of a 3-D simulation on deep depletion MOSFETs and CCDs together with a graphical representation for better analysis and insight in terms of the electrostatic potential and charge distributions in the channel region. The numerical simulation method in terms of physical models, used in this work, was presented in reference [8]. The solution of the device equations is carried out using the EVEREST 3-dimensional device modelling package [11], which combines geometric modelling, mesh generation, definition of doping profiles, problem solution and post-processing. EVEREST was developed for suitable algorithms for the analysis of semiconductor devices in three dimensions, and software implementing the most effective of the algorithms. After the simulations, an analytical model is required to derive a doping profile of the device using the inverse threshold and threshold voltages obtained from the simulation. The structure and operation of a BC MOSFET is described in Section II along with an analytical model from which the channel doping profile may be determined. In Section III, a deep depletion CCD to be used as an astronomic image sensor is considered to improve the charge detection efficiency with an accurate estimate of a radiation-sensitive volume in the device. Results from the numerical solutions and their comparisons with measured ones are discussed in Section IV. Conclusions are drawn in Section V.

2. Device Analysis

A depletion MOSFET usually includes a finite channel layer with an n-type doping density identical to that of the source and drain diffusion layer, which are implanted by phosphorus or arsenic into a p-type substrate material. To produce a normally-on type device, an n^+-polysilicon gate should be employed as this produces a surface depletion layer due to the work function difference between the poly-silicon gate and the channel region with no gate voltage. This work function difference controls the threshold voltage.

2.1 Device structure and operation

The device considered here was made for p-type silicon with a specified resistivity of 100 Ωcm (1.5E14 /cm^3) and a $<100>$ orientation. A buried channel layer which is overlying the p-type substrate was implanted by an n-type phosphorus doping at an energy of 120 KeV under annealing conditions of 30 minutes and temperature of 1100°C. Most phosphorus doses are deposited in silicon through the oxide thickness of 0.13 μm (in practice the oxide is a composite dielectric layer consisting of 85 nm of silicon oxide and of 85 nm of silicon nitride) resulting in a peak concentration at the silicon surface. The device has a channel length of 8 μm and a channel width of 64 μm with a sideways diffusion of 0.2 μm.

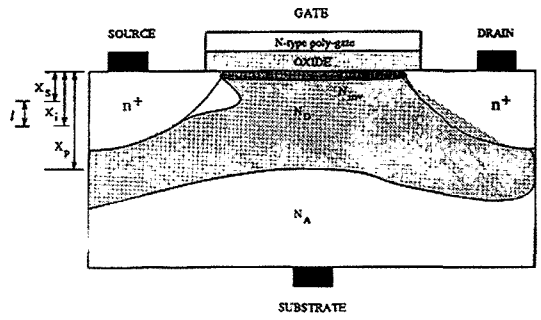


Fig. 1 A cross section of a typical BC MOSFET with a pinch-off mode.

The device, having a deep implanted doping profile, has a channel conductive layer with no external bias. Under different bias conditions it will operate in various modes such as enhancement, depletion, inversion and mixed modes [8] because of the varying channel potential.

Let us consider the operation of a buried channel MOSFET. First, under a constant drain-to-source voltage, V_{ds}, which is less than the gate-to-source voltage, V_{gs}, enhanced surface conduction will be formed due to the additional gate-induced electric field at the surface bringing an accumulation layer near the silicon surface. When the drain-to-source voltage is increased the current flow in the channel is then linearly increased. However, if the gate-to-source voltage is reduced below V_{ds} to avoid the mixed operation mode such as mixed accumulation/depletion mode, the device enters the entire depletion mode. When V_{gs} is further reduced to V_{ds}-V_{TH}, where V_{TH} is the threshold voltage, it will be finally operated under a pinch-off state. However, for deep depletion MOSFETs, with the sufficient reduction of the applied gate bias the surface region will be inverted due to free holes from the p^+-channel stops beneath the field oxide.

The device operation mode we desire is the channel pinch-off mode with a surface inversion layer as shown in Fig. 1 In Fig. 1, the surface depletion edge, x_s, meets up with the n-region depletion edge, x_n, of a channel-substrate

junction resulting in the absence of a channel conductive layer. The inversion layer can be controlled by considering the implant depth, dose and oxide thickness under proper operation voltage conditions since the channel punch-through and inverse threshold point are largely determined by them. In deep depletion MOSFETs there are two ways that channel punch-through may occur before the surface region is inverted: one is achieved by varying the source-to-substrate bias, V_{SS}, the other with a voltage difference between source and drain terminals [12]. The methods have the same effect against the inverse threshold point in that the formation of the surface inversion layer is delayed as much as V_{SS} or V_{ds} applied respectively which reduces the surface potential. In our analysis a substrate bias is used to control the surface inversion region and the depletion width in the channel since it is easy to control the channel and depletion width modulation and it also provides less limitation for CCD operation voltage conditions [13].

2.2 Flat band voltage

The device is operated as a normally-on or depletion BC MOSFET when an n^+-type poly-silicon gate is employed. The surface potential is then varied by the work function difference, ϕ_{ms}, between the poly-silicon gate and the n-channel region resulting in a threshold voltage shift. To eliminate this variation of the electrical characteristics an external bias may be applied to the gate terminal and thereby a flat band condition can be achieved at the Si/SiO_2 surface interface. An additional factor that effects the threshold voltage shift is the charge due to the surface states.

In our analysis the operating mode of the device is, however, under inversion mode since it has a deeply implanted channel. The built-in voltage should be replaced by the potential formed at the inverted surface layer, φ_{inv}, since it would be excluded in flat band condition due to the formation of additional capacitance at the Si/SiO_2 surface interface when the surface is completely inverted. The total flat band voltage, V_{FBT} will be, therefore, defined as

$$\begin{aligned} V_{FBT} &= V_{FB} + \varphi_{inv} \\ &= \phi_m - (\chi + E_g/2q + \varphi_B) + (kT/q)\ln(N_A/N_D) \end{aligned} \quad (1)$$

where χ is the electron affinity, q elementary electron charge, φ_B potential difference between the Fermi level and intrinsic Fermi level, n_i intrinsic concentration and E_g bandgap energy.

2.3 Inverse threshold voltage

In addition to the flat band voltage representing the flat band condition identifying the accumulation and depletion modes, one of the most important parameters is a threshold voltage at which negligible mobile carriers flow in the channel. For the semiconductor devices, in general, two kinds of devices are available: normally-off and normally-on (or depletion mode) types. The former has usually no channel conductance under zero external bias at which the flat band condition is maintained while the latter includes a finite depletion thickness even when no bias is applied. So, for the depletion mode the applied bias equal or less than the pinch-off voltage will be required to turn it off.

Using an abrupt depletion approximation the threshold voltage can be derived :

$$\begin{aligned} V_{TH} = {} & V_{FB} + \varphi_{ch} - q\,x_i N_D\{1/(2\,C_i) + 1/(C_{ox})\} \\ & + (1/C_i + 1/C_{ox}) \times \{q\varepsilon_s N_{ib}(\varphi_{ch} - V_{ss})\}^{1/2} \\ & - \{(N_{ib}/N_D)(\varphi_{ch} - V_{ss})\} \end{aligned} \quad (2)$$

with $N_{ib} = N_A N_D / N_A + N_D$, $C_i = \varepsilon_s / x_i$, $C_{ox} = \varepsilon_{ox} / x_{ox}$ and $\varphi_{ch} = V(y) + V_{bi}$

where V(y) is the channel potential at a point along the channel, V_{bi} is the built-in potential, and x_i and x_{ox} are the implant depth and oxide thickness, respectively. In practice, φ_{ch} becomes V_{bi} since V(y) is negligible, in the procedure of the parameter extraction, but in our case it will be considered to obtain more accurate analysis.

The channel pinch-off cannot be achieved even with a sufficiently lower gate bias resulting in a restricted quasi-saturation current level since the surface region is inverted before the channel reaches the pinch-off state. This means that the depletion width is out of control due to the formation of the inversion layer at the surface with the applied gate bias. There exists, thus, two different threshold voltages in the device with the deep implant and/or heavy dose: threshold and inverse threshold voltages. Therefore, the substrate bias should be added to give some controllability from the gate-induced electric field perpendicular to the surface. This is possible because the gate voltage is referenced to the substrate bias [13]. Then, the channel width will be further depleted resulting in the variation of the surface potential and potential drop across the oxide thickness and thereby the inverted layer finally disappears. In this manner, the punch-through state can be attained using appropriate bias conditions between gate and substrate terminals. The effect of the substrate bias on the cancellation of the channel region is the same as that of the applied drain bias. When the surface potential is less than the substrate potential the surface region is always inverted by free holes from the p^+-channel, which stops below the field oxide connected to the substrate bias, still resulting in

a significant channel conduction, since the inversion layer is connected to the substrate. The number of the minority carrier concentration in the inversion layer is, then, equal to the channel doping of the implant. For further reduction of the substrate bias the surface depletion edge, x_S, meets together with the n-side depletion edge of the metallurgical junction. In this situation the gate voltage applied becomes an inverse threshold voltage and the BC MOS transistor is finally turned-off resulting in negligible conduction current in the channel.

When a strong inversion layer is formed at the surface, the surface potential, φ_S, is written by

$$\varphi_s(inv) = V_{ss}(inv) + \varphi_{inv} \tag{3}$$

Where $$\varphi_{inv} = kT/q \ln(N_A/N_D) \tag{4}$$

Using kirchhoff's voltage law, the inverse threshold voltage may be expressed as [8]

$$\begin{aligned} V_{Ti} - V_{FB} &= V_{ox}(inv) + \varphi_s(inv) \\ &= -2/C_{ox} \{\delta(\varphi_{ch} + |V_{ss}(inv) + \varphi_{inv}|)\}^{1/2} \\ &\quad + \varphi_{inv} + V_{ss}(inv) \end{aligned} \tag{5}$$

where $\delta = q\varepsilon_s N_D$ and $V_{OX}(inv)$ is the voltage drop across the oxide layer and equal to Q_{sm}/C_{OX} where Q_{sm} is the surface depletion charge density under an inversion mode and is represented by

$$Q_{sm} = 2\{\delta(\varphi_{ch} + |V_{ss(inv)} + \varphi_{inv}|)\}^{1/2} \tag{6}$$

2.4 Channel profile approximation

The main purpose of using an analytical model of the device is to give an accurate consideration of the distributions of its electrostatic potential and charge carrier. They are usually determined by the average doping concentration in the channel, N_D and its depth, x_j, whose product represents an actual implant dose. So, in this analysis the channel and substrate concentrations occupied in the device are assumed to be step profiles. In this manner we have derived simple analytical expressions that provide a high accuracy for determining the average charge concentration and its depth [8]. To measure an inverse threshold voltage, drain voltage applied (which is always referenced to source) is close to zero. A drain-to-source voltage of about 50 mV was used in our measurement and simulation to clearly see the effect of the gate bias on variations at the surface as a function of the substrate bias. The average channel doping concentration, surface depletion width, actual implant dose in the channel and implanted channel depth may be expressed by [8]

$$N_D = -SL^2 C_{ox}^2/(2q\varepsilon_s) \tag{7}$$

$$x_s = (V_{g\min}(PT) - V_{FBT}) C_{ox}/(qN_D) \tag{8}$$

$$\begin{aligned} N_{imp} &= (V_{g\min}(PT) - V_{FBT}) \\ &C_{ox}/q + \{2\varepsilon_s N_{ib}/(qN_D)(\varphi_{ch} + |\varphi_{inv} + V_{ss}|)\}^{1/2} \end{aligned} \tag{9}$$

$$x_i = N_{imp}/N_D \tag{10}$$

where $V_{gmin}(PT)$ is equal to the potential across the oxide layer under a punch-through state and SL is the slope ot the regression curve, which determines the average channel doping concentration.

3. Application of BC CCD: JET-X CCD

For buried channel CCDs as solid-state imagers the most important characteristics are charge handling capability and charge transfer efficiency. The former is largely determined by the implant process parameters and gate clock voltage ranges since it decreases with decreasing channel depth thereby increasing the effective channel doping concentration. The profile of the implant and its dose may be optimized for a maximum charge handling capacity as a function of the substrate doping concentration and gate clock voltage. Their optimization may be achieved by considering the two conflicting factors mentioned above and thereby defining an optimized potential depth of the storage well under the absence and presence of the signal charge.

The latter is a measure of charge loss from the signal charge packet in the charge transfer process. It is dominated by three main factors: thermal diffusion, self-induced drift and fringing field effects. For small charge packets the transfer process will be dominated by thermal diffusion and fringing field, while a self-induced electric field will be significant for large charge packets. To transfer the whole signal from one storage well to the next without surface charge trapping at a given charge transfer time, the potential difference between the surface interface and channel minimum point should be greater than 10 kT/q [14].

For efficient charge collection the leakage current caused by the thermal generation of impurities in the Si crystal should be kept as low as possible, since it produces the detector noise when biasing is applied for charge collection

If a large contribution from the leakage is added in the charge pulse, the CCD will lose its function. Another important factor for a higher charge collection is a large sensitive collection volume or depletion layer. The large depletion layer also provides a small CCD capacitance and thus lower output noise. Increasing the depletion layer is possible by raising the applied reverse bias, but due to the occurrence of the breakdown phenomena the depletion layer is limited. Therefore, the two problems mentioned above, such as leakage current and limitation of the depletion layer due to low breakdown voltage can be largely eliminated by using a high resistivity bulk material.

For energy photons with long absorption length (i.e. wavelengths less than 1 nm or greater than 600 nm), the Q.E. depends largely on the thickness of the photosensitive volume. Intermediate wavelengths have relatively short absorption lengths in silicon and silicon dioxide, and throughout this spectral region the Q.E. depends largely on the transparency, reflectance and surface conditions of the surface layers that overlie the photosensitive volume.

Thus, the improvement of Q.E. is achieved by using a thicker device with high-purity bulk material for high X-ray energy and with thinner gate electrodes for low X-ray energy. Such a CCD electrode structure for astronomic application is shown in Fig. 2 The purpose of using the struc ture is to improve high spatial resolution, achieving good spectral resolution and efficient rejection of background charged particle signals for a spectral band of 0.1~10 KeV. This structure has a depletion depth of 38 μm and a field-free region of 27 μm. In this structure the image section consists of two channel regions with different implant doses of 3.0×10^{11} and 5.5×10^{11} ion/cm^2 respectively, resulting in a potential barrier between two channels.

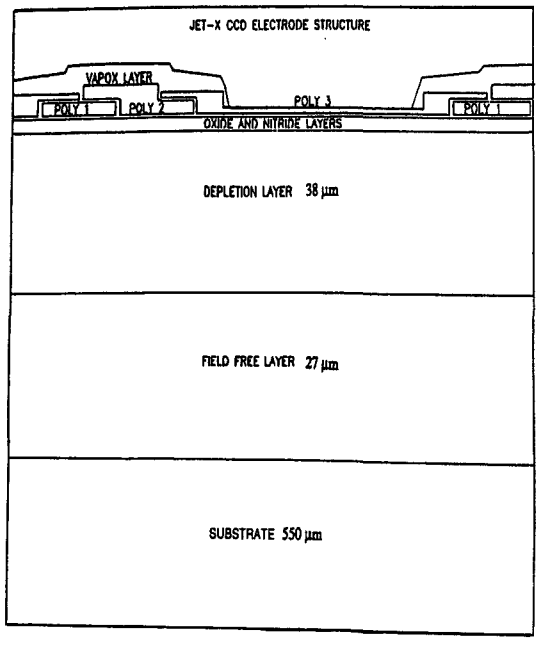


Fig. 2 A schematic of a deep depletion CCD structure.

In order to accurately estimate the potential maximum, potential barrier, and depletion depth in a deep depletion CCD a numerical simulation was performed. So far, their approximations have been obtained by a 1-dimensional model [8] based on an assumption of an abrupt depletion edge. In practice the depletion edge is determined at a point where the electric field becomes zero through several Derby lengths. Thus, such a depletion approximation results in its underestimation.

The depletion width of a CCD can be controlled by the floating diode voltage, gate clock voltage and substrate voltage. The maximum voltage of the floating diode strongly depends upon the channel doping level. The diode voltage determines the channel maximum potential as a function of the implant doping in the channel, in the same manner as the effect of a drain voltage on the channel potential in BC MOSFET. The depletion edge becomes deeper as the diode voltage increases. When the diode voltage reaches a maximum value the p-region depletion edge of the p-n junction will be constant to be maximum. In this situation the application of gate voltage gives a further increase of the depletion edge by extending a surface depletion width. However, further increase of gate voltage makes the location of the potential minimum close to the surface interface resulting in a higher probability of channel charge interaction with the surface states. After a maximum depletion width is obtained by the two voltage applications mentioned above, a substrate bias is applied to achieve a further increase in width. The effect of the substrate bias on the depletion width is almost the same as that of the gate bias, since the gate voltage is referenced to the substrate. So, a final maximum depletion width can be achieved by decreasing the substrate bias, which effectively makes

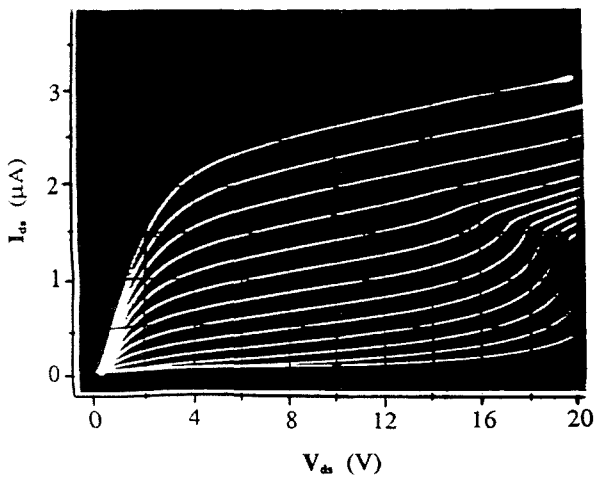


Fig. 3 I-V Charateristic curves of a buried channel MOSFET.

the gate voltage increase. The results obtained from the simulation will be discussed in the next section.

4. Results and Discussion

During this work, many different device simulations have been performed to demonstrate an analysis technique for a deep depletion BC MOSFET and BC CCD. A transistor curve tracer can be used to produce sets of operational characteristic curves of MOSFETs. The I-V characteristic curves of a typical CCD MOS transistor fabricated by EEV Ltd. are shown in Fig. 3. These curves were obtained with a substrate bias of -10 V, varying gate-to-source voltages from 0 V to -12 V (in which a vertical scale of I_D=0.5μA/div and horizontal scale of V_{ds}=2V/div was given). It is shown from the curves that avalanche breakdown caused by an impact ionisation occurs at V_{ds}>18 V. The specifications of the process parameters used in simulation are shown in Table 1 for n-type BC MOSFETs. All the devices with similar process conditions result in the peak concentrations at the surface. They have been simulated to analyze the dependence of V_{Ti} and V_{TH} on implanted doping profile in the channel region. The device structure used in the simulation has a channel geometry in which y axis represents one-tenth of a channel width of 64 μm, which is an actual dimension of an EEV device, to reduce computer running time and memory capacity requirements. The narrow channel effect could be negligible since the channel potential difference between the simulation results with 6.4 and 64 μm showed about 0.11 V. Also, this was proved in Reference [16] where it was presented in detail.

Table 1 Device parameters values used in simulations of BC MOSFET

Parameters		Parameters	
Implant dose (cm^{-2})	9.4E11 to 1.27E12	workfunction voltage	0.92 V
Oxide thickness μm)	0.13	Substrate doping (cm^{-3})	1.5E14
Channel length (μm)	8	Fixed oxidecharge (cm^{-2})	1.0E11 ~ 1.4E11
Channel width (μm)	6.4	Sideways diffusion (μm)	0.2

From the potential and charge distributions produced from the simulation, with a sufficient mesh density in the channel region, the operating modes of the device could be described. The channel region is gradually eliminated as the gate voltage as a function of the substrate bias negatively increases before a punch-through state is reached. Fig. 4 illustrates the isometric potential and electron carrier distributions under the inversion mode and punch-through state, respectively. It can be clearly seen in Fig. 4(b) and 4(d) that punch-through state electron carriers in the channel region were completely depleted and the channel potential was negatively increased, whilst Fig. 4(a) and 4(c)

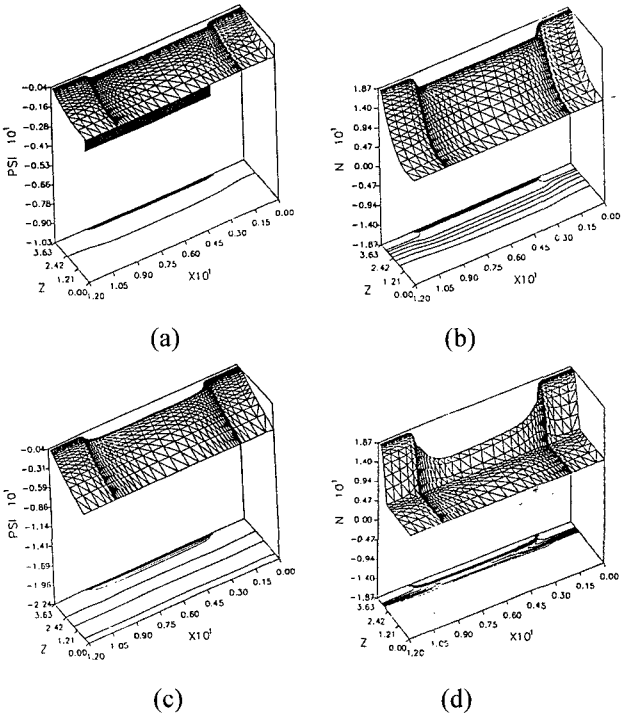


Fig. 4 Isometric potential and charge impurity distributions for case 2: (a) and (c) strong inversion state (with V_{gs}(inv) = - 4.35 and V_{ss} = 0 V), (b) and (d) punch-through state (with V_{gs}(PT) = -10.45 and V_{ss}(PT) = -2.8 V).

Table 2 A comparison of V_{Ti}s and V_{PT} simulated and measured

Vss	VTi(simulated)			VTi(measured)	Error(%)
	Case 1	Case 2	Case 3	Case 2	Case 2
0.0	4.14	4.43	4.69	4.3	3.0
0.4	5.20	5.54	5.86	5.45	1.6
1.0	6.56	6.97	7.34	6.8	2.5
1.4	7.36	7.82	8.24	7.65	2.2
1.8	8.11	8.61	9.07	8.45	1.9
2.2	8.77	9.36	9.86	9.2	1.7
2.3	V[PT]		10.05		
2.5		9.88	10.43	9.85	0.3
2.7		10.19	10.83	10.05	1.4
2.8		V[PT]			
3.0			11.31	10.8	
3.1			11.47	V[PT]	
3.3			V[PT]		

indicate the potential and electron distributions, respectively, under an inversion mode where the surface depletion depth is limited due to the inversion layer.

The gradual increase of gate voltage as a function of a substrate bias enabled the device to reach punch-through before resumption of the strong inversion mode. This gate controllability for the channel cancellation can be clearly described from Fig. 5. Under a sufficiently high operating voltage condition a potential minimum point can be determinedwhen the punch-through state is reached as represented at curve 6 of Fig. 5(a) and 5(b), respectively. In this situation, the drain current will be negligible due to no neutral channel region. In our analysis, a complete punch-through point was defined when drain current level was approximately 1.0E-8 A (the drain current was approximately 2.0E-7 A for simulation of a device with 64 μm). The results simulated by EVEREST demonstrated that deep depletion BC MOSFETs required higher V_{Ti} and V_{TH} as the implant dose increased. They are numerated in Table 2 for three different implant doping cases. For case 2, different V_{Ti}s and V_{TH} extracted from the simulation showed good agreement with those measured as shown in Table 2. In this comparison, it was clear that the simulated punch-through point was reached with lower operation voltages than those used in the measurement, leading to some errors in the determination of doping profile as seen in Table 3. However, for inverse threshold voltages they showed an excellent agreement with the measurement. All the parameter values extracted from respective device simulations and measurement data are summarized in Table 3, which are obtained using a 1-dimensional analytical model. In practice, the actual channel implant dose, N_{imp}(act), is calculated by deducting $N_A \cdot x_i$ from the implanted dose deposited in silicon, N_{imp}.

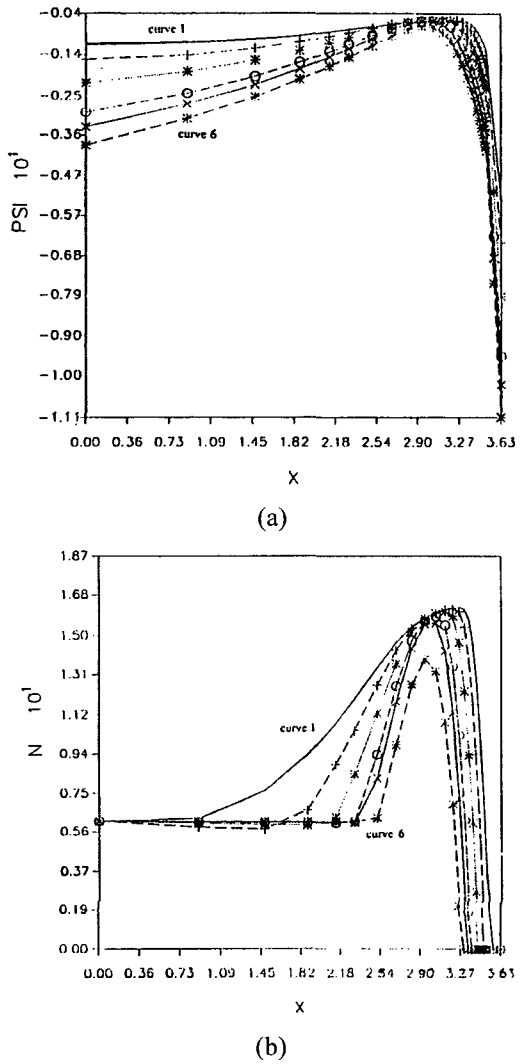
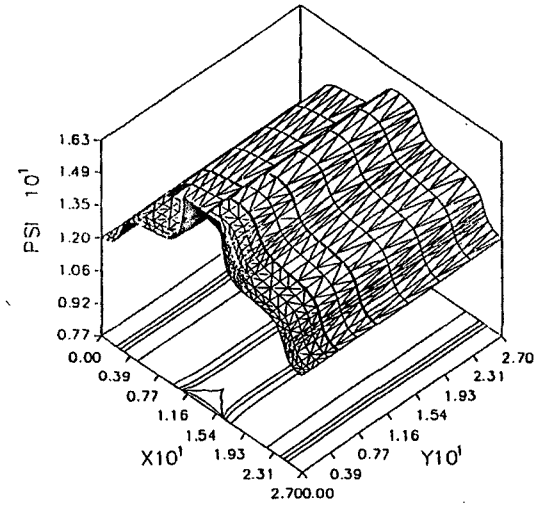


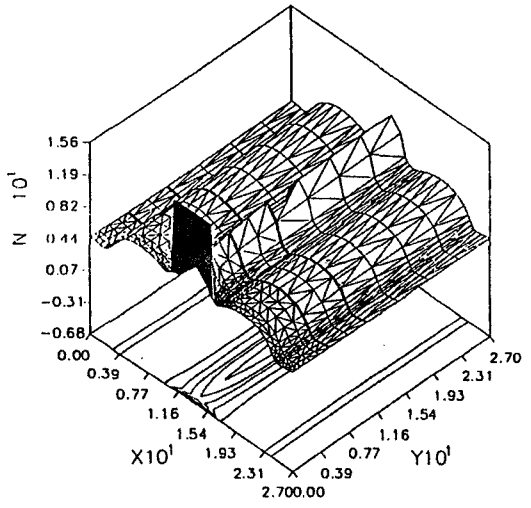
Fig. 5 Potential (a) and charge (b) distributions for case 2 with V_{SS} = -4.35, -5.5, 6.9, -8.55, -9.3, -10.2 V and V_{SS} = 0.0, -0.4, -1, -1.8, -2.2, -2.8 V for curves 1 to 6, respectively.

The simulated doping profile in the channel region, presented in Table 3, also agreed very well with those found based on the measurement data, although some errors in the determination of punch-through point were involved in the simulation. A significant improvement was possible when for more accurate analysis a drain-source voltage and surface potential across the inversion layer at the surface are considered in the extraction program for a plot of $(V_{Ti} - V_{ss})$ versus $(V_{bi} + |V_{ss}|)^{1/2}$. In practice such small factors have been ignored since their influence on the determination of the implant doping profile could be said to be negligible. Deep depletion device hole carrier concentration compensated at the surface usually exists due to the inversion layer resulting in slight decrease in the channel implant doping according to the charge neutrality of the whole system. This effect may be significant if the difference between the channel doping and substrate concentrations becomes very large. In doing so, an improvement of about 4% of predicting the implant profile was achieved [8]. It was shown from the result [8] that the differences between curve 1 ($V_{ds} = \varphi_{inv} = 0$) and curve 2 ($V_{ds} + \varphi_{inv} = 0.177$) for the slope and intercept was 0.14 and 0.4, respectively. Such variations have given rise to a higher underestimation of N_D and thus overestimation of x_i in our case.

To further investigate this effect a p-type BC MOSFET was simulated and its result is shown in case 4 of Table 3. An implant dose of 1.4E12 ion/cm^2 through an oxide thickness of 0.12 um was used to generate a p-type channel on a substrate material with a substrate concentration of



(a)



(b)

Fig. 6 The potential (a) and electron (b) distributions across the channel width of JET-X CCD.

8.5E14 cm^{-3}. The device parameters used in the simulation are detailed in reference [6]. The result obtained from the simulation showed quite good estimation for channel doping profile with the same number of nodes for mesh refinement. In this case a small improvement of 0.7% was achieved because the substrate concentration was higher than our device, thereby resulting in a lower inversion voltage. Its effect on the determination of doping profile was therefore negligible in this case. Our results demonstrated good agreement with the results obtained from reference [7].

During this work it was realized that for a 3-D numerical analysis of a deep depletion MOSFET with a p-n junction of approximately more than 1.0 μm the whole system volume under consideration could not be covered with the

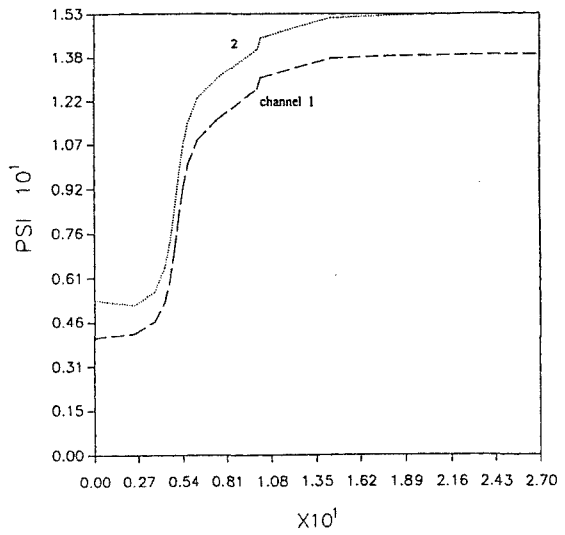


Fig. 7 The potential difference between two different channels in the image section.

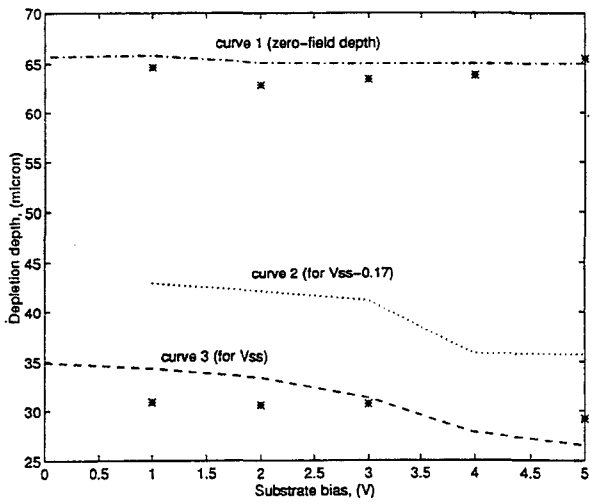


Fig. 8 Comparisons between the simulated (curves 1, 2 and 3) and estimated depletion depths [17].

number of nodes required for mesh refinement used in our simulation. This is because the p-n junction is placed too far away from the surface and a higher number of nodes is necessary. It means when the device approaches a punch-through mode much more numerical computations will be required for accurate numerical solution, since the totally depleted channel regions and extended p-side depletion edge of the p-n junction are formed, requiring an increase in ICCG iterations.

For efficient charge transfer process the potential barrier between two channels should be investigated, where channel 2 includes an additional doping at a higher level than the implant doping of channel 1. Under the punch-through state the potential and electron distributions on a potential maximum point can be seen in Fig. 6(a) and 6(b), respectively, where the floating diffusion, gate and

substrate voltages were 16, 12 and 3 V, respectively. In Fig. 6 the potential and electron distributions show three different levels which consist of channel 2 (highest doping level), channel 1 (medium doping level) and both end regions including no doping impurity (lowest), respectively. Fig. 7 illustrates the potential difference between channel 1 and channel 2. For further increase of the barrier the implant doping in channel 2 should be increased if the doping in channel 1 is fixed to be constant. The potential barrier is increased by 0.4 V when the doping of channel 2 becomes higher by 0.5×10^{11} cm^{-2}.

In order to estimate the depletion depth of a deep depletion CCD different operating voltage conditions such as a function of the substrate bias have been used in the simulation. In fact, it was very difficult to accurately estimate its depth using the potential and/or electric field distributions, since their variations were not clear when a different substrate bias was applied. So, we divided the depletion region into three different parts: intrinsic depletion, strong depletion and light depletion.

Table 3 Comparisons of doping profiles extracted from different simulations

Case	Mean dose (N_D) ($1\times10^{16}/cm^3$)	Imp. channel depth (x_i)/(um)	Actual implant dose (simu.) ($1\times10^{12}/cm^2$)	Actual implant dose (calcu.) ($1\times10^{12}/cm^2$)	$\frac{(N_{imp}(act)-N_D\cdot x_i)}{N_{imp}(act)}$(%)
1	1.79	0.50	0.893	0.93	4.1
2	2.10	0.495	1.04	1.09	4.6
3	2.42	0.496	1.20	1.264	5.0
4	2.63	0.513	1.349	1.353	3.0

For the intrinsic depletion region its depth may be clearly determined from the distribution of the hole carriers occupying the depletion region. Its depletion edge was found at a point where the hole carriers are significantly dropped to minimum level (from the substrate doping level) whilst the field density then decreases greatly toward the substrate. For the second depletion region the electric field does not fall down to zero and the potential approaches to the substrate bias applied at the depletion edge. In this part the electric field density at its depletion edge was approximately $2 \sim 4\times10^2$ V/cm, which amounts to about 2 ~ 4% of the maximum field density and is varied as a function of the substrate bias. In case of the third one the electric field becomes, finally, zero at the depletion edge. In this manner the depletion width has been classified. Fig. 8 shows the simulated depletion depths and their comparison with the measure-ment [17]. The measurement data demonstrates that the strong depletion edge increases with a decreasing substrate bias, while the location of the simulated edge was placed at 38 μm regardless of the substrate bias. For the intrinsic depth the effect of a higher substrate bias than 4 V on the depletion depth made our analysis difficult and the result is shown only for the substrate bias less than 3 V. In the simulation the light depletion width was about 38 μm when the substrate bias was applied to 2 V. There exists some difference between the simulated and measured data. This is probably because each depletion edge was strongly dependent on the distribution of the substrate concentration. In our simulation the substrate doping distribution was assumed to be uniform as 1×10^{13} at/cm^3 while the fabricated device includes a non-uniform substrate doping distribution. However, their comparisons showed good agreement. Finally, in order to accurately estimate the different depletion edges a non-uniform doping profile of the substrate must be added to the simulation.

5. Conclusions

Buried channel MOSFETs and CCDs with deep implants have been analyzed to estimate the actual doping profile in the channel, and the potential barrier and the depletion depth in the device, respectively. The EVEREST simulation showed a powerful potential for solving the deep depleted region and thus provided a good prediction for the electrical behaviour of the device. All the simulations performed in this work have been run on a SUN spark-workstation. Our simulation results indicated very good agreement with the measured inverse threshold and punch-through voltages as well as the doping profile determined by a one-dimensional theoretical model based on the measurement for BC MOSFETs.

For BC CCDs the depletion depth and the barrier height of a deep depletion CCD with a complicated doping distribution has been estimated using an advanced adaptive technique. From the simulated result for the depletion depth, it can be seen that a uniform substrate doping profile may result in some errors on the determination of the accurate depletion depth, since the simulated depletion depths were, as a rule, constant regardless of the substrate bias, especially, for the intrinsic and strong depletion edges. Therefore, it was evident that the EVEREST simulation package was a very useful tool for analysing the electrical behaviour of n- and p-type BC MOSFETs as well as BC CCDs.

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Man-Ho Kim

He received his Ir degree from Delft University of Technology in Holland (1986-1989) and his Ph.D from Leicester University in the UK (1992-1995). His research interests are the CCD/CMOS image sensor and Optical laser transmission system.

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