스펙트럼 감시를 위한 고속 탐색 디지털-IF FFT 수신기 설계 및 분석

A Design and Performance Analysis of the Fast Scan Digital-IF FFT Receiver for Spectrum Monitoring

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ABSTRACT

A fast scan digital-IF FFT receiver at the radio communication band is presented for spectrum monitoring applications. It is composed of three parts: RF front-end, fast LO board, and signal processing board. It has about 19GHz/s scan rate, multi frequency resolution from 10kHz to 2.5kHz, and high sensitivity of below -99dBm. The design and performance analysis of the digital-IF FFT receiver are presented.

주요기술용어(주제어) : Fast Fourier Transform(FFT), Digital Signal Processing(DSP), Analog-to-Digital(A/D), Spurious Free Dynamic Range(SFDR), Phase-Locked Loop(PLL), Direct Digital Synthesizer (DDS)

1. Introduction

In modern combat environment, electronic warfare(EW) receivers are used for obtaining all the information as monitoring any randomly directed signals. Hence, these receivers should have wide frequency range, high sensitivity and wide dynamic range, high probability of intercept, multiple simultaneous signal detection, fine frequency resolution, and real-time operation[1,2].

Earlier receivers are built using analog technology. These are channelized, compressive, and bragg cell receivers. They have reasonable performance to meet EW receiver requirements but have unreliable performance due to non-linear analog circuits. Moreover, these designs are also bulkier.

Many advances in radio design and architecture such as low cost digital signal processing(DSP) chips and high dynamic range analog-to-digital (A/D) converters have made possible the design of the high performance receivers. These advances allow for reduction of cost, size and complexity, and replace unreliable and inaccurate analog circuits with digital circuits[3,4]. These digital receivers provide improved performances such as

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the capability of multiple simultaneous signal processing with good frequency accuracy, high singe- and two-tone spurious free dynamic range(SFDR) for detecting a weak signal in the presence of an adjacent strong signal. The digital receiver is currently receiving considerable attention in the design of the compact, and high performance EW receivers because of the technical benefits.

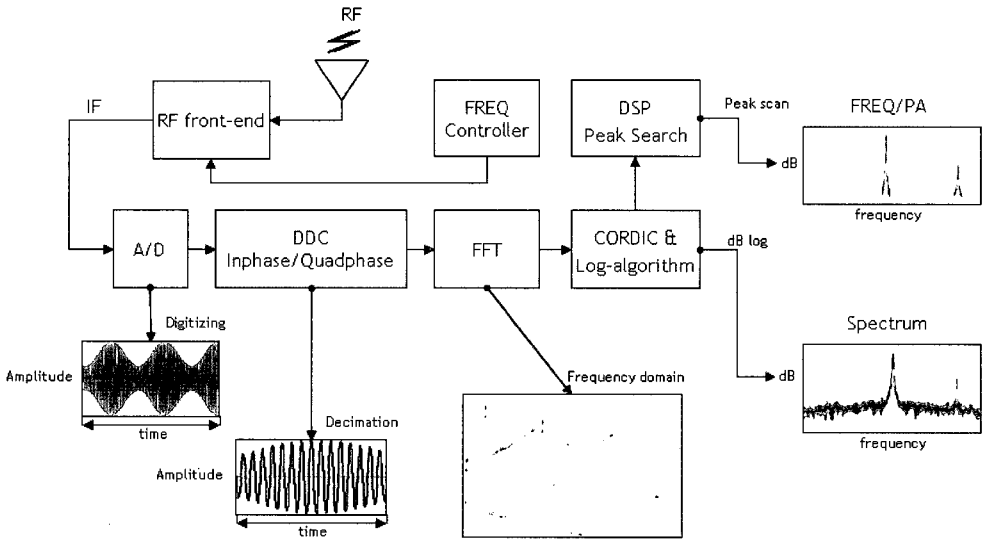
In this paper, the fast scan digital-IF FFT receiver are designed and analyzed for spectrum monitoring at the radio communication band. It has characteristics of fast scan rate, multi-resolution, high frequency accuracy and sensitivity, and flexibility. The fast scan rate make it useful for monitoring the frequency hopped spread spectrum signal suggested to reduce the interference jamming.

2. Design of the digital-IF FFT receiver

An operational diagram of the digital-IF FFT receiver architecture is shown in Fig. 1. It consists of RF front-end, local oscillator(LO) board, signal processing board. An unknown modulated signal is received by RF front-end where it is filtered, amplified, and down converted to a low IF signal. This signal is sampled by a high speed A/D converter and then down converted by digital down converter(DDC) to a baseband signal. Once decimated signal, a variety of processing such as FFT, CORDIC(coordinate rotation digital computer), log algorithm, and peak search is conducted to extract signal information.

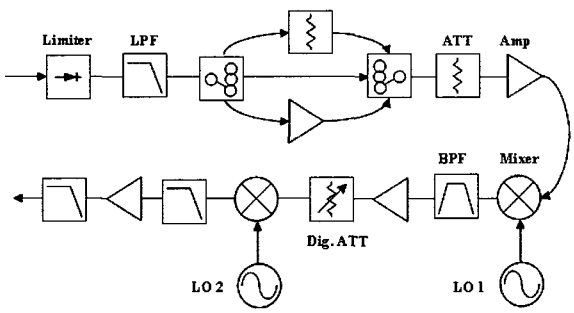
2.1 RF front-end

RF front-end is composed of two parts: amplification part and down-converter part as shown in Fig. 2. The former part plays role in boosting the desired signal level while minimally adding to the noise of the received signal. The limiter diode is inserted to protect RF circuits from high input signal and the switching path controls the instantaneous dynamic range up and down. The latter part down converts to RF



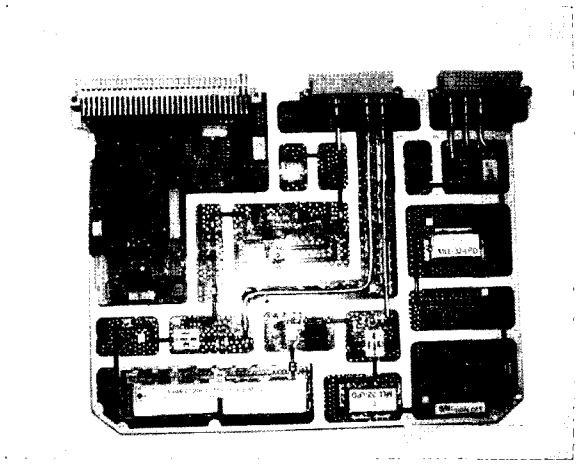
[Fig. 1] Functional diagram of the digital-IF FFT receiver

signal to a lower intermediate frequency(IF) by mixing the RF signal with a LO signal. The IF placement is carefully selected to reduce unwanted harmonics generated by amplifier and mixer. These spurious signals degrade the quality of receiver performance such as SFDR and signal identification. The IF is placed so that the second and third harmonics fall into unused sections of bandwidth as shown in Fig. 3. The image frequency will be rejected by the image rejection filter before mixer. The signal path gain is automatically controlled by using the received signal strength indicator(RSSI) to drive the A/D converter according to the received signal power. To improve the sensitivity and selectivity, a dual-conversion IF topology is employed. That is, the first IF(high) is used for image rejection, and the second IF(low) is used for ease of highly selective filtering. The implemented RF front-end is presented in Fig. 4.



[Fig. 2] Configuration of the RF front-end

[Fig. 3] IF frequency plan of the RF front-end

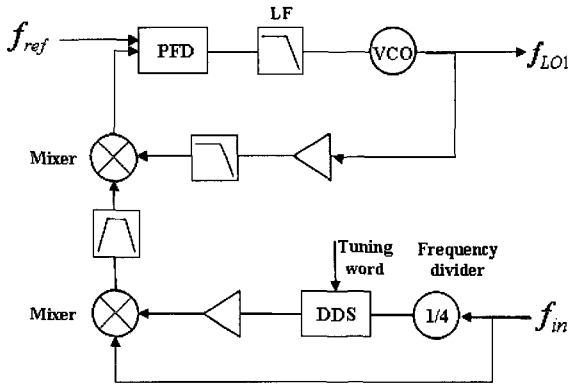


[Fig. 4] Photograph of the RF front-end

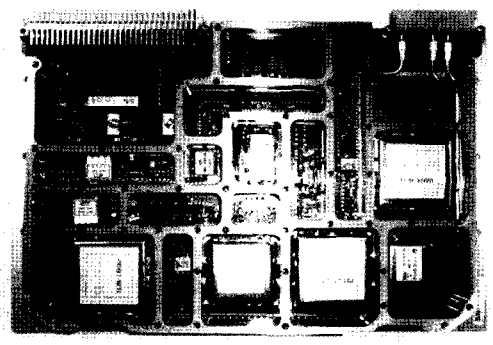
2.2 LO board

The frequency synthesizer is one of most essential components of the receiver. The frequency tuning range of several hundreds of megahertz has to be covered and adjusted within frequency steps of some tens of hertz or less for spectrum monitoring in dense EW environments[3]. Spurs must be minimized by using narrow loop bandwidth but also settling time in channel switching has to be short, in some case less than 1ms to monitor the fast frequency hopped signals[5]. To satisfy the above requirements, DDS-offset phase-locked loop(PLL) synthesizer is designed. It consists of phase detector, loop filter, voltage control oscillator(VCO) and direct digital synthesizer(DDS) as shown in Fig. 5. The DDS output signal controlled by the frequency tuning words(FTW) is fed into the first mixer and then is mixed with the VCO output in the PLL feedback path.

The employed DDS is tunable with a 32bit word, equivalent to minimum frequency step of less than 1Hz. The PLL module has a dual modulus prescaler that has pulse swallow function. The dual modulus prescaler make it possible for the frequency synthesizer to generate



[Fig. 5] DDS-offset PLL



[Fig. 6] Photograph of the LO board

higher output frequency and also finer frequency resolution. Since the VCO output is phase locked to the DDS, the output frequency of the VCO changes rapidly according to the change of DDS-offset frequency. This DDS-offset PLL synthesizer has characteristics of low phase noise, finer frequency resolution and fast settling time less than max 40μs. The implemented LO board is presented in Fig. 6.

2.3 Digital signal processing board

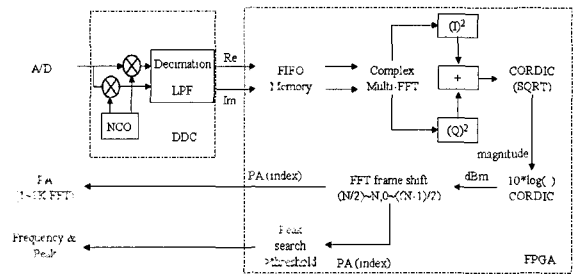
The A/D converter digitizes IF input signal with sampling rate of 85.6MHz with 14bit. The sampling rate should meet the following criterion[6]:

$$f_s = \frac{4f_{IF}}{2k-1} \tag{1}$$

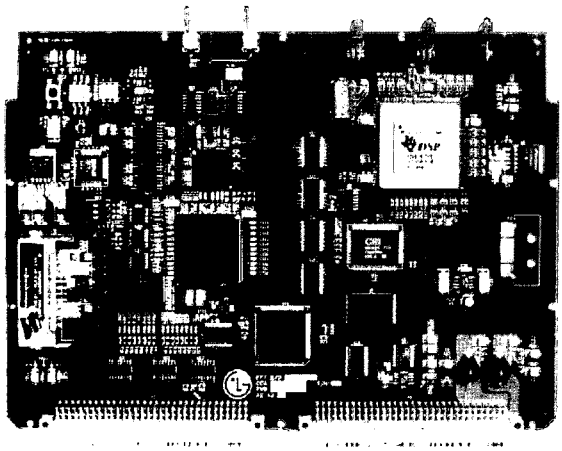
where k is the image number. For simple implementation, k=1 is selected. The digital samples coming out of A/D converter are being fed to digital down converter(DDC) and then numerically demodulated I and Q samples serially by using digital direct synthesizer(DDS). The decimating low pass filter accepts input samples from digital mixer at the full A/D sampling frequency. It performs a dramatic reduction in the signal bandwidth from 85.6MHz down to 10.625MHz, a decimation factor of 8 and also the sampling rate has reduced 10.625MHz for complex output. The decimation factor is determined:

$$Output\ bandwidth = \frac{Input\ sample\ rate}{N} \tag{2}$$

where N is decimation ratio. In our design, the decimation factors are selected as 8, 16, 32. That is, the signal bandwidth is controled from 10MHz to 2.5MHz. The complex output of the DDC allows to compute a complex FFT power spectrum centered at 0Hz. The FFT is designed as radix-4 FFT with multi-resolution from 1024 to 4096 FFT. This structure has fast processing time in comparison with radix-2 FFT because it has the separated memory in the input and output. After



[Fig. 7] Functional diagram of the signal processing board



[Fig. 8] Photograph of the signal processing board

the time-frequency conversion in the complex FFT, CORDIC and peak search algorithm is carried out to calculate magnitude and search the peak of signals. The functional diagram and photograph of the digital signal processing board are shown in Fig. 7 and Fig. 8 respectively.

3. Performance Analysis of the digital-IF FFT receiver

As noted earlier, the EW receivers should have high performance such as high sensitivity and wide dynamic range, low phase noise, and fast settling time and scan rate for spectrum monitoring applications. The typical recommended specifications for digital monitoring receivers are summarized in table 1.

3.1 Sensitivity

The receiver sensitivity is significant factor in the design of the EW receivers because they may have to work with very low input signal levels in the presence of very large levels of unwanted signal. Hence, the noise figure and linearity of the early stage, RF front-end of the receiver are of key importance. The receiver sensitivity is generally defined as the smallest signal that a receiver needs at its input to adequately process the signal. It is frequently expressed by:

[Table 1] Recommended specifications for digital monitoring receiver[3]

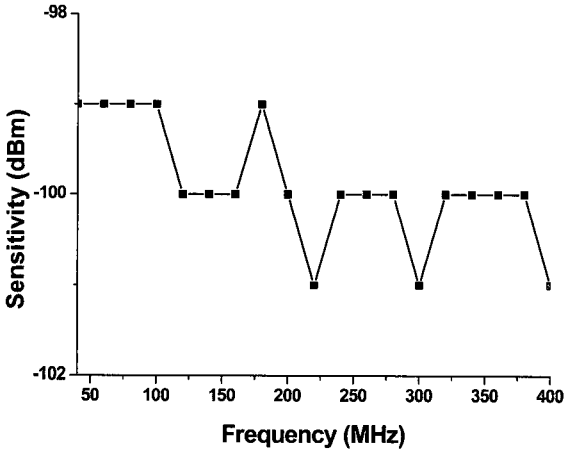
Parameter	Specifications
LO tuning resolution	≤ 10Hz
LO settling time	≤ 5ms
LO phase noise	-100dBc/Hz in 10kHz offset
Noise Figure	< 12dB
3rd order intercept	> 10dBm
2nd order intercept	> 40dBm
IF rejection	> 80dB
Image rejection	> 80dB
Input VSWR	< 2.5

$$Sensitivity = kTB + NF + SNR_{req} \quad (3)$$

where k is 1.38×10^{-23} J/K, T is ambient temperature in K, and B is noise bandwidth. Assume that B is 15kHz, SNR_{req} is 10dB, and NF is 10dB, The estimated sensitivity is -114dBm. The sensitivity is measured by the following procedures. At fixed frequency, the minimum signal power such that the receiver cannot detect the signal starts and then increase in steps, until the receiver can detect the correct frequency. The high sensitivity of below -99dBm is achieved as shown in Fig. 8.

3.2 Dynamic range

An important parameter in the spectrum monitoring receiver is receiver dynamic range.



[Fig. 8] Measured receiver sensitivity

Generally, a single signal dynamic range(SSDR) is taken as the ratio of the 1dB compression point level to the receiver noise level. This range must be capable of handling the signal power variation greater than 100dB owing to multi path and path loss. The SSDR of digital receiver achieved by 110dB and is accomplished with only RF front-end by use of an instantaneous automatic gain control(AGC).

The different definition of dynamic range is SFDR. It is informative to determine the dynamic signal operation range of a system from third order intermodulation. The third order intermodulation product signal levels are related to the level of the two signals. The SFDR can be estimated by the following relationship[7]:

$$SFDR = 2/3(IP3 - KTB(NF)) \quad (4)$$

Given that the measured IP3 is 26.3dBm, B is 15kHz, and NF is 10dB, the calculated SFDR is 93.5dB.

3.3 Settling time and phase noise

The fast settling time and good frequency resolution are required for EW receiver to monitor fast frequency hopped signals in the dense radio communication band. The settling time is generally defined as the time it takes for a PLL to switch from an initial frequency to a final frequency for a given frequency jump to within a given tolerance[8]. The settling time and frequency resolution of the PLL are measured by Spectrum Analyzer. They are achieved by maximum 35 us and 1Hz respectively. If the LO output contains phase noise, the desired signal is corrupted because the LO output is mixed with incoming signal. As a result of mixing, the phase noise from the LO causes energy from adjacent channels to integrate into the desired channel as an increased noise floor. The quantity of the phase noise for fractional-N synthesizer can be estimated by:

$$\begin{aligned} Phase\ noise = {} & (1Hz\ normaized\ phase\ noise) \\ & + 10^{*} log(comparison\ frequency) \\ & + 20^{*} log(N) \end{aligned} \quad (5)$$

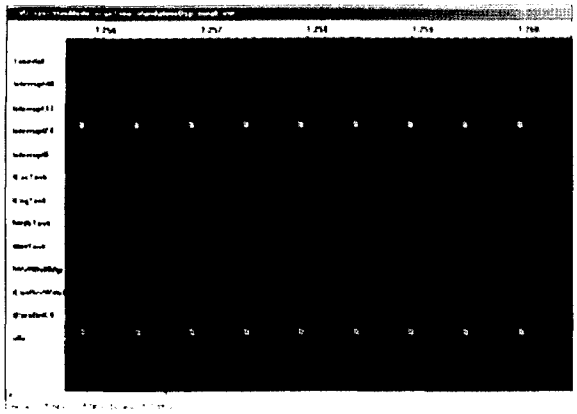
The measured phase noise is obtained by below -99.7dBc/Hz in 10kHz offset.

3.4 Scan rate

The fast scan rate is also important factor for spectrum monitoring receiver. It provides high probability interception of the frequency hopped spread spectrum signal suggested by reducing the interference jamming. The scan rate can be calculated by:

$$Scan\ rate = B_{INS} / T_{PRO} \quad (6)$$

where B_{INS} is instantaneous bandwidth and T_{PRO} signal processing time for extracting information such as frequency, magnitude, peak signal from unknown transmitted signals. The scan rate is measured by using two oscilloscopes and signal



[Fig. 9] Scan period of instantaneous bandwidth of 10MHz.

generators, and controling PC. In order to keep the scan rate consistent, the measurement is repeated above 10 times. Fig. 9 shows the scan period within instantaneous bandwidth of 10MHz to measure the scan rate. The scan rate is achieved around 19.33GHz/s.

4. Conclusion

We have developed a fast scan digital-IF receiver for spectrum monitoring in the radio communication band. To improve the scan rate and wide frequency coverage, the DDS-offset PLL with fast settling time is designed. The designed DDC and Radix-4 FFT with multi-resolution provide short signal processing time and flexibility of instantaneous bandwidth and frequency resolution. The high performance of this receiver makes it useful for spectrum monitoring receiver in the radio communication band.

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