

# The Neural-Network Approach to Recognize Defect Pattern in LED Manufacturing

Wen-Chin Chen<sup>1</sup>, Chih-Hung Tsai<sup>2†</sup>, and Shou-Wen Hsu<sup>1</sup>

<sup>1</sup>Graduate Institute of Management of Technology  
Chung-Hua University  
30 Tung-Shiang, Hsin-Chu, Taiwan, ROC

<sup>2</sup>Department of Industrial Engineering and Management  
Ta-Hwa Institute of Technology 1 Ta-Hwa Road, Chung-Lin  
Hsin-Chu, Taiwan, ROC  
Tel: +886-3-5430-466 Fax: 886-3-5926-848  
E-mail: ietch@thit.edu.tw

## Abstract

This paper presents neural network-based recognition system for automatic light emitting diode (LED) inspection. The back-propagation neural network (BPNN) is proposed and tested. The current-voltage (I-V) characteristic data of LED from the inspection process is used for the network training and testing. This study selects 300 random samples as network training and employs 100 samples as network testing. The experimental results show that if the classification work is done well, the accuracy of recognition is 100%, and the testing speed of the proposed recognition system is almost one half faster than the traditional inspection system does. The proposed neural-network approach is successfully demonstrated by real data sets and can be effectively developed as a recognition system for a practical application purpose.

**Key Words:** Neural Network-based Recognition System, Light Emitting Diode, Back-propagation Neural Network, Current-voltage (I-V) Characteristic Data

## 1. Introduction

Due to the dramatic change of international economic environment in recent years, semiconductor manufacturers have faced unprecedented operation dilemmas and challenges, and several back end semiconductor manufacturers were forced to merge. To survive in such a competitive environment, semiconductor manufacturers must have superb products and pro-

---

†Corresponding Author

---

duction technology and must seek opportunities for cost reduction and sales increase. In consequence, semiconductor manufacturers continuously improve their production capability and increase production efficiency. The light emitting diode (LED) technology has developed for the past few decades. The epitaxy process, one of the critical processes in semiconductor manufacturing, determines the product quality of LEDs. Any contamination or defect occurred during the epitaxial process can cause a non-intrinsic P-N junction diode, which degrades the performance of LEDs. The testing process for detecting failed diodes is very complicated. Even though there are several types of inspection systems available, they are usually time-consuming in inspection, especially for traditional testing systems. Because a short testing time is particularly concerned by the LED industry, the development of an automatic testing process is essential for LEDs manufacturing to increase the testing speed and the product competitiveness.

In the recent years, many researchers have investigated the use of neural networks for automatic semiconductor inspection systems (Obaidat *et al.*, 1998; Chen and Liu, 2000; Lee *et al.*, 2001; Bhatikar and Mahajan, 2002; Mehrotra *et al.*, 2000; Chen *et al.*, 2003; Palma *et al.*, 2005; Sharma *et al.*, 2005). The major reason for adopting neural networks is because a neural network has a better sample identification capability on the problem of non-linear system categorization. Numerous researchers have studied pattern classification by using back-propagation neural networks (BPNN) for the automatic inspection system in the semiconductor industry (Zoroofi *et al.*, 2001; Su *et al.*, 2002; Chen *et al.*, 2005). Zoroofi *et al.* (2001) used curve recognition to detect the contamination on a wafer surface during semiconductor production. Three conventional classification models, a back-propagation technique, a minimum distance algorithm and a maximum likelihood classifier, were used and the performance of three models was compared. The results showed that the back-propagation classifier has a better classification performance. Su *et al.* (2002) proposed a neural-network approach for semiconductor wafer post-sawing inspection. BPNN, radial basis function network (RBFN), and learning vector quantization (LVQ) were employed in the inspection models. The inspection results showed that both BPNN and LVQ have excellent prediction result with 100% accuracy. Chen *et al.* (2005) used BPNN in the etch semiconductor process to identify and classify endpoint curves. By real-time monitoring of changes in the endpoint curve, the abnormalities of products can be detected immediately. The system can reduce the uncertainty in the process curve classification and provide machine shut-down suggestion immediately when necessary. The common characteristics of BPNN, as suggested by previous studies, are an easier-comprehended theory, a faster recalling speed, and higher learning accuracy. However, the superiority of a network's function approach depends on the network architecture and parameters, and the problem complexity. If inappropriate network architecture and parameters are selected, the results may be undesirable. Conversely, the results will be much more significant if good network architecture and parameters are selected. The BPNN consists of input layer, hidden layer and output layer. The parameters for the BPNN include:

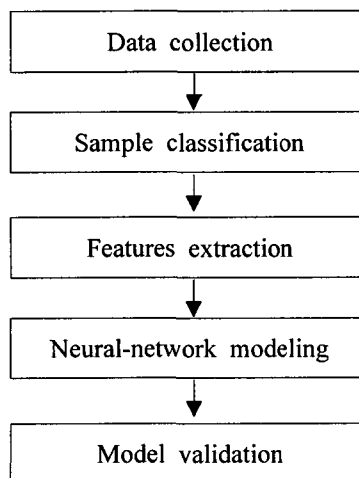
---

the number of hidden layers, number of hidden neurons, learning rate, momentum, etc. All of these parameters have significant impacts on the performance of the neural network. Fogel (1991) proposed final information statistic (FIS) process based on Akaike's information criterion (AIC) to determine the number of hidden layers and neurons. The limitation of Fogel's research is that the process can only perform in simple binary classifications. Murata & Yoshizawa (1994) and Onoda (1995) proposed a method to improve AIC, respectively. These methods, called network information criterion (NIC) and neural network information criterion (NNIC), use statistical probability together with an error energy function to determine the number of hidden neurons.

In this study, an automatic inspection system is developed for the semiconductor LED manufacturing. The BPNN is applied to the proposed system. In the experiment, an 8255 card with PCI interface connects an industrial computer and the tester for controlling the current and voltage of the tester. The tester transmits the desired current and voltage levels to the prober. The prober tests every single diode, and the output current and voltage from a prober is digitalized by analog/digital converter (A/D) and then stored in the PC database. These data are next pre-processed and used as input variables for neural networks. The rest of this paper is organized as follows. Sections 2 and 3 provide model construction and give the experimental results and some discussions. Some conclusion remarks are made in the last section.

## 2. The Model Construction and Experiment

The purpose of this study is to develop an automatic LED inspection system with high speed



**Figure 1.** Flow chart of the proposed approach

and accuracy to replace current traditional inspection system. The flow chart of this research is as shown in Figure 1, and is divided into five stages: data collection, sample classification, features extraction, neural-network modeling and model validation.

## 2.1 Data Collection

This research focuses on the LED inspection process in the semiconductor industry. Data is collected from an anonymous LED manufacturing company located in Hsinchu, Taiwan. The constructed system from circuit hardware to software is as shown in Figure 2. Because the testing needs to be performed according to different LED product classifications, the circuit hardware of the tester has to provide several different voltage/current levels. The tester used in this research has 25 different current levels and 3 different voltage levels. An 8255 card with PCI interface connects an industrial computer and the tester for controlling the current and voltage of the tester. The tester transmits the desired current and voltage levels to the prober. The prober tests every single diode, and the obtained current and voltage levels

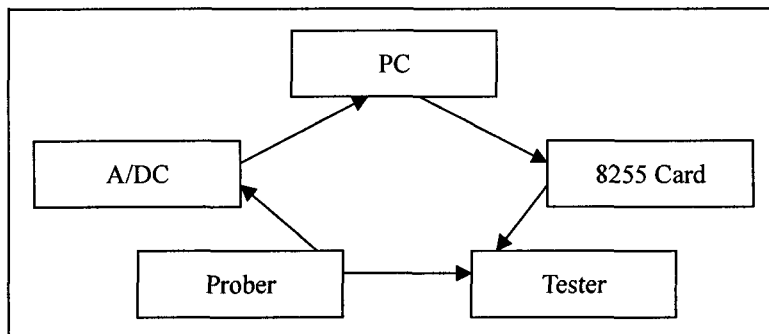


Figure 2. Flow chart of the testing system

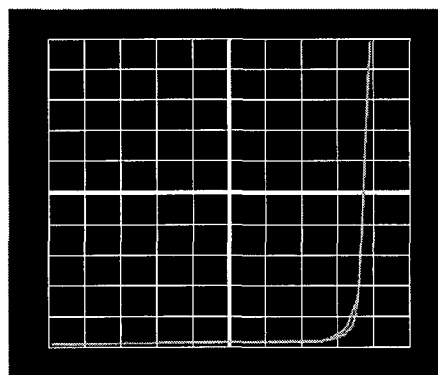


Figure 3. Process curve generated by a computer

are output to PC via 16 bits A/DC. To ensure the accuracy in providing current and voltage levels of designated diodes and to strictly synchronize the response time of the 8255 card and A/DC, an interface program is written by Turbo C and Visual Basic software. The collected data is then regenerated into a curve through the computer program. An example of the regenerated curve is shown in Figure 3, where the horizontal axis is voltage and the vertical axis is current.

## 2.2 Sample Classification

The LEDs are P-N junction diodes which are formed by joining p-type and n-type semiconductors together. When current passes through the normal diode, the current-voltage (I-V) curve of a diode has the characteristic of a positively increasing function. However, particles or any other contamination on the LED wafer can cause many different defects, which can result in mal-functional diodes in the final products. A normal diode and an abnormal diode can be observed from the I-V characteristics when voltage is applied. In this study, four types of product are classified based on the I-V characteristics. The first type is normal diodes, and the I-V curve of a diode has the characteristic of a positively increasing function, as shown in Figure 4. The second type is diodes with two I-V curves. This type of diodes can be further categorized into two kinds of products. If the difference between the two curves is less than 5%, the diodes are normal. Otherwise, the diodes are abnormal. These two kinds of diodes are as shown in Figures 5 and 6. The third type is diodes with the thyristor effect (or snapback effect) and is as shown in Figure 7. No matter there is one or two curves, they are treated as abnormal. The fourth type, as shown in Figures 8 and 9, is diodes with a large irregular variation I-V curve. The diodes usually have very large thyristor effect, and they are treated as abnormal. In the above-stated figures, the vertical axis is the current level, and the horizontal axis is the voltage level. Each grid represents the level of the adjusted I-V. The area that the arrow pointed to is the zone with the thyristor effect. In this zone, the I-V curve may not be a positively increasing function. If a diode is found

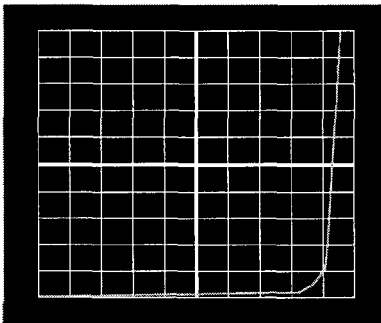


Figure 4. Type I for normal diodes

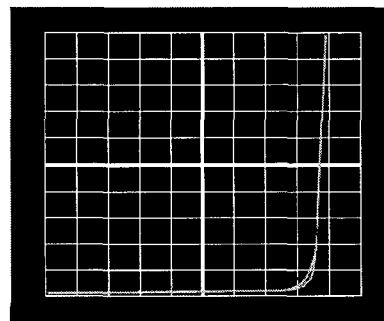


Figure 5. Type II for normal diodes

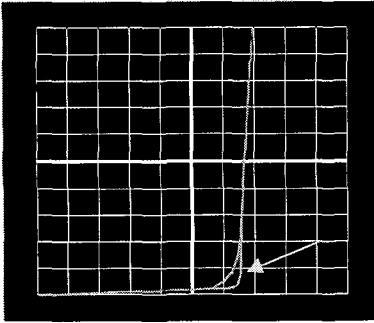


Figure 6. Type II for abnormal diodes

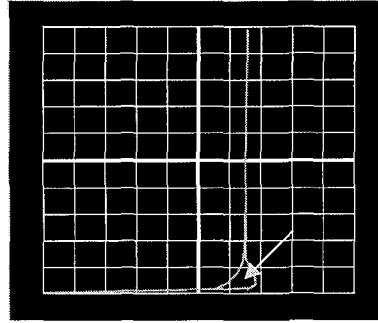


Figure 7. Type III for abnormal diodes

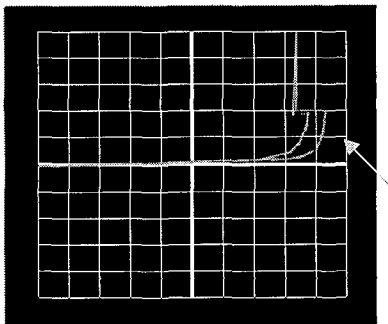


Figure 8. Type IV for abnormal diodes (1)

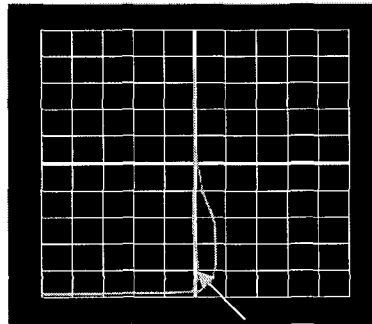


Figure 9. Type IV for abnormal diodes (2)

with the thyristor effect, it is determined as abnormal diode. Therefore, in this research, we can classify products as either normal or abnormal according to the I-V characteristics.

### 2.3 Features Eextraction

Currently, the LED inspection is done by comparing a section of I-V curve with the normal pattern, or by checking whether the maximum voltage level is larger than the final voltage level. If the number of data collection is numerous, the sampling time for generating an I-V curve is time-consuming, and current method is not suitable for in situ inspection. This research first bases on a statistical method for classifying the diodes to find out the location of abnormal diodes. The results show that about 64% of abnormal diodes are located at low current level (1~200  $\mu\text{A}$ ), 22% at medium current level (200~900  $\mu\text{A}$ ), 11% at high current level (1-5 mA), and about 3% at a current level  $> 5$  mA. Therefore, the products are classified into three zones: high current zone, medium current zone and low current zone. Twenty-five points are selected from these three zones as current characteristic values, and three points are chosen from vertical axis as voltage characteristic values. Another 25 points with the same current characteristic values are selected again after 0.1 second. A total of 53

points are collected and characteristic points for I-V curve is shown in Table 1. These I-V curve values are provided for the designed neural network as input variables.

**Table 1.** Characteristic points for I-V curve

| Characteristic points | Current values | Characteristic points | Current values | Characteristic points | Current values | Characteristic points | Voltage values |
|-----------------------|----------------|-----------------------|----------------|-----------------------|----------------|-----------------------|----------------|
| 1                     | 1 $\mu$ A      | 11                    | 200 $\mu$ A    | 21                    | 1 mA           | 1                     | 1.7 V          |
| 2                     | 3 $\mu$ A      | 12                    | 250 $\mu$ A    | 22                    | 2 mA           | 2                     | 1.8 V          |
| 3                     | 5 $\mu$ A      | 13                    | 300 $\mu$ A    | 23                    | 3 mA           | 3                     | 1.9 V          |
| 4                     | 10 $\mu$ A     | 14                    | 350 $\mu$ A    | 24                    | 4 mA           |                       |                |
| 5                     | 15 $\mu$ A     | 15                    | 400 $\mu$ A    | 25                    | 5 mA           |                       |                |
| 6                     | 20 $\mu$ A     | 16                    | 500 $\mu$ A    |                       |                |                       |                |
| 7                     | 25 $\mu$ A     | 17                    | 600 $\mu$ A    |                       |                |                       |                |
| 8                     | 50 $\mu$ A     | 18                    | 700 $\mu$ A    |                       |                |                       |                |
| 9                     | 100 $\mu$ A    | 19                    | 800 $\mu$ A    |                       |                |                       |                |
| 10                    | 150 $\mu$ A    | 20                    | 900 $\mu$ A    |                       |                |                       |                |

### 3. Neural-network Modeling and Model Validation

This research establishes a systematic approach for semiconductor LED inspection. Two types of neural networks are applied to the proposed approach. The details of neural-network modeling and model validation are discussed as follows:

#### 3.1 Backpropagation Neural Network (BPNN) and Parameter Setup

In this research, the steepest descent method is used to find the weight change and to minimize the error energy function. The activation function is a hyperbolic tangent function,  $f(x) = \tanh(x)$ . According to past studies (Cheng and Tseng, 1995; Hush and Horne, 1993), there are a few conditions for network learning termination: (1) when the root mean square error (RMSE) between the expected value and network output value is reduced to a preset value; (2) when the preset number of learning cycles has been reached; (3) when cross-validation takes place between the training samples and test data. The first two methods are related to the preset values. This research adopts the first approach by gradually increase the network training time to gradually decrease the root-mean-square error (RMSE) until the RMSE is stable and acceptable. The RMSE is defined as follows:

$$RMSE = \frac{1}{N} \sqrt{\sum_{i=1}^N (d_i - y_i)^2}$$

where  $N$ ,  $d_i$  and  $y_i$  are the number of training samples, the actual value for training sample  $i$ , and the predicted value of the neural-network for training sample  $i$ , respectively;  $d_i$  is either 1 or 0 to represent a good or bad pattern; and  $y_i$  is between 0 and 1. When applying the neural network to the system, sample collection, features extraction and random samples testing are considered to verify the learning effectiveness. To determine the number of hidden layers, this research tests both one and two hidden layers. The result shows that one hidden layer is enough to produce the ideal result. The number of neurons in the hidden layer is a major factor that affects the result, and this number is set to twenty six after a few tests are performed. The learning rate is 0.7, the learning decay rate is 0.95, and the number of epochs for the learning decay rate is 500. Because the momentum does not affect convergence significantly, we set the moment at 0.6 after a few tests are performed.

### 3.2 Experimental Procedures

In this study we randomly choose curves generated by different production lines as system training and testing samples. The main reason is that the training and testing samples should cover different levels of changes in normal and abnormal patterns to generalize the trained and tested results. Three hundred samples are randomly collected as training samples from the historical data stored in the database. Another one hundred samples are used to test the training result. The experimental procedures used in this research are divided into four steps, described as follows:

- Step 1:** Based on the engineers' experience, classify the curves collected in the database through the A/DC using a developed program.
- Step 2:** Assign a computer code to each of the 300 curves collected according to the classification, and store the curves as a training file. During the learning process, the RMSE value decreases when the number of iteration epochs increases. The learning process is continued until the desired RMSE value is achieved. The classification code for the training file is then removed and the file is saved as another test file. The purpose of this test file is to put the original training data into the system for testing after the training file has completed its job. Theoretically, the test recognition rate should be 100% since these data are the original training data. If the tested result is not 100%, this means that the training data is not correctly classified or that the optimum weighted value is not trained. Because there always have noise in the samples, the trained network output value will not be exactly 0 or 1 even though



the process curve state is set at either 0 or 1. Therefore, the threshold values must be established to determine whether the output value is close to the target value. Using the simplest trichotomy method, we define the value range between Min value and Max value. This is an ambiguous range, and any trained network output value that falls within this range is considered a failed recognition. Adjustment on Min and Max values can be made during the test of the training data. The purpose of these adjustments is to identify the range of the weighted values trained by the neural-network under different patterns of sample data. For example, we can increase the Min value and decrease the Max value to observe the change in corresponding results. Table 2 shows that different ranges lead to significant different recognition rates (Chen *et al.*, 2005). Since the network output value falls between 0 and 1, the zone that network output value is smaller than the Min value is set to 0 and the zone that network output value is greater than the Max value is set to 1. The ambiguous zone is between the Min value and the Max value, and any trained network output value that falls within this range is considered a failed recognition. The most suitable range should be subjectively determined by the process engineers. If the test recognition rate does not fall within a satisfactory range, the curves must be fed back into the system for re-learning or the samples must be reclassified.

**Table 2.** The result generated using different zone values

| No               | 1      |     | 2      |      | 3      |     | 4      |      | 5    |     |
|------------------|--------|-----|--------|------|--------|-----|--------|------|------|-----|
| Zone value       | Min    | Max | Min    | Max  | Min    | Max | Min    | Max  | Min  | Max |
|                  |        | 0.3 | 0.7    | 0.25 | 0.75   | 0.2 | 0.8    | 0.15 | 0.85 | 0.1 |
| Recognition rate | 97.67% |     | 96.79% |      | 96.21% |     | 93.29% |      | 20%  |     |

**Step 3:** Load the test sample file into the testing program.

**Step 4:** Load the trained and tested neural-network program into the production line system.

After a wafer has completed its production process, the data of the wafer is standardized and a curve is generated for recognition in the network.

### 3.3 Experimental Results and Discussions

In this research, we apply BPNN to LED curve recognition. The neural network is trained by the 300 pieces of training data, and the 100 pieces of verifying data are used to make curve recognition. From the experimental results, the present model has 100% accuracy, and the relationship between RMSE and iteration epochs is shown in Figure 10. The ambiguous threshold zone is set between 0.4 and 0.6 after network training is finished. Any trained network output value that falls within this range is considered a failed recognition. When

applying this method to the production line, a failed recognition shall cause an alarm for calling the engineers' or operators' presence to verify whether the curves are normal.

For current traditional LED inspection systems, the testing speed must maintain about 3.5~4.0 die/sec, and a short testing time is particularly concerned by the LED industry. This research simulates 3-inch silicon wafer on the inspection system by applying BPNN. The proposed system simultaneously test 55,000 dies in a 2.8 GHz PC. The results show that the testing speed of the proposed inspection system is approximately 6.4 die/sec. As a result, the proposed approach is better than the current traditional LED inspection system. The present experiment is performed at off-line status to achieve automatic pattern recognition. The results show that if the classification work is done well, the accuracy can be up to 100% and the testing speed of the proposed approach is almost one half faster than the traditional system does. This research can improve the performance of the traditional LED inspection process and provides a better approach for the future LED inspection system.

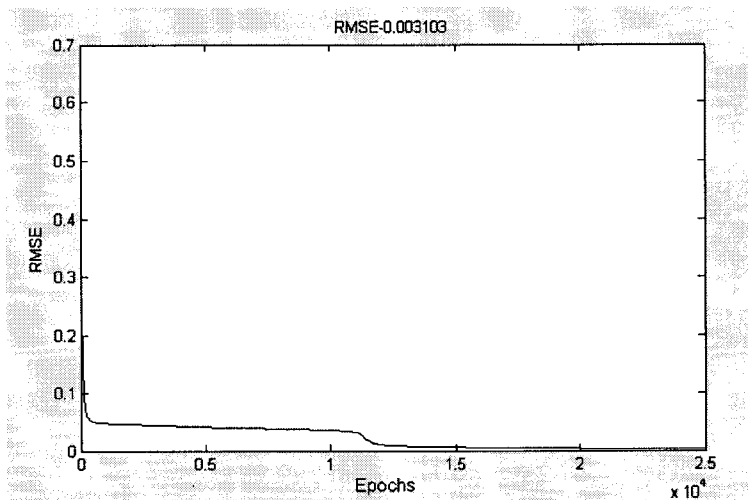


Figure 10. RMSE versus iteration epochs for BPNN

#### 4. Conclusion

This research develops a neural network application to LED process curve recognition. The BPNN is employed and tested. The empirical results show that when ambiguous threshold zone is set between 0.4 and 0.6, the proposed model has 100 % accuracy of recognition. In addition, the testing speed of the LED inspection system is almost one half faster than the traditional system does. The proposed neural-network approach is successfully

demonstrated by real data sets and can eventually be developed as an on-line system for ideal LED automation inspection.

## References

1. Bhatikar, S. R. and Mahajan, R. L.(2002). Artificial neural-network-based diagnosis of CVD barrel reactor. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 15, No. 1, pp. 71-78.
  2. Chen, F. L. and Liu, S. F.(2000). A neural-network approach to recognize defect spatial pattern in semiconductor fabrication. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 13, No. 3, pp. 366-373.
  3. Chen, F. L., Liu, S. F., Doong, Y. Y. and Young, K. L.(2003). LOGIC product yield analysis by Wafer Bin Map pattern recognition supervised neural network. *IEEE International Symposium on Semiconductor Manufacturing*, No. 1, pp. 501-504.
  4. Chen, W. C., Chen, C. T., Ho, T. H., Chen, J. H. and Sheu, L. J.(2005). Use of neural network in pattern recognition of semiconductor etching process. *The Proceedings of the 11<sup>th</sup> International Conference on Industrial Engineering and Engineering Management*, No. 1, pp. 719-725.
  5. Cheng, C. S. and Tseng, C. A.(1995). Neural network in detecting the change of process mean value and variance. *Journal of the Chinese Institute of Industrial Engineers*, Vol. 12 No. 3, pp. 215-223.
  6. Fogel, D. B.(1991). An information criterion for optimal neural network selection. *IEEE Transactions on Neural Networks*, Vol. 2, No. 5, pp. 490-497.
  7. Hush, D. R. and Horne, B. G.(1993). Progress in supervised neural networks. *IEEE Signal Processing Magazine*, Vol. 10, No. 1, pp. 8-39.
  8. Lee, J. H., You, S. J. and Park, S. C.(2001). A new intelligent SOFM-based sampling plan for advanced process control. *Expert Systems with Applications*, No. 20, pp. 133-151.
  9. Mehrotra, K., Mohan, C. K., et Ranka and Sanjay, R.(2000). *Elements of artificial neural networks*. MIT Press: Cambridge, Massachusetts.
  10. Murata, N., Yoshizawa, S. and Amari, S.(1994). Network information criterion-determining the number of hidden units for an artificial neural network model. *IEEE Transactions on Neural Networks*, Vol. 5, No. 6, pp. 865-872.
  11. Obaidat, M. S., Khalid, H. and Sadoun, B.(1998). Ultrasonic transducer characterization by neural networks. *Journal of Information Sciences*, No. 107, pp. 195-215.
  12. Onoda, T.(1995). Neural network information criterion for optimal number of hidden units. *Proceedings of the IEEE International Conference on Neural Networks*, No. 1,
-

pp. 270-280.

13. Palma, F. Di., Nicolao, G. De., Miraglia, G., Pasquinetti, E. and Piccinini, F.(2005). Unsupervised spatial pattern classification of electrical-wafer-sorting maps in semiconductor manufacturing. *Pattern Recognition Letters*, No. 26, pp. 1857-1865.
  14. Sharma, V., Jha, R. and Naresh, R.(2005). An augmented Lagrange programming optimization neural network for short-term hydroelectric generation scheduling. *Engineering Optimization*, Vol. 37, No. 5, pp. 479-497.
  15. Su, C. T., Yang, T. and Ke, C. M.(2002). A neural-network approach for semiconductor wafer post-sawing inspection. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 15, No. 2, pp. 260-266.
  16. Zoroofi, R. A., Taketani, H., Tamura, S., Sato, Y. and Sekiya, K.(2001). Automated inspection of IC wafer contamination. *Pattern Recognition*, No. 34, pp. 1307-1317.
-