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전력선 계통의 순시 전압 강하 제어기 설계

(Instantaneous Voltage Sag Corrector Conrtroller Design of Power Line System)

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(Sang-Hoon Lee · Hyun-Mun Hong)

요 약

본 논문은 전력품질 향상을 목적으로 VSC의 새로운 제어 기법의 디자인에 대하여 기술하였다. 전압강하의 빠른 검출 기술은 동기 회전 d·q-기준축에서 순시값의 검출을 통해서 구현되었다. 1차 디지털 필터는 노이즈에 대하여 둔감한 특성을 막을 수 있는 검출 알고리즘을 부가하였다. 필터의 전체 검출과 컷오프 주파수 사이에서 관계에 대하여 기술하였다. 에너지 저장 요소로서 사용되는 캐패시터 뱅크의 사이즈는 회로 해석으로서 입·출력 에너지의 관점에서 디자인 되었다. 마지막으로, 제안된 기법의 유효성은 모의실험을 통하여 증명되었다.

Abstract

This paper describes the novel control techniques design of VSC(Voltage Sag Corrector) for the purpose of power line quality enhancement. A fast detecting technique of voltage sag is implemented through the detection of instantaneous value on synchronous rotating dq-reference frame. The first order digital filter is added in the detection algorithm to protect the insensitive characteristics against the noise. The relationship between the total detection time and cut-off frequency of the filter is described. The size of the capacitor bank used as the energy storage element is designed from the point of view of input/output energy with circuit analysis. Finally, the validity of the proposed scheme is proven through the simulated results.

Key Words : VSC(Voltage Sag Corrector), Power Quality, Faults, Series Compensation, PSCAD/EMTDC

1. INTRODUCTION

The power line has a lot of disturbances such as sags, swells, harmonics, and etc. The voltage sag is the most frequent problem among them, and it is caused by the following two reasons. One is the line fault, especially SLGF(Single Line-to-Ground Faults). The other is caused by the load characteristics, for example motor starting. Until a few years ago, the voltage sag seldom affected to most of system. But it can induce the fatal results to the load today; automatic manufacturing processor using computer system, electronic

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equipment with high accuracy, sensitive communication equipment, and high-technology medical facilities. So the regulation of the line voltage or the compensation of the line voltage sag has become one of the most prolific issues in the power quality industry[1].

Mark F. McGranaghan proposed the CVTs(Constant Voltage Transformers) for thecompensation of voltage sags. This is easy and economic to install, but not efficient under the variable load condition or the large inrush current condition as the fixed output voltage. The UPS(Uninterruptible Power Supply) is more excellent than CVTs, which can generates the constant voltage and constant frequency ac power at any load conditions. But it needs frequent maintenance and repair, and its cost is too high. So it is not proper to apply to the power distribution line. The other solution is a VSC(Voltage Sag Corrector) using series compensator. The VSC protects the sensitive load against the voltage sag at the PCC(Point of Common Coupling). This scheme has a good dynamic characteristics and relatively economical advantage to the former case, so the research has progressed in active. But the existing studies made no mention for the following terms in spite of the importance: [2~6]

1. Fast detecting technique when the voltage sag occurs
2. Insensitive operation against the noise
3. Design process for the rating of an energy storage system (dc capacitor)

This paper proposes the novel control techniques of VSC to overcome the above limits. The fast detecting technique of voltage sag is accomplished through the detection of instantaneous value on synchronous rotating dq-reference frame. The robust characteristic against the noise is available by inserting the first order LPF(Low Pass Filter) in the detection circuit. The relationship between the detecting speed and the cut-off frequency of the filteris induced as a numerical formula. Because the VSC system supplys the active power to load, it is required to design the proper size of the ESS(Energy Storage Element), such as the capacitor bank, battery or flywheel system, and etc. In this paper, the capacitor bank is used as an ESS, and the size of the capacitor is designed from the point of view the input/output energy as the output power rating and the magnitude and duration time of the voltage sag. The filter design process is described properly with the mathematical equations. The simulation is accomplished by PSCAD/ EMTDC UNIX version. This paper consists of 4 terms: basic theory of the VSC, detection method of the line disturbances, design of the DC capacitor and simulation results.

2. System and Control Alogorithm

The general requirements to be met by a voltage sag corrector are the following; fast dynamic response, robust characteristic for noise, and insulation of harmonics. The last requirement is not mentioned in this paper.

The control block diagram is shown in fig.1. The proposed control scheme is based on instantaneous control scheme with double control structure to improve dynamic response. During the fault conditions, the controller is operated constantly to keep the load voltage. Otherwise during normal conditions, the DC capacitor is charged from source and the controller is not operated at this time.

The proposed controller is consisted of 4 parts; detection part, PLL part, feedforward and feedback

compensator with general PI(Proportion Integrator) controller, and PWM part.

In general, the feedforward compensator has two main objecties. First, it can remove the coupling terms which is resulted in synchronous reference frame transformation. Second, inherent disturbances which is included in the inverter system, can be canceled by feedforward compensation of capacitor voltage and load current. Moreover, the dynamic response of controller can be improved in the predictive technique of load current.

The feedback compensator is double control structure which is combined with voltage controller as outer loop and current controller as inner loop. Because the response of capacitor voltage is very slow, fast dynamic response is available by the adding a reactor current controller. The significant issue in the feedback compensator must be decided in the reference voltage. In the next, the positive and negative symmetric components of injected voltage to load are given by:

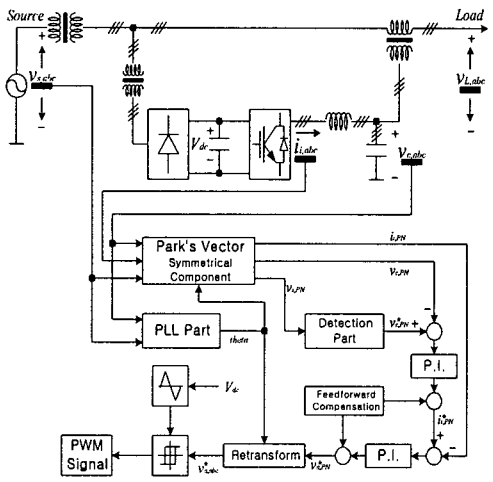


Fig. 1. Control block diagram

$$v_{c,P} = v_{ref,P} - v_{s,dqP} \quad (1a)$$

$$v_{c,N} = v_{ref,N} - v_{s,dqN} \quad (1b)$$

where, $v_{ref,P}$ is a peak value of the source voltage and $v_{ref,N}$ is zero. Thus, the capacitor voltage controller is compared with reference voltage and actual load voltage, the difference being supplied by the VSC.

3. Detection Method

The detection algorithm has to satisfy the following requirements: fast detection time and robust characteristics for noise. The existing method, averaging method has a disadvantage of long detection time and precise zero crossing detection. But in this paper, because the faults detection is implemented in synchronous reference frame the zero crossing detection is not need. Also the robust characteristics for noise is available to adding the first order LPF as shown in fig 2.

In fig.2, if e_{LDF} is less than e^*_d, the controller regards e_d as a noise. As a consequence, total detection time is the time when e_{LDF} is same e^*_d. And the total detection time is calculated using transfer function such as (2).

From (2), the relationship between the detection time and cut-off frequency of LPF is shown in fig.1. The figure describe that the cutoff frequency is the higher in the detection time is the shorter, but sensitivity for noise is increased.

$$T_{det} = -\frac{1}{2\pi f_c}\ln\left(1-\frac{e^*_d}{e_d}\right) \quad (2)$$

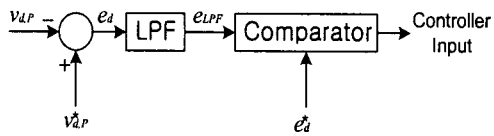
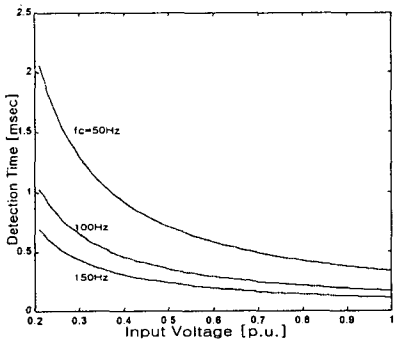
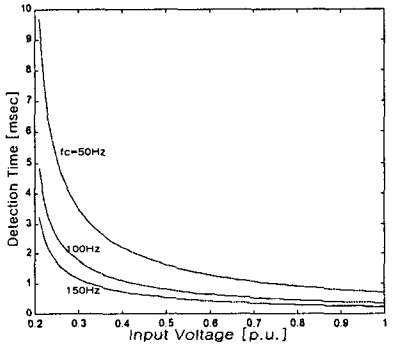


Fig. 2. Detection block diagram



(a) e_d^* = 0.1 [p.u.]



(b) e_d^* = 0.2 [p.u.]

Fig. 3. Input voltage and detection time

4. DESIGN OF DC CAPACITOR

Generally, the VSC consists of three parts: energy conversion part, energy storage part, and coupling part. Specially, because the VSC system supply the active power to load, it is required ESS, such as capacitor with rectifier, battery, FES, and SMES. In this paper, the capacitor is used as an ESS.

The capacitor is charged from source in the normal condition, and it supplies the active power to load in the fault condition. The critical issue in the design of the capacitor is amplitude and duration time of the faults. So, if we know those parameters, we can calculate the capacitance from the point of view input/output energy.

First for convenience, it is need assume such as:

- ◆ neglect of losses in switching elements and output filter.
- ◆ neglect of losses in transformer
- ◆ the capacitor voltage is 1.35 times of line-to-line voltage

From fig.1, we can write input/output power such as (3), when load power factor is cos.

$$P_{in} = V_{dc} \cdot I_{dc}[W] \tag{3a}$$

$$P_{out} = \sqrt{3} v_{c,p} i_o \cos\phi\,[W] \tag{3b}$$

The input/output energy is given by:

$$W_{in} = \frac{1}{2} C_i (V_{dc} - V_{low})^2 [J] = \frac{0.24}{860} \frac{1}{2} C_i (V_{dc} - V_{low})^2 [Wh] \tag{4a}$$

$$W_{out} = P_{out} \cdot T_{duration}[Wh] \tag{4b}$$

where, the Vlow is lower limit of DC voltage which is mean controllable area of inverter and its value changes according to fault conditions. The T duration is a fault duration time. Thus, if we know output power and T duration, we can calculate the DC capacitance from (4).

$$C_i = \frac{860 \cdot 2 \cdot W_{out}}{0.24 \cdot (V_{dc} - V_{low})^2}\,[F] \tag{5}$$

5. SIMULATION RESULTS

The simulation is accomplished by PSCAD/EMTDC using the parameter of table 1. All variables are changed to per unit, and the voltage in table is mean peak value of phase voltage. The voltage ration of main transformer(TM in fig.1) is 22900/220[V] and /Y connected. The winding ration of series and parallel transformer(TS, TP in fig.1) is 1 : 1 and

the primary of series transformer is connected. The switching element is used IGBT(Insulated Gate Bipolar Transistor) and PWM(Pulse Width Modulation) technique is used triangular wave comparison method.

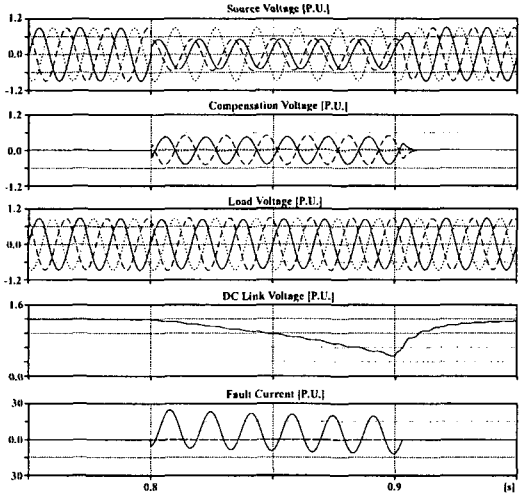


Fig. 4. VSC in SLGF

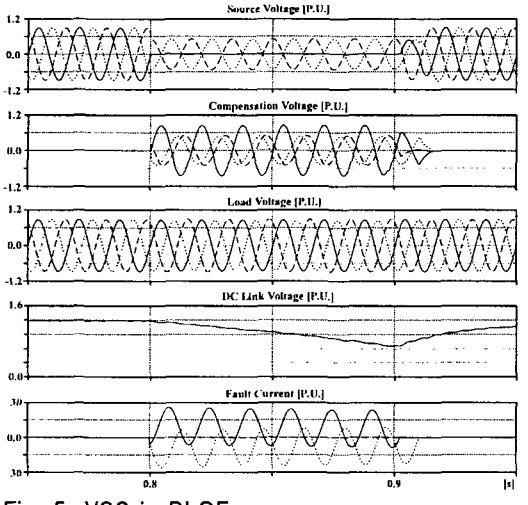


Fig. 5. VSC in DLGF

The fig. 4, 5, and 6 are simulated results for VSC's operation under SLGF, DLGF, and TLGF condition respectively. All of the figures show main transformer secondary voltage, compensation voltage, load voltage, DC link voltage, and fault current from top. The fault is sustained for 300 milisecond. The fault resistance and capacitance for fault conditions is shown in table 2. The simulated results show that proposed VSC has a good dynamic performance and capacitance is well designed by (5).

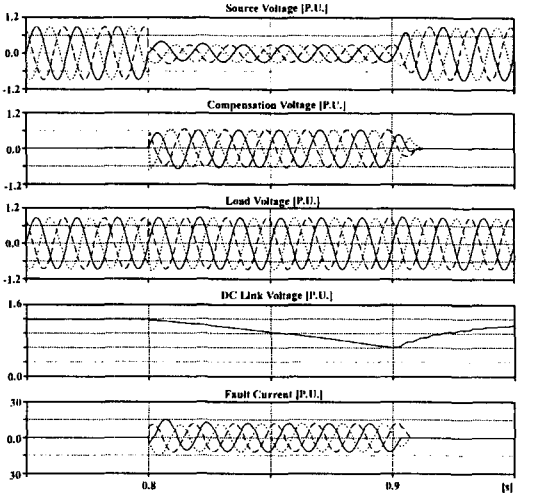


Fig. 6. VSC in TLGF

The fig. 7 is simulated result for temporary outage. The outage duration time is 100 milisecond and 20[mF] of capacitor is used. From fig. 7, we can know that the proposed VSC system is able to compensate temporary outage.

Table 1. Simulation parameters

parameter	value	parameter	value
Power rating	10[KVA]	Switching frequency	5[kHz]
Voltage	311[Vpeak]	Impedance	8.4[Ω]
Current	37.1[Apeak]	DC Link Voltage	514[V]
Frequency	60[Hz]	LPF cutoff frequency	100[Hz]

Table 2. Fault resistance and DC capacitance

Parameters	SLGF	DLGF	TLGF
Resistance	0.005[Ω]	0.005[Ω]	1.5[Ω]
Capacitance	5.9[mF]	53[mF]	5.9[mF]

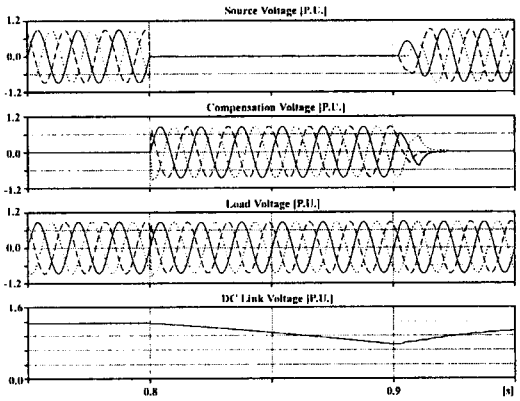


Fig. 7. VSC in temporary outage

7. CONCLUSION

This paper has presented power quality enhancement through compensation using VSC for instantaneous voltage sag caused by faults in distribution line. The simple detection algorithm which is implemented in synchronous reference frame, has a fast detection time. The robust characteristic against the noise is available by inserting the LPF. Also the relationship between the detection time and the cut-off frequency is induced in a numerical formula. The DC capacitor is designed from point of view the input/output energy as the output power rating and the amplitude and duration time of the faults. The simulated results is shown that the proposed scheme has a good performance and protects to sensitive load for temporary outage.

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