Electrical Characteristics of CMOS Circuit Due to Channel Region Parameters in LDMOSFET

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The electrical characteristics of CMOS inverter with LDMOSFET are studied for high power and digital circuit application by using two dimensional MEDICI simulator. The simulation is done in terms of voltage transfer characteristic and on-off switching properties of CMOS inverter with variation of channel length and channel doping levels. The channel which surrounds a junction-type source in LDMOSFET is considered to be an important parameter to decide a circuit operation of CMOS inverter. The digital logic levels of input voltage show to increase with increase of n-channel length and doping levels while the logic output levels show to the almost constant.

Keywords : CMOS inverter, LDMOSFET, Channel, Transfer characteristics

1. INTRODUCTION

LDMOS is very easy to integrate into a CMOS or a BiCMOS process which facilitates the fabrication of control, logic circuit and power switches on a single chip[1,2]. The basic operation of LDMOSFET(lateral double-diffused MOSFET) is the same as that of any MOSFET. However, the drain-source blocking voltage may be in the range of 100 voltages and the current driving capability of this device is usually high. Advantages of LDMOSFET are that it requires only a small input current[3,4] and the high switching speed can be controlled with very small gate current, so that LDMOSFET finds increasing applications in low-power high-frequency IC.

Conventional CMOS inverter is the most popular digital logic circuit because of wide power supply range and high speed[5-7]. The inverter logic circuits have been available as standard packages for use in conventional digital system design since 1970's. Recently, a new type of CMOS inverter is suggested for a diverse power application and a large output voltage swing in digital driver IC.

We studied LDMOSFET pair in CMOS inverter for a high power application and fast speed. Compared to a typical CMOS inverter, LDMOSFET complementary inverter is considered to have a high voltage allowance due to the p/n junction-type source. The junction-type source in LDMOSFET can control the channel parameters to provide a high voltage swing in digital logic.

Electrical characteristics of a LDMOSFET CMOS inverter were studied in terms of voltage transfer characteristics, on-off switching properties with variation of channel length and impurity concentration. The cross section of LDMOSFET device is shown in Fig. 1, where LDMOSFET has a typical structure which is composed of drift region and main channel enclosing source region.

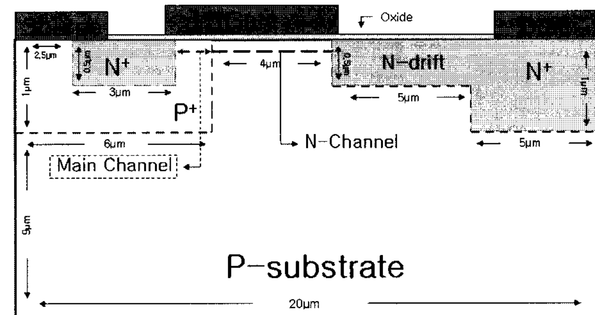

Fig. 1. Cross section of LDMOSFET.

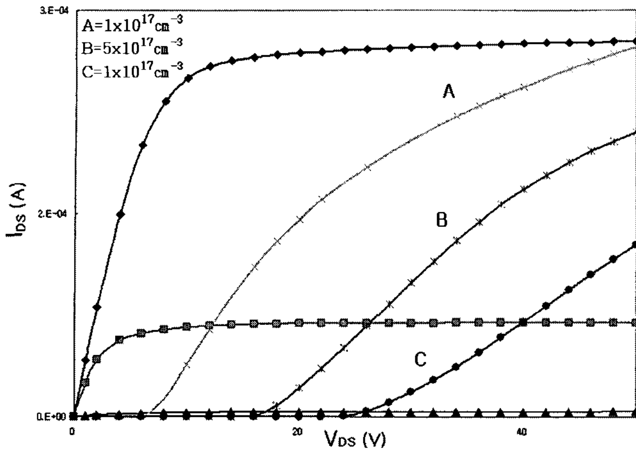

Fig. 2. Characteristics of I_D vs.V_{DS} and I_D vs.V_{GS} with variation of n-channel doping levels.

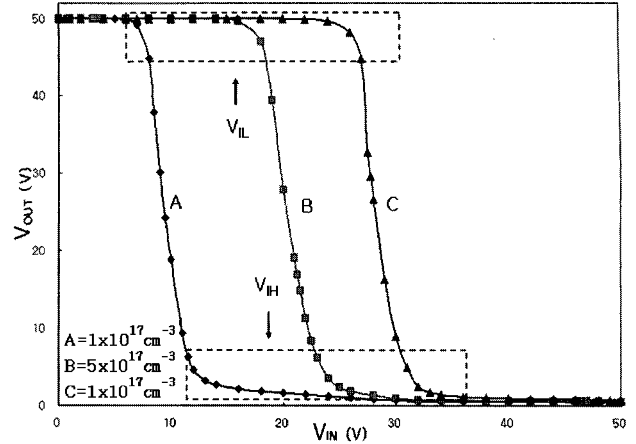

Fig. 3. Voltage transfer characteristic of CMOS inverter with variation of n-channel doping levels.

2. RESULTS

Figure 2 shows the characteristics of drain current versus gate and drain voltages. From the graph of current versus drain voltage at V_{GS}=25 V, trans-conductance in saturation region are almost constant for the 3 cases of channel length, while threshold voltages from the graph of current versus gate voltage at V_{DS}=1 V show to increase with higher n-channel doping levels.

The channel doping level of LDMOSFET is an important parameter to decide the threshold voltage and drain current of MOFET. Electrical characteristic of CMOS inverter is studied with variation of channel doping levels. Figure 3 shows the voltage transfer characteristic with variation of n-channel doping levels. Each transfer characteristic has five distinct segments corresponding to the different modes operation of n-channel LDMOSFET. The first segment of transfer characteristics is obtained when p-LDMOSFET is in triode region and n-LDMOSFET is in saturation, while the last segment is in an opposite operating region. We consider the two cases of logic input voltages, low input voltage V_{IL} when input voltage V_I is at logic-0 level, and high input voltage V_{IH} when input voltage V_I is at logic-1 level. The low input voltage V_{IL} and high input voltage V_{IH} in Fig. 3 depend on threshold voltage. The linear region in transfer characteristics in Fig. 3 show almost same slope of graph with variation of n-channel and p-channel doping levels. The slope depends on trans-conductance of channel which is almost same with variation of channel doping levels as shown in the saturation region of Fig. 2. With increase of n-channel doping levels, V_{IL} and V_{IH} are shown to increase. The result comes from the dependency of threshold voltage and conductance of LDMOSFET on channel doping levels. The high and low digital output logic levels are

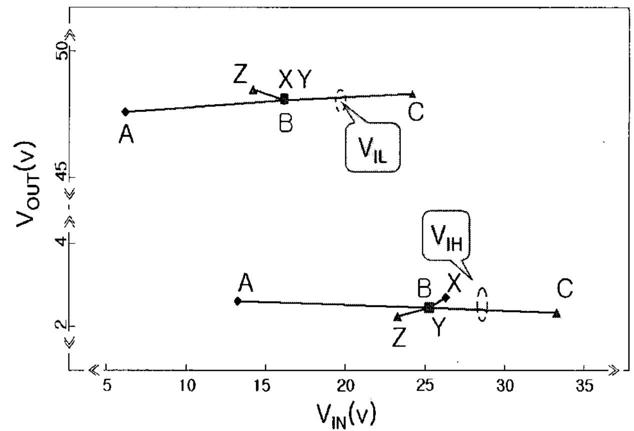

Fig. 4. High and low logic levels of input voltage with variation of n-channel doping levels(A,B,C) and p-channel doping levels(X,Y,Z).

almost in the output voltage where the input voltages V_{IL} and V_{IH} locate. The logic output voltages don't show a strong dependency on channel doping levels as much as the input voltages of V_{IL} and V_{IH} do.

The input logic levels V_{IL} and V_{IH} with variation of channel doping levels are shown in Fig. 4 where A, B, and C are in the 3 different n-channel doping levels of 1x10^{17} cm^{-3}, 5x10^{17} cm^{-3}, 1x10^{18} cm^{-3} respectively. The effect of p-channel doping levels is also shown in Fig. 4 where X, Y, Z are in doping levels of 1x10^{17} cm^{-3}, 5x10^{17} cm^{-3}, 1x10^{18} cm^{-3} respectively at the channel length of 0.5 μm. With increase of n-channel doping level, threshold voltage and channel conductance of n-MOSFET increase. It makes the transfer characteristic change and results in the increase of V_{IL} and V_{IH}. However, the increase of p-channel doping levels shows to decrease of V_{IL} and V_{IH}.

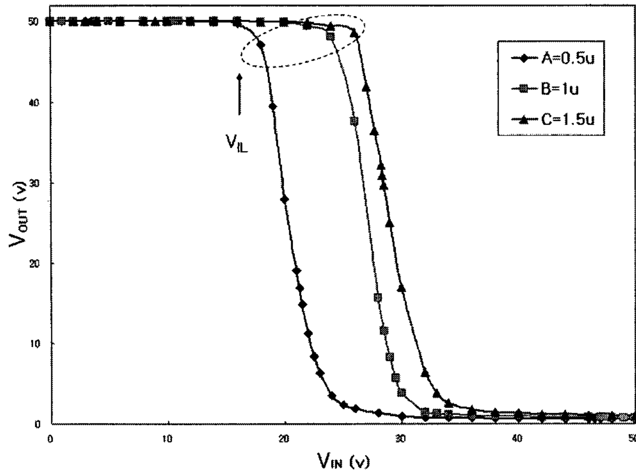

Fig. 5. Voltage transfer characteristic of CMOS inverter with variation of n-channel length.

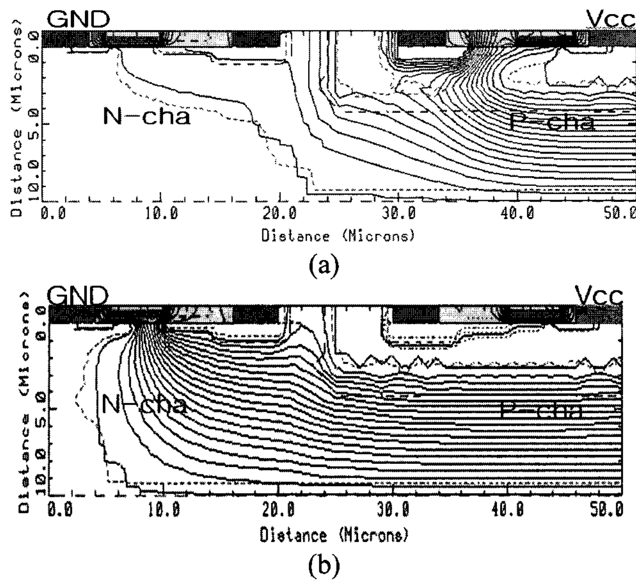

Fig. 6. (a) Cross-sectional view of equipotential lines at 0.5 μm channel length with Vg=25 V. (b) Cross-sectional view of equipotential lines at 1.5 μm channel length with Vg=25 V.

Figure 5 shows the voltage transfer characteristic with variation of n-channel length. It shows that the digital input logic levels V_{IL} and V_{IH} increase with increase of channel length. With increase of channel length, the main channel with higher doping level controls the threshold voltage to increase. The effect of channel length on the transfer characteristic of CMOS inverter indicates almost the same effect with doping levels as shown in Fig. 2.

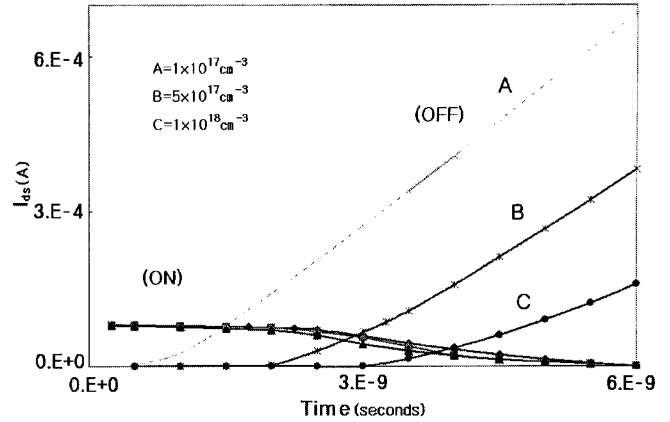

Fig. 7. On-off transient characteristics of drain current with variation of n-channel doping levels.

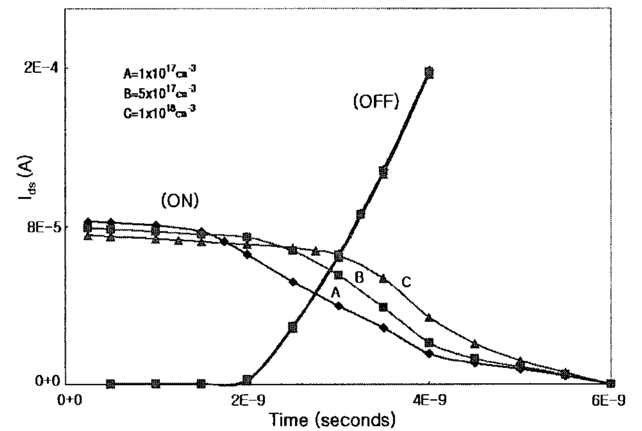

Fig. 8. On-off transient characteristics of drain current with variation of p-channel doping levels.

The effect of n-channel length on the output logic levels can be seen in the equipotential lines at about 25 V gate voltage as shown in Fig. 6. In Fig. 5, low output voltage is obtained in A channel length(0.5 μm) at the input voltage of 25 V, while, at the same input voltage, high output voltage is shown in C channel length(1.5 μm)

Figure 6(a) which is in 0.5 μm channel length indicates that p-channel LDMOSFET is in higher potential compared to n-channel one. Output current is considered to flow between n-channel MOS and GND. Consequently, output voltage is at logic-0 level. On the other hand, opposite case is shown in the second structure which is in 1.5 μm channel length and output voltage is at logic-1 level. In the case of Fig. 6(b), the n-channel device is turned off, the p-channel device is on, so there is dc path from Vg to V_{CC}. In both cases of Fig. 6, the edge of drift region is in a high potential and the

junction type source is in a low potential region. It shows, even in same voltage application, the channel length can change the output logic level.

The characteristics of a transient current at the moment of high(on) and low(off) output with variation of n-channel doping levels shown in Fig. 7, where the current is defined to flow from p-channel to n-channel LDMOSFET. The off characteristic shows that the transient current increases with increase of time and the slope(current vs. time) decreases with increase of n-channel doping levels while the on characteristic shows no dependency on the n-channel doping levels. The slope in the off transient characteristics depends on the channel conductance. The conductance is proportional to a carrier mobility which decreases with increase of impurity concentration.

The transient characteristics with variation of p-channel doping levels is shown in Fig. 8, which shows the opposite result compared to Fig. 7. Although the off decay times are independent of p-channel doping levels, the on characteristic indicates the shorter time decay with higher channel doping levels. The transient characteristics can be summarized that n-channel doping levels affect mostly on the off characteristic and p-channel doping levels affect on the on characteristic, which means driver device(load device) affects on the off(on) transient time.

3. CONCLUSION

Electrical characteristics of LDMOSFET CMOS inverter are investigated with variation of channel region parameters. The transfer characteristics of CMOS inverter and the switching operation show a strong dependency on the channel length and doping levels. The digital logic levels of input voltage increase with increase of n-channel length and doping levels and with decrease of p-channel doping levels, while those of output voltage show no dependency. The on and off transient characteristics show that the on characteristic depends mostly on the p-channel doping levels.

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