A 1.2-V Wide-Band SC Filter for Wireless Communication Transceivers

Huikwan Yang, Sanghyun Cha, Seungyun Lee, Sangheon Lee, Jinup Lim, and Joongho Choi

Abstract—**This paper presents the design of a low-voltage wide-band switched-capacitor (SC) filter for wireless communication receiver applications. The filter is the 5th-order Elliptic lowpass filter. With the clock frequency of 50MHz implying that an effective sampling frequency is 100MHz with double sampling scheme, the cut-off frequency of the filter is programmable to be 1.25MHz, 2.5MHz, 5MHz and 10MHz. For low-power systems powered by a single-cell battery, the SC filter was elaborately designed to operate at 1.2V power supply. Simulation result shows that the 3rd-order input intercept point (IIP3) can be up to 27dBm. The filter was fabricated in a 0.25-μm 1P5M standard CMOS technology and measured frequency responses show good agreement with the simulation ones. The current consumption is 34mA at a 1.2V power supply.**

Index Terms—**Switched-capacitor (SC) filters, Wireless Communication, Low-voltage, Double-sampling.**

I. INTRODUCTION

The wireless telecommunication becomes the major trend for data transmission as well as the conventional voice signal. As demands for larger amount of data transfer have been continuously increased, a wireless communication technology has been developed in order to satisfy data-rate requirements higher than Mb/s these days [1,2]. In addition to improvements in the areas of wireless communication and digital signal processing technologies, the advent of VLSI technology makes it possible to implement the transceiver system with a SoC (System-on-Chip) methodology and correspondingly RF front-end, base-band analog front-end, and digital MODEM can be combined into a single chip [3,4]. Fig. 1 shows the block diagram of wireless communication receiver system. The filter blocks of the receiver path are placed between the RF/IF down conversion mixer block and analog-to-digital converter of the base-band analog front-end module [5]. The main operation of the filter block is to filter out the undesired channel signals of interferences and aliasing components. The bandwidth of the channel-selection filter has been continuously increased in order to achieve the data-rate higher than Mb/s. Because of the high bandwidth required for channel-selection filters, several design constraints should be properly considered in terms of the architect-ture and implementation methodology issues.

The Gm-C filter topology can be chosen for high-frequency filtering operations thanks to the open-loop configuration of included transconductance amplifiers. However it is hard to meet large dynamic range performance due to poor linearity characteristics. On the other hand, the active-RC filter has high linearity performance and can be efficiently used in high-frequency operations. But in this type of filter the operational amplifier might drive the heavy resistive load resulting in the increased power dissipation. The SC filters achieve high linearity performance with the

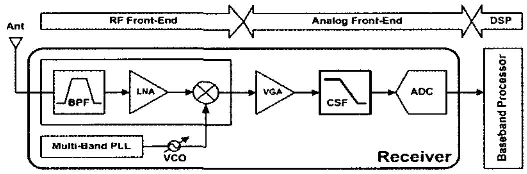

Fig. 1. Wireless communication receiver.

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negative feedback configuration. The frequency characteristics can be precisely determined and kept to be constant in spite of several variations of the operating environment.

The design of analog circuit operating under low supply voltage becomes more and more important which will reduce power dissipation and increase the battery life-time for mobile applications. Many works have been recently performed on techniques for implementing low-voltage switched-capacitor circuit with a low power supply [6-9]. In this paper, a low voltage double sampling 5^{th}-order Elliptic lowpass SC filter is presented for wireless communication receiver applications. Low-voltage operational amplifier and switched-capacitor integrator are designed for the filter that uses a single-cell battery as power supply. The filter is fabricated in a 0.25-μm standard CMOS technology and operated at 1.2V supply voltage.

II. Filter Structure

The designed filter is the 5^{th}-order Elliptic lowpass filter which is obtained from RLC ladder prototype as in Fig.2. Because of the multi-feedback path, this configuration of the filter maintains regular frequency response in spite of variations of components rather than a cascaded topology. The frequency response of the filter is determined so that a cut-off frequency up to 10MHz is obtained with a -6dB passband gain and a stop-band attenuation higher than -40dB at the frequency of 1.7 times the cut-off bandwidth. The clock frequency is set to 50MHz which implies that the effective sampling frequency is 100MHz with a double sampling scheme described later in detail. A frequency divider control is used to program the cut-off frequency so that 5MHz, 2.5MHz and 1.25MHz are available in addition to 10MHz.

The block diagram of the designed 5^{th}-order Elliptic

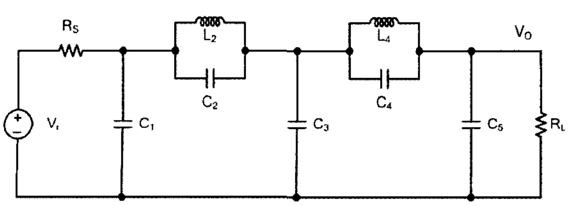


Fig. 2. Lowpass filter RLC ladder prototype.

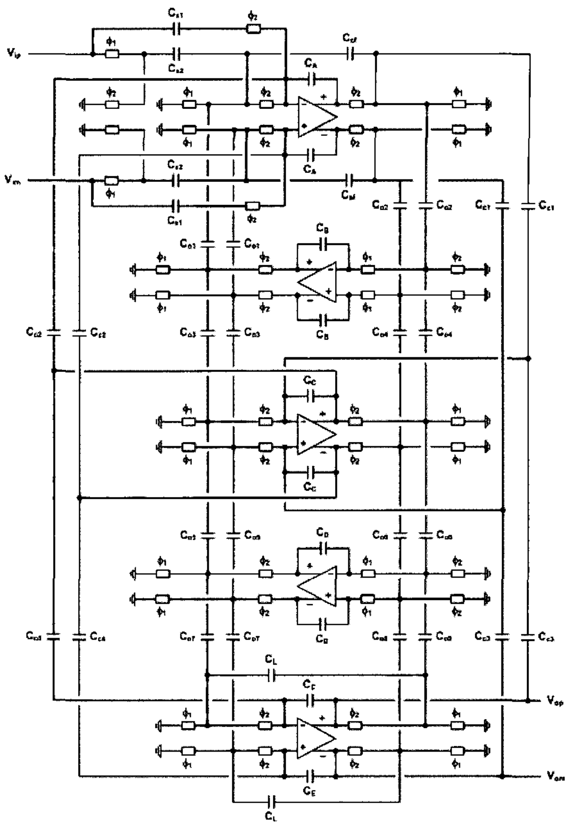


Fig. 3. Block diagram of the filter.

lowpass switched-capacitor filter is shown in Fig.3. In actual implementation, the input switched-capacitor circuits are doubled with opposite clocks in order to incorporate the double sampling scheme. The bilinear frequency transformation from s- to z-domain is used to achieve the accurate frequency response. All branch gain values and corresponding capacitor values are scaled so that maximum operating range can be obtained. To reduce the common mode noise and to increase the linearity characteristics at a low supply voltage, the filter is realized in a fully differential signal scheme.

III. Circuit Design

1. Low-voltage SC integrator

The switched-capacitor (SC) circuit is the most appropriate approach for high quality analog signal processing with low power supply. But with the supply voltage less than 2V, the switch-on condition cannot be guaranteed for acceptable signal ranges. In order to overcome this drawback, several solutions were proposed.

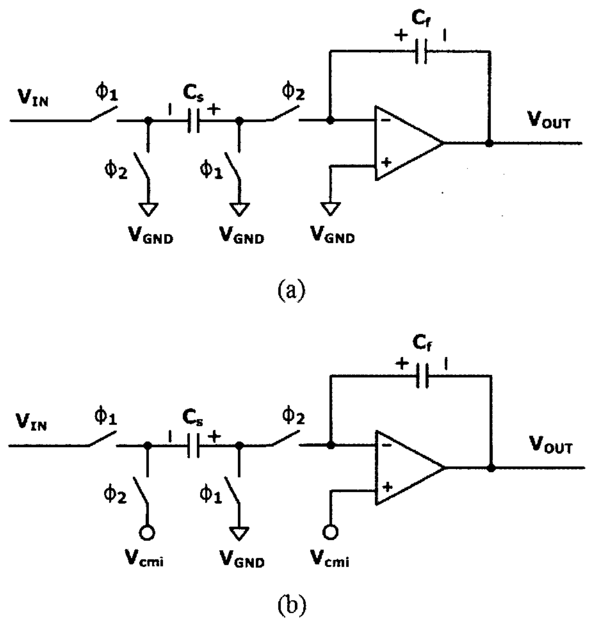


Fig. 4. Switched-capacitor integrator.
(a) Conventional integrator. (b) Low-voltage integrator.

One solution is to using a switched-op amp configuration [5]. Another solution is to use the clock boot-strap scheme which increases the clock driving signal magnitude [6].

A conventional schematic of a SC integrator is shown in Fig. 4(a). Here, input and output common-mode bias levels are identical to be V_{GND} (about $V_{DD}/2$). This makes it difficult to be included in low-voltage power-supply circuits because neither PMOS nor NMOS differential pair can function correctly when included in the operational amplifier as the input stage. To overcome this problem, a modified version of SC integrator was proposed in [8-9]. The schematic of the improved SC integrator is shown in Fig. 4(b).

When ϕ_1 is on, the input signal is sampled through C_S with respect to the common-mode level of V_{GND}. When the charge stored on C_S is transferred to C_F for integration during ϕ_2, the common-mode levels of both sides of C_S are changed to V_{cmi}. This value is also used for determining the common-mode input level of the used operational amplifier. The value is chosen so that the input differential pair can work correctly. In our design, it is set to be 0.3V for PMOS differential pair operating under 1.2V supply voltage. The output common-mode level of the operational amplifier is V_{GND} so that the sampling of the next stage can be performed with the identical common-mode level of V_{GND}.

2. Double-Sampling SC integrator

Examination of circuit operations in the SC integrator of Fig. 4 reveals that during ϕ_1 of sampling phase, the operational amplifier in the integrator is idle. Full utilization of this amplifier can be achieved by using double sampling scheme described in [10]. The schematic of a double-sampling SC integrator is show in Fig. 5. Here two sampling branches consisting of C_{S1} and C_{S2} are used. During the clock phase of ϕ_1, V_{IN} is sampled onto the sampling capacitor C_{S1}, while C_{S2} is transferring the charge to C_{FB}. During ϕ_2, the situation is reversed. Using this double-sampling scheme, the effective sampling clock frequency can be doubled compared to a single sampling scheme. With the double-sampling SC integrator, the extra area is required due to the additional sampling capacitor and four relevant switches. The issue of mismatch problem between C_{S1} and C_{S2} must also be considered carefully.

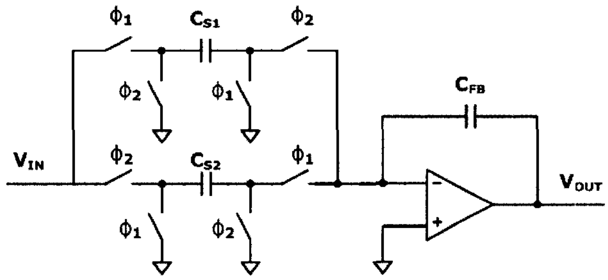


Fig. 5. Double-sampling SC integrator.

3. Operational Amplifier

In the SC filter, the sampling frequency should be quite larger than the input signal bandwidth. This requires operational amplifiers that should operate at a high sampling rate, which implies that large power dissipation of the filter cannot be avoided. Fig. 6 shows the circuit schematic of the operational amplifier used in the filter. It is a 2-stage Miller-compensation operational amplifier whose input stage consists of the folded configuration. Fig. 7 shows the open-loop frequency response of the operational amplifier. The open-loop DC gain and unity-gain frequency of the amplifier are 64dB and 320MHz, respectively for a load capacitance of 2pF. The current dissipation of each amplifier is 5.5mA. The common-mode feedback (CMFB) circuit is implemented

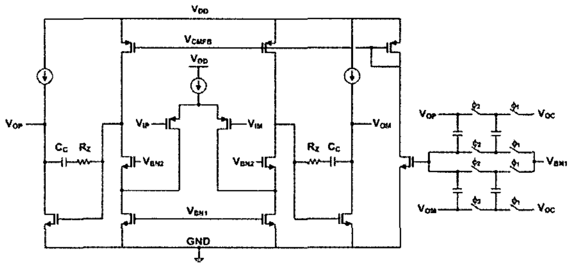


Fig. 6. Schematic of the operational amplifier.

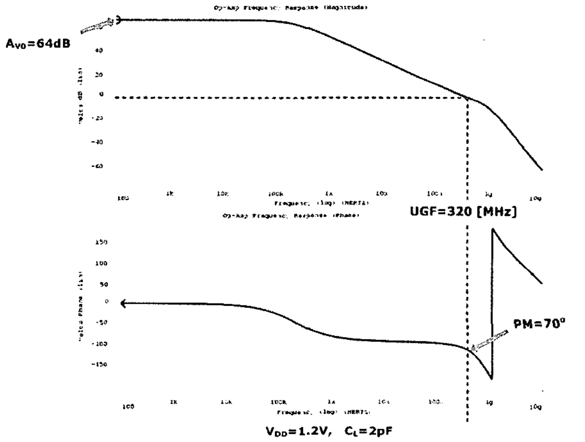
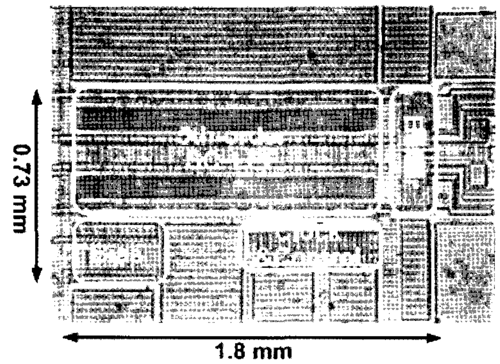


Fig. 7. Frequency response of operational amplifier.

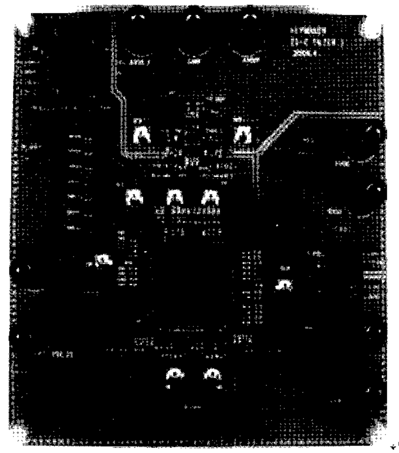
with a SC circuit in order to achieve larger operating range of the output swings and reduce power dissipation.

IV. IMPLEMENTATION

The filter is designed and fabricated in a 0.25-μm 1-poly 5-metal standard CMOS technology. A chip microphotograph and test PCB are shown in Fig. 8, where the bias circuit, clock and control circuit and output buffer are also shown. The active area of the filter is 0.73 x 1.8 mm^2. Fig. 9 shows simulation results of the frequency magnitude response. Fig. 10 shows the measured frequency characteristics of the filter. The cut-off frequencies of the filter can be controlled to be 1.25MHz, 2.5MHz, 5MHz, and 10MHz using the 2-bit digital control signal. The stop-band attenuation around 1.7 times of the cut-off frequency is shown to be larger than 40dB satisfying the required specifications. Measured results of the designed filter are summarized in Table 1. The power dissipation of the filter is 14.4mW when cut-off frequency is set to be 1.25MHz, 2.5MHz, 5MHz, while more power dissipation is unavoidable when the cut-off frequency is set to be 10MHz cut-off condition in order to guarantee the wide bandwidth operation of the op-amp. Our research work is compared with other previously published results in terms of the figure-of-merit (FOM) for the case of 5MHz cut-off frequency operation. The compared results are shown in Fig. 11.



(a)



(b)

Fig. 8. Hardware implementation.
(a) Chip microphotograph (b) Test PCB

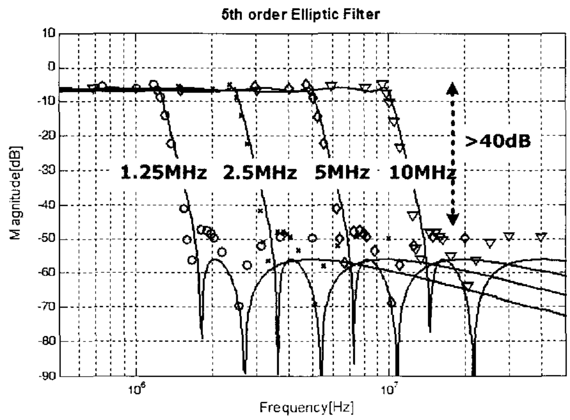


Fig. 9. Simulation results of the frequency response.

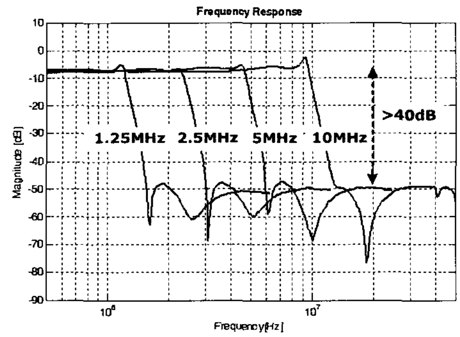


Fig. 10. Measurement results of the frequency response.

Table. 1. Performance summary of the filter.

Specifications		Results
Filter Type		5^{th}-order Elliptic LPF
Cutoff Frequency		1.25/ 2/ 5/ 10MHz
Sampling Frequency		100MS/s (f_{CLK}=50MHz)
Pass-band Gain		-6dB
Stop-band Attenuation		> 40dB
Linearity(In-band IIP3)		27dBm
Power dissipation	f_C =10MHz	39mW @ 1.2V Supply
	f_C=1.25/2.5/ 5MHz	14.4mW @ 1.2V Supply
Area		0.73 × 1.8 mm^2
Technology		0.25-μm 1P5M CMOS

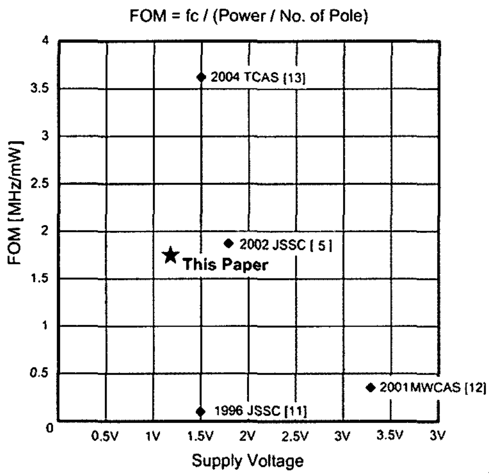


Fig. 11. Comparison of figure-of-merit.

V. CONCLUSIONS

The low-voltage wide-band SC filter is implemented for wireless communication receiver applications. The 5^{th}-order Elliptic lowpass filter is suitable for performing the proper channel selection operations. For the filter operated at low-supply voltage, a low-voltage switched-capacitor integrator is adopted as well as the low-voltage operational amplifier. Double-sampling scheme is incorporated in order to double the sampling clock frequency with the same power consumption. The filter is fabricated in a 0.25-μm 1P5M standard CMOS technology and runs at a supply voltage of 1.2V.

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REFERENCES

[1] A. Parssinen, J. Jussila, A.I. Halonen, “A 2-GHz wide-band direct conversion receiver for WCDMA applications,” *IEEE Journal of Solid-State Circuits*, pp. 1893-1903, Dec. 1999.

[2] A. A. Abidi, “Direct-conversion radio transceiver for digital communications,” *IEEE Journal of Solid-State Circuits*, pp. 1399-1410, Dec. 1995.

[3] J. Crols, M. S. J. Steyaert, “A Single-chip 900MHz CMOS receiver front-end with high performance low-IF topology,” *IEEE Journal of Solid-State Circuits*, pp. 1483-1492, Dec. 1995.

[4] R. Gharpurey, et al., “A direct conversion receiver for 3G WCDMA standard,” *IEEE Proc. CICC*, pp. 239-242, May. 2002.

[5] S. Azuma, et al., “Embedded anti-aliasing switched-capacitor ladder filter with variable gain and offset compensation,” *IEEE Journal of Solid-State Circuits*, Vol.37, No.3, pp.349-356, Mar. 2002.

[6] Steyaert, J. Crols, “Switched-Opamp: An Approach to Realize Full CMOS Switched-Capacitor Circuits at Very Low Power Supply Voltages,” *IEEE Journal of Solid-State Circuits*, Vol.29, No.8, pp. 936-942, Aug. 1994.

[7] Chung-Yu Wu, Wei-Shinn Wey, Tsai-Chung Yu, “A 1.5V CMOS Balanced Differential Switched-Capacitor Filter with Internal Clock Booster” *IEEE Proc. ISCAS*, pp. 1025-1028, Seattle, May 1995.

[8] P. Filoramo, G. Giustolisi, G. Palmisano, G. Palumbo "Approach to the design of low-voltage SC filters," *IEEE Proc. Circuits Devices syst.*, vol. 147, No. 3, pp. 196-200, June 2000.

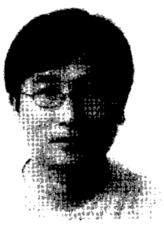
[9] W. Aloisi, G. Giustolisi, G. Palumbo, "Design of low-voltage low-power SC filters for high-frequency applications," *IEEE Proc. ISCAS*, pp. 605-608, May 2003.

[10] Mikko Waltari and Kari Halonen, "A 10-Bit 220-Msamples/s CMOS Sample-and-Hold Circuit", *IEEE Proc. ISCAS*, pp. 253-256, 1998.

[11] G. Nicollini, A. Nagari, P. Confalonieri & C. Crippa, "A -80dB THD 4Vpp switched capacitor filter for 1.5V battery-operated systems," *IEEE Journal of Solid-State Circuits*, vol. 31, No. 8, pp. 1214-1219, Aug. 1996.

[12] B. Manai & P. Loumeau, "A wide-band CMOS switched capacitor filter for UMTS direct conversion receiver," *IEEE MWSCAS,* pp. 377-380, Aug. 2001.

[13] W. Aloisi, G. Giustolisi & G. Palumbo, "Exploiting the high-frequency performance of low-voltage low-power SC filters," *IEEE Trans. CAS-II*, vol. 51, No. 2, pp. 77-84, Feb. 2004.



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