A 10-GHz CMOS *LC* VCO with Wide Tuning Range Using Capacitive Degeneration

Tae-Geun Yu, Seong-Ik Cho, and Hang-Geun Jeong

Abstract—**In order to widen the tuning range, capacitive degeneration is applied to fully CMOS LC VCOs. Small signal analysis shows that the fixed MOSFET capacitance seen by the LC tank is smaller than that of the traditional LC VCO, resulting in significant extension in the tuning range. This improvement in the tuning range has been verified through measurement of a 10-GHz LC VCO fabricated by 0.18㎛ CMOS process. The measured tuning range is from 9.8-GHz to 12-GHz, which is better than those of the reported CMOS LC VCOs in 10-GHz band. The measured phase noise is -103dBc/Hz at 1MHz offset.**

Index Terms—**capacitive degeneration, parasitic capacitance, tuning range, voltage-controlled oscillator(VCO).**

I. INTRODUCTION

For bipolar or BiCMOS technologies, capacitive degeneration has recently been applied, yielding a very high oscillating frequency and wide tuning range[1]-[3]. But the new topology has not yet been applied to CMOS technology. Fully CMOS *LC* oscillators are advantageous for single-chip wireless transceivers. The conventional CMOS *LC* VCOs using cross-coupled differential pairs have narrow tuning ranges due to the relatively larger portion of the fixed capacitance of MOSFET. For example, in the np core complementary cross-coupled topology, the oscillation node is connected to the gate and drain terminals of the four MOS transistors. The output buffer is also connected to the oscillation node. This structure increases the fixed parasitic capacitance at the oscillation node and results in the reduction in the relative portion of the variable capacitance. To solve this problem, capacitive degeneration can be applied to CMOS *LC* VCOs, where the tuning range can be extended because in this topology the *LC*-tank is loaded only by the gates of the MOS transistor. Through small signal analysis, it is proven that the equivalent capacitance due to MOSFET capacitances in the proposed structure can be decreased in comparison to that of the conventional *LC* VCO structure using a cross coupled pair. The proposed *LC* VCO yielded a measured tuning range of 20% in 10-GHz band, which is a significant improvement over comparable CMOS VCOs [4]-[7].

Manuscript received Sep 9, 2006; revised Nov. 10, 2006.
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II. SMALL SIGNAL ANALYSIS OF THE PROPOSED *LC* VCO

Fig. 1 shows a simplified circuit model for a parallel *LC* oscillator, where G_p represents the tank loss, G_{eq} is the effective negative conductance generated by the active devices, and C_{eq} is the effective shunt capacitance contributed by the active devices. $|G_{eq}|$ must be larger than G_p in order to ensure the oscillation. To obtain a wide tuning range, C_{eq} must be made as small as possible and C_{var} should be increased. Our proposed *LC* VCO topology using capacitive degeneration is based on this concept.

The traditional negative conductance cell using a cross coupled pair and its small signal equivalent model are shown in Fig. 2, where g_m, r_o, and C_{gs} are transconductance, output resistance, parasitic capacitance

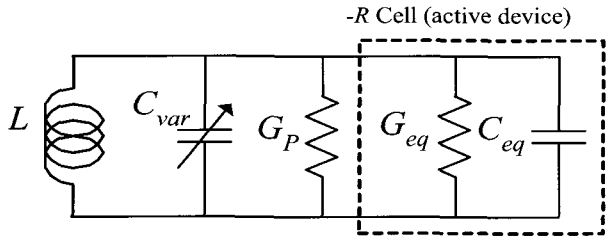

Fig. 1. Parallel *LC* VCO model.

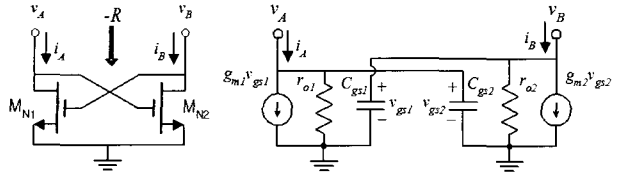

Fig. 2. Traditional negative conductance cell using a cross coupled pair and its small signal equivalent circuit model.

between gate and source, respectively, of the MOSFET.

When the transistor sizes of M_{N1} and M_{N2} are the same, $g_{m1} = g_{m2} \equiv g_m$, $r_{o1} = r_{o2} \equiv r_o$, and $C_{gs1} = C_{gs2} \equiv C_{gs}$ in Fig. 2. The admittance between drain terminals of M_{N1} and M_{N2} is given by Eq. (1). Because $1/r_o$ has a much smaller value than g_m, G_{eq} and C_{eq} are approximately $-g_m/2$ and $C_{gs}/2$, respectively.

$$\begin{aligned} Y &= \frac{i_A - i_B}{2(V_A - V_B)} \\ &= \frac{g_{m1}V_{gs1} + V_{gs2}sC_{gs2} + V_{gs2}/r_{o1} - (g_{m2}V_{gs2} + V_{gs1}sC_{gs1} + V_{gs1}/r_{o2})}{2(V_{gs2} - V_{gs1})} \\ &= (-g_m + sC_{gs} + 1/r_o)/2 \end{aligned} \quad (1)$$

The proposed *LC* VCO is shown in Fig. 3. M_1 and M_2 provide a negative conductance to the *LC* tank using capacitive degeneration, which are differentially implemented by M_3 and M_4.

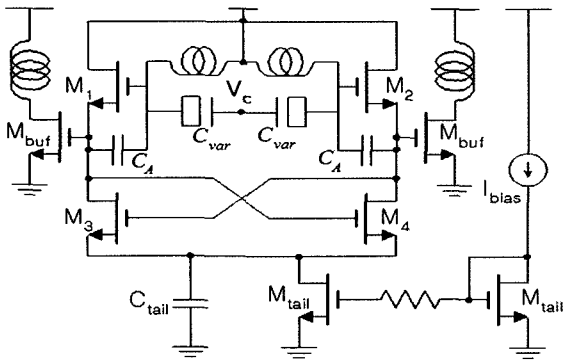

Fig. 3. The proposed *LC* VCO schematic using capacitive degeneration.

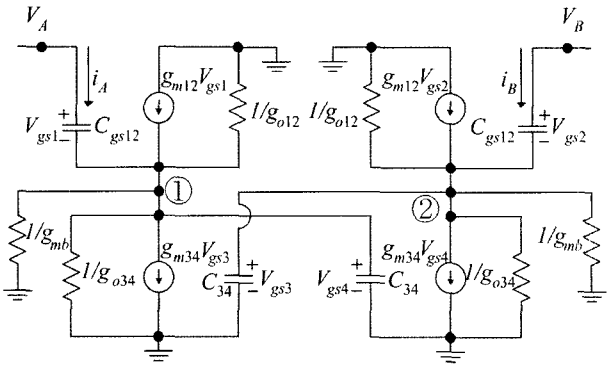

Fig. 4. The small signal equivalent circuit for the proposed *LC* VCO.

Fig. 4 shows the small signal equivalent circuit for the proposed *LC* VCO. In this Fig., g_{m12} and g_{m34} are transconductances of M_1, M_2 and M_3, M_4, respectively. The admittance between the two terminals of *LC*-tank can be expressed as in Eq. (2).

$$Y = \frac{i_A - i_B}{2(V_A - V_B)} = \frac{sC_{gs12}(V_{gs1} - V_{gs2})}{2((V_{gs1} - V_{gs2}) - (V_{gs3} - V_{gs4}))} \quad (2)$$

Using Kirchhoff's current laws at the nodes of ① and ②, Eqs. (3) and (4) are obtained.

$$V_{gs1}(sC_{gs12} + g_{m12}) - g_{m34}V_{gs3} - V_{gs4}(sC_{34} + g_{mb} + g_{o12} + g_{o34}) = 0 \quad (3)$$

$$V_{gs2}(sC_{gs12} + g_{m12}) - g_{m34}V_{gs4} - V_{gs3}(sC_{34} + g_{mb} + g_{o12} + g_{o34}) = 0 \quad (4)$$

Subtracting Eq. (3) from Eq. (4), and then substituting for V_{gs1}-V_{gs2} in Eq. (2), Eq. (5) can be derived.

$$\begin{aligned} Y &= \frac{s^2C_{gs12}C_{34} + sC_{gs12}(g_{mb} + g_{o12} + g_{o34} - g_{m34})}{2\{(g_{mb} + g_{o12} + g_{o34} + g_{m12} - g_{m34}) + s(C_{gs12} + C_{34})\}} \\ C_{34} &(= C_{gs34} + C_{12sb} + C_{db34} + C_{dg34} + C_{load}) \end{aligned} \quad (5)$$

In the denominator of Eq. (5), by making real part much smaller than imaginary part, we can obtain Eqs. (6) and (7). In addition, g_{mb} was made zero by tying the bodies to the sources of the corresponding transistors, which is allowed in the triple well CMOS process.

$$G_{eq} = \frac{C_{gs12}(-g_{m34} + g_{o12} + g_{o34})}{2(C_{gs12} + C_{34})} \quad (6)$$

$$C_{eq} = \frac{C_{gs12}C_{34}}{2(C_{gs12}+C_{gs34})} \quad (7)$$

Table 1. Comparison for G_{eq} and C_{eq}.

	Traditional LC VCO using NMOS latch	The proposed LC VCO
G_{eq}	$-\frac{g_m}{2}$	$-\frac{C_{gs12}g_{m12}}{2(C_{gs12}+C_{34})}$
C_{eq}	$\frac{C_{gs}}{2}$	$\frac{C_{gs12}C_{34}}{2(C_{gs12}+C_{34})}$

Table 2. Ratio of MOS parasitic capacitance in the proposed tuned LC VCO.

L [nH]	C_{gs12} [fF]	$C_{total\ parasitic\ capacitance}$			C_{MOS} [%]
		C_{ind} [fF]	C_{MOS} [fF]	C_{Load} [fF]	
0.51	140	60	82	20	51
	240	60	108	20	57
	340	60	136	20	63

Table 1 shows the comparison for G_{eq} and C_{eq} between the traditional LC VCO using a cross coupled pair and the proposed LC VCO. The C_{eq} of the proposed LC VCO is smaller than that of the traditional LC VCO, and this enables a wide tuning range. But, because the C_{34} capacitance of the proposed LC VCO is larger than C_{12} capacitance, $|G_{eq}|$ of the proposed LC VCO is smaller than that of the traditional LC VCO, which is a disadvantage of the proposed scheme. This drawback can be overcome by inserting a capacitor (C_A) between the gate and the source of M_1, M_2 as shown in Fig.3.

Table 2 shows the ratio of MOS parasitic capacitance to the total capacitance in the proposed LC VCO. From Table II, we can see that the increasing C_{gs12} by inserting C_A as in Fig. 3 in the proposed LC VCO results in higher ratio of MOS capacitance to the total capacitance. As a result, the tuning rang in the proposed LC VCO is reduced.

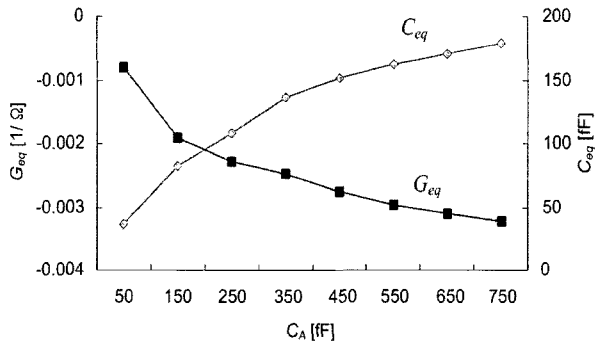

Fig. 5. Changes of C_{eq} and G_{eq} for variation of C_A.

Fig. 5 shows the simulation results of C_{eq} and G_{eq} for change of C_A.. C_{eq} increases with C_A, while G_{eq}, which is negative conductance, decreases with C_A, Considering the trade-off relation, C_A was chosen to be 240fF.

III. Measured Results and Discussion

Fig. 6 shows the photograph of the fabricated LC VCO. The chip size is 850×850μm^2.

The MOS varactor used in this paper is a typical accumulation mode n-well varactor shown in Fig. 7. The VCO control voltage is applied to the gate of the MOS varactor. Fig. 8 shows the variation of oscillation frequency as a function of the control voltage. As the control voltage varies from 0 to 2.5V, the oscillation frequency changes from 9.8-GHz to 12-GHz. The simulated and measured results agree well with each other. Fig. 9 is the measured spectrum of the output waveform. The estimated phase noise from the measured output spectrum is -103dBc/Hz at 1MHz offset.

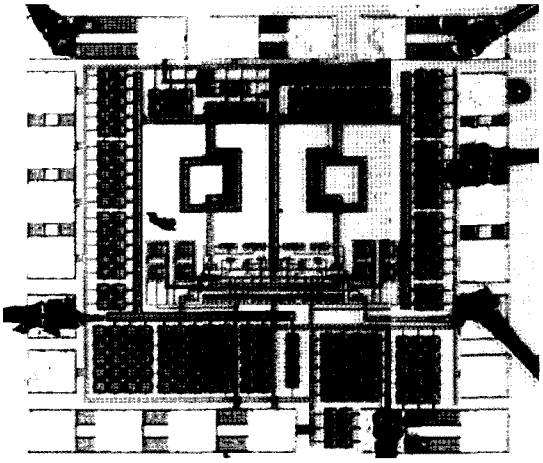

Fig. 6. Photograph of the fabricated VCO chip wire-bonded to test PCB.

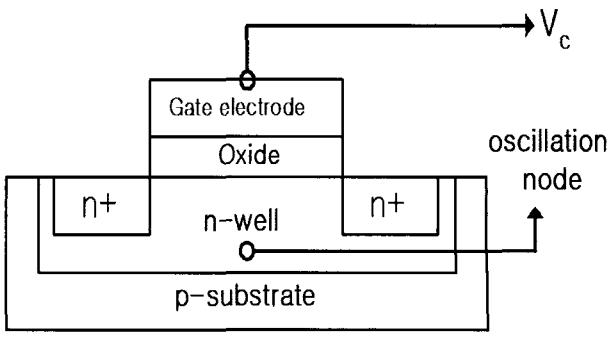

Fig. 7. Structure of the MOS varactor.

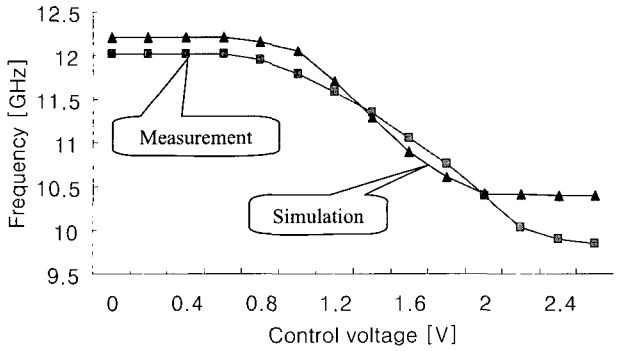

Fig. 8. Simulation and measurement of the *LC* VCO output frequency versus control voltage.

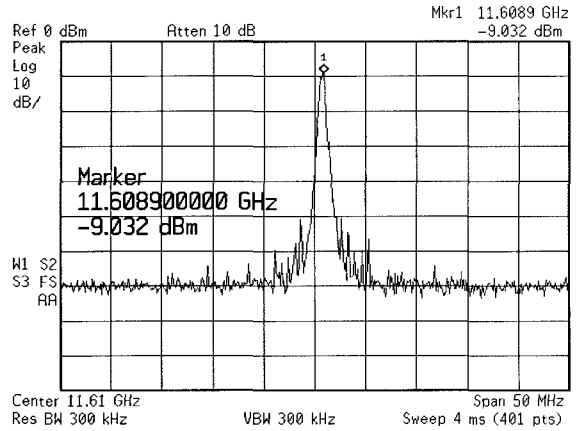

Fig. 9. Measured output spectrum of the *LC* VCO.

IV. CONCLUSIONS

Capacitive degeneration scheme that can attain a wide tuning range and high oscillation frequency was applied to CMOS *LC* VCO. It was proven through small signal analysis that the parasitic capacitance of the active devices in the proposed *LC* VCO is reduced in comparison to the traditional *LC* VCO using a cross coupled pair.

The fabricated *LC* VCO has a tuning range of about 20% with a power dissipation of 8.64mW. Table 3 shows the tuning ranges for the papers that have been published for 10-GHz frequency band. The proposed *LC* VCO has wider tuning range characteristics than those in the other papers.

Table 3. Comparison for tuning ranges.

Refer-ence	Power (mW)	Phase noise (dBc/Hz)	Tuning range (GHz)	Tuning range (%)	CMOS process (μm)
[4]	3.7	-102	9.53 ~ 10.03	5.1	0.18
[5]	28.0	-105	12.20 ~ 12.50	2.4	0.35
[6]	11.6	-115	9.67 ~ 9.93	2.7	0.35
[7]	28.0	-104	10.25 ~ 10.55	2.8	0.25
This	**8.6**	**-103**	**9.80 ~ 12.00**	**20.0**	**0.18**

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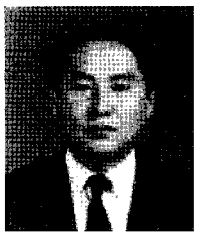

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