A 0.12GHz-1.4GHz DLL-based Clock Generator with a Multiplied 4-phase Clock Using a 0.18um CMOS Process

Hyung-Joon Chi, Jae-seung Lee, Jae-Yoon Sim, and Hong-June Park

Abstract—**A 0.12GHz~1.4GHz DLL-based clock generator with the capability of multiplied four phase clock generation was designed using a 0.18um CMOS process. An adaptive bandwidth DLL with a regulated supply delay line was used for a multiphase clock generation and a low jitter. An extra phase detector (PD) in a reference DLL solves the problem of the initial VCDL delay and achieves a fast lock time. Twice multiplied four phase clocks were generated at the outputs of four edge combiners, where the timing alignment was achieved using a coarse lock signal and the 10 multiphase clocks with T/8 time difference. Those four clocks were combined one more time using a static XOR circuit. Therefore the four times multiplication was achieved. With a 1.8V supply, the rms jitter of 2.1ps and the peak-to-peak jitter of 14.4ps were measured at 1.25GHz output. The operating range is 0.12GHz ~ 1.4GHz. It consumes 57mW and occupies 450*325um2 of die area.**

Index Terms—**Delay-locked loop (DLL), phase detector (PD), clock generator, edge combiner, low jitter, adaptive bandwidth.**

I. INTRODUCTION

Applications of serial link such as computer-to-computer or computer-to-peripheral interconnection are requiring gigabit-per-second data rates. As the transmission speed is increased, the supporting clock speed also should be increased. Therefore on-chip clock generation and multiplication with high-performance has received considerable attention for VLSI circuits in recent years. In a multi-Gb/s transceiver circuit, a low-jitter clock is required to achieve an acceptable bit error rate in the link.

A Phase-locked loop (PLL) is mostly used for high speed clock generation because it has an ability of frequency multiplication. But the PLL has a number of drawbacks ; it is required a complicate system for accurate clock generation in noisy environments such as power supply and substrate noise. At least, the PLL has two pole system so that it has limited stable operation region, which makes it difficult to design. In addition, the delay variations of VCO due to supply noise cannot be corrected instantaneously by the PLL. Therefore the PLL output jitter is accumulated over multiple oscillation cycles. On the other hand, a DLL has several advantages over PLLs. The DLL is a single-pole system so that it is inherently stable, easier to design than the PLLs. The DLL also needs smaller area for loop filter than PLLs. Because the DLL use an open loop voltage-controlled delay line (VCDL), the jitter is only accumulated in a delay line. However, the DLL doesn't have an ability of frequency multiplication as the PLL does. Therefore another circuits are needed for frequency multiplication[1,2]. In these days, DLL-based clock generators such as a multiplying DLL (MDLL) have been reported[3~7].

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Proposed MDLL consists of one reference DLL, four edge combiners and latches, and one xor gate. In a reference DLL, two phase detectors (PDs) are used. One is used for coarse locking and the other is used for fine locking. The former PD eliminates the constraint on the initial VCDL delay for the DLL to be locked at one clock period position and it reduces lock time due to the monotonic decreasement of the control voltage of VCDL[8]. An adaptive bandwidth scheme was used for low jitter and broad operating range[9]. This reference DLL makes one coarse lock signal and ten multiphase clocks with T/8 time difference ; T is the reference clock period. Edge combiners are also used for frequency multiplication by the factor of two. But those can not make evenly spaced multiphase clocks at the same time. In this paper, a evenly spaced multiplied multiphase clock generation technique was introduced.

Section 2 shows the architecture of the proposed DLL-based clock generator which has the ability of evenly spaced multiplied multiphase clock generation. Section 3 shows the measurement results. Conclusion is given in section 4.

II. ARCHITECTURE

Fig. 1 shows the total block diagram of the proposed MDLL. It consist of one reference DLL, four frequency multipliers (FM) and one xor gate. Reference DLL makes evenly spaced eight phase clocks which have the time delay of T/8 and two additional clocks for further use. Each FM has four input clocks which have T/4 time difference. Four FMs use even terms or odd terms to make four clocks which are multiplied by two. The FM_Trigger signal (Coarse_Lock) was used for timing alignment. These four clocks are combined in a xor gate so that another multiplication of two was achieved.

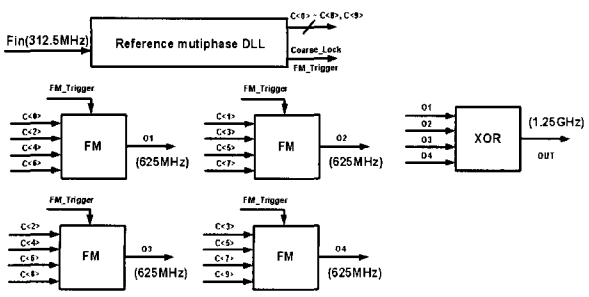

Fig. 1. MDLL architecture.

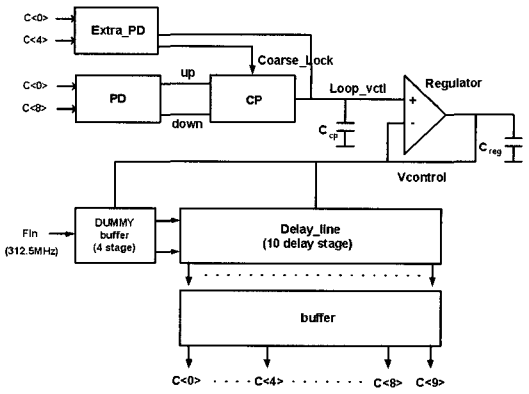

Fig. 2. Reference multiphase DLL.

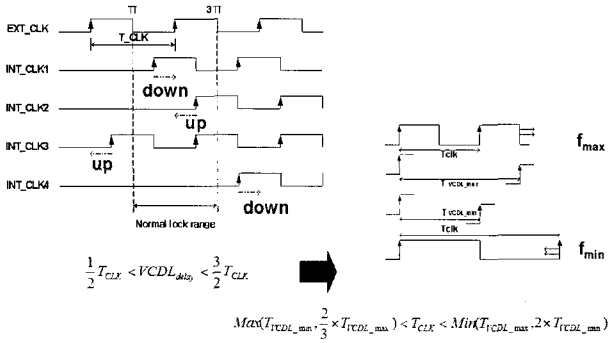

Fig. 3. Initial VCDL delay constraint of the DLL.

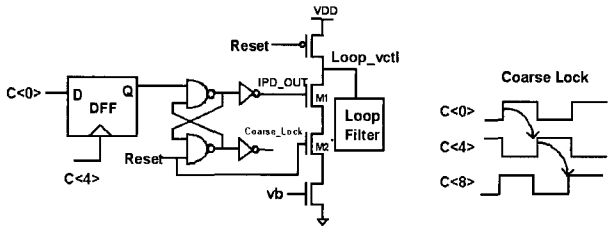

Fig. 4. Extra_PD in the reference DLL.

Fig. 2. shows the reference DLL, in which two loops exist. One is for coarse lock using Extra_PD and other blocks except the PD and CP, the other is for fine lock using all blocks except the Extra_PD. Conventioanl DLL has an intial VCDL delay problem at the power on state. Fig. 3 shows the problem and the initial VCDL delay constraint which results in a severly limited operating range. Extra_PD shown in Fig. 4 solves the constraint and also reduce lock time due to a monotonic decreasement of the control voltage of the VCDL. The extra_PD locates the rising edge of the middle clock near the falling edge of the first clock so that the rising edge of the last clock be located near the first clock next rising edge position. For this operation, it needs initial

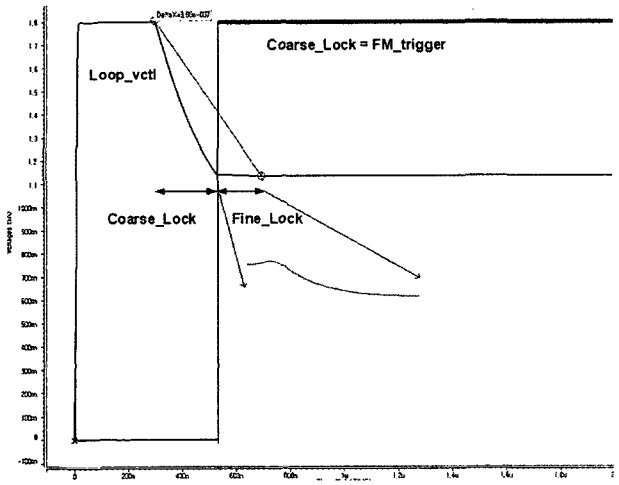

Fig. 5. HSPICE simulation of the reference DLL.

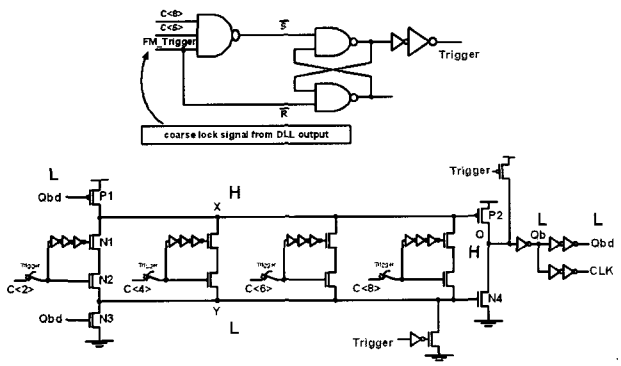

Fig. 6. FM circuit.

reset condition. Using loop control voltage, the charge pump (CP) current and the gain of the delay line are being controlled to keep the ratio of the loop bandwidth to operating frequency below 1/10. This is called adaptive bandwidth scheme.

Fig. 5. shows the simulation result of the reference DLL. At the initial reset, the Loop_vctl is high. When the reset signal is high, the Extra_PD works and it monotonically decrase the Loop_vctl until coarse lock is done. After coarse locking, main PD and CP works for fine locking. The coarse lock signal was used for triggering FM so that it was called FM_trigger.

The FM comprises one edge combiner and one latch. Fig. 6. shows the two components. The Trigger signal was used to activate the FM. And the trigger can be active high when the all three inputs of the nand gate are high. There are two processes. At first the FM_trigger should be high for the latch to change state because coarse lock signal should come first. After the FM_trigger signal is high, each FM waits for the last

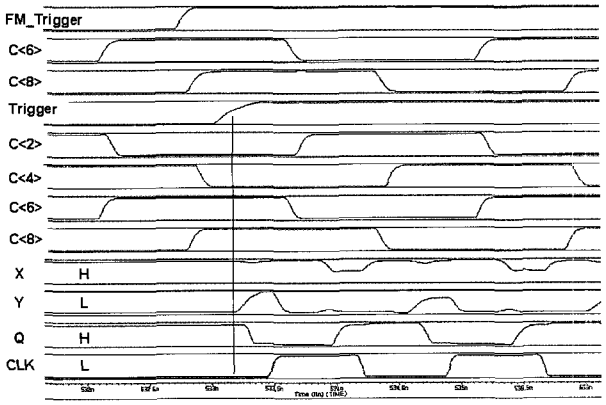

Fig. 7. HSPICE simulation of the FM circuit.

clock rising edge among four FM input clocks. Therefore the rising edge of the first clock in the FM always come after the FM is triggered. This distinguishes the combination of C<0>, C<2>, C<4>, C<6> from C<2>, C<4>, C<6>, C<8>, otherwise those combinations result in same outputs. Thus each output of the four FMs has different starting point, which makes evenly spaced multiplied four phase clocks.

Fig. 7. shows the simulation result of the FM. Before coare lock, the trigger signal is low so that node X and Q are high and node Y and Qbd are low. After the coarse lock , the FM_trigger signal is high and then FM waits for the last clock rising edge. Here the last clock is C<8>. After C<8> is high, trigger signal is high that makes the node Y is high, which in turn change the node Q into low. The node Y falls into low after three inverter delay between Q and Qbd. At the first clock C<2> rising edge, the node X is low and then the node Q is changed to high, and so on. Therefore FM output frequency is multiplied by two.

Another multiplication of two is achieved with the xor gate. A static xor gate shown in Fig. 8 is used. The reference DLL generates 8 phase clocks by internally comparing the rising edges between phase 0° and phase 360° of the output of the delay cells. The consecutive comparing through negative feedback loop guarantees that the rising edges are evenly spaced. Although the output duty error can exist, the output of the FM can have 50 % duty cycle because the FM uses rising edges only. The static xor gate use four FM outputs as inputs. And the inputs are located to make the node A toggle at the optimum position. Node n1 or n2 is pre-discharged before the node A discharge. And node p1 or p2 is pre-

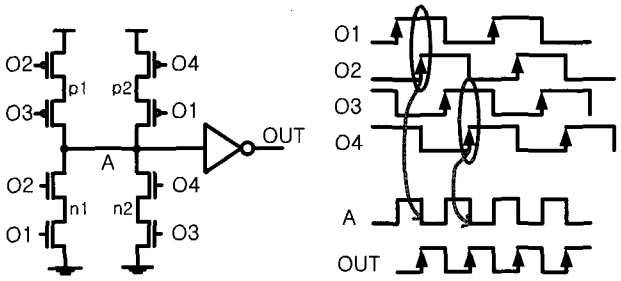

Fig. 8. Static xor gate.

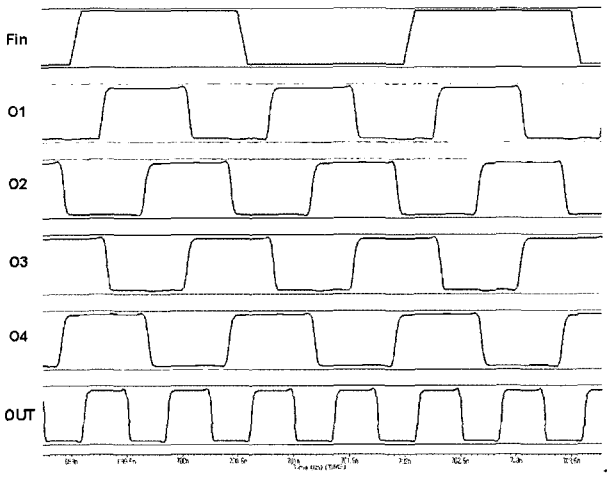

Fig. 9. HSPICE simulation of the MDLL.

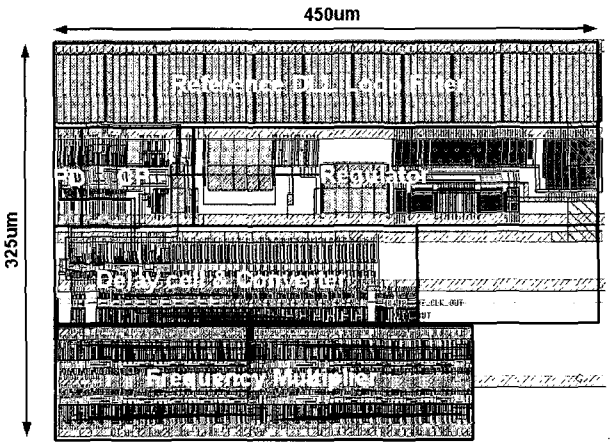

Fig. 10. Test chip layout.

charged before the node A charge.

Fig. 9. shows the total simulation result. In this case, the Fin indicates the external clock of 312.5MHz. The O1 through O4 are the outputs of the four FMs and have the frequency of 625MHz. These four signals are evenly spaced multiplied multiphase signlas. Finally the OUT signal is the xor output which has the frequency of 1.25GHz. The evenly spaced multiplied multiphase clocks can be used to make higher data rates than the on-chip frequency. And the multiplied single output can be used as a system clock.

Fig. 10. shows the test chip layout. The reference DLL has an area of 240x450 um^2 and the four FMs have an area of 88x350 um^2.

III. Measurement Results

Fig. 11. shows the external input clock of Fin and the final multiplied output clock. The Fin is 312.5MHz and the output is 1.25GHz. Fig. 12. shows the jitter performance at 1.25GHz output.The peak-to-peak jitter of 14.4ps and the rms jitter of 2.1ps.

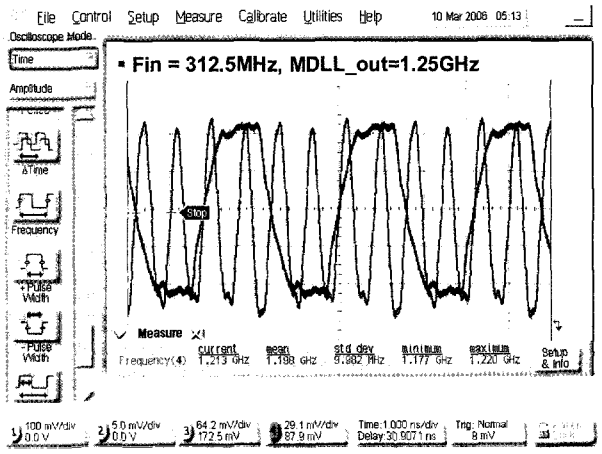

Fig. 11. Measured waveform of Fin and output.

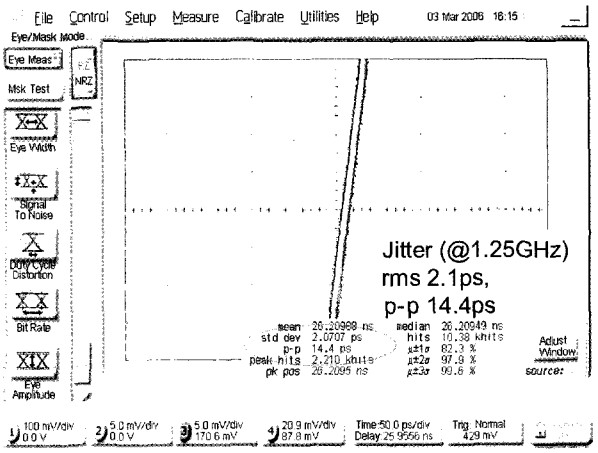

Fig. 12. Measured jitter of the output at 1.25GHz.

IV. Conclusions

A 0.18um CMOS 1.25GHz DLL-based clock generator was proposed. It can generate evenly spaced

multiplied four phase clocks and a signle multiplied clock. An adaptive bandwidth DLL with a regulated supply delay line was used for a multiphase clock generation and a low jitter. An extra PD in a reference DLL solves the problem of the initial VCDL delay and achieves fast lock time. Two times multiplied four phase clocks were achieved by four edge combiners and latches using coarse lock signal and 10 multiphase clocks with T/8 time difference. Those four clocks were combined using a static xor gate. Therefore four times single multiplication was achieved. With a 1.8V supply, rms jitter of 2.1ps and p-p jitter of 14.4ps was measured at 1.25GHz output. The operating range is 0.12GHz ~ 1.4GHz. It consumes 57mW and occupies 450*325um^2 of die area.

ACKNOWLEDGMENTS

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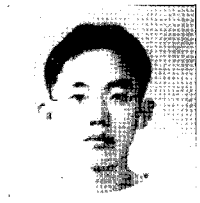

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