

Charge Pump Circuits with Low Area and High Power Efficiency for Memory Applications

Kyeong-Pil Kang and Kyeong-Sik Min

Abstract—New charge pump circuits with low area and high power efficiency are proposed and verified in this paper. These pump circuits do not suffer the voltage stress higher than V_{DD} across their pumping capacitors. Thus they can use the thin-oxide MOSFETs as the pumping capacitors. Using the thin-oxide capacitors can reduce the area of charge pumps greatly while keeping their driving capability. Comparing the new pump (NCP-2) with the conventional pump circuit using the thick-oxide capacitors shows that the power efficiency of NCP-2 is the same with the conventional one but the area efficiency of NCP-2 is improved as much as 71.8% over the conventional one, when the V_{PP}/V_{DD} ratio is 3.5 and $V_{DD}=1.8V$.

Index Terms—charge pump, power efficiency, area efficiency, memory, DRAM

I. INTRODUCTION

Charge pump circuits whose output voltage (V_{PP}) is higher than supply voltage (V_{DD}) have widely been used in many SoC applications. In the charge pump circuits, a V_{PP}/V_{DD} ratio is considered important and recently this ratio goes higher while V_{DD} becomes lower as devices are scaled further. This ratio is especially high in case of DRAM circuits, where V_{PP} is used to boost the word-line voltage higher than V_{DD} . Because the long refresh time is crucial to DRAM, the threshold voltage of memory cell is high in spite of low V_{DD} . Thus V_{PP} of the word-line boosting voltage should also be high enough

to overcome the speed degradation by this high threshold voltage [1]. To make V_{PP} higher than $2V_{DD}$, the number of stages of the charge pump has to be larger than 2 in recent DRAMs.

In addition to the word-line boosting, there are many other circuits such as the bit-line switch and the sense-amplifier driver where V_{PP} is used to compensate the slow speed due to the V_{DD} lowering. As more circuits in DRAM are driven by V_{PP} instead of V_{DD} , the charge pump should deliver larger current to its load than before. To increase the output current of charge pump, the pumping capacitance should be large. Because the area of charge pump is determined mainly by the area of its pumping capacitor, the large-area capacitor increases the total area of charge pump drastically. Hence it is very favorable to design an area-efficient charge pump to decrease the total chip area.

II. NEW CHARGE PUMP CIRCUITS

Many charge pumps have been proposed since 1970's. Of these, most popular ones are based on Dickson pump [2] or cross-coupled voltage doubler [1], [3]. Fig. 1(a) shows a conceptual diagram of these conventional circuits, where $C1$, $C2$, and $C3$ act as the pumping capacitors and the switches are assumed ideal. Here, though $C1$ has the voltage stress as high as V_{DD} , $C2$ and $C3$ suffer from the stress higher than V_{DD} . At the phase-I, $C1$ has a voltage of V_{DD} between its two terminals. At the following phase-II, the node 'A' is driven up to $2V_{DD}$ by the charge pumping so that a voltage as high as $2V_{DD}$ is stored across $C2$. At the following phase-I, $C2$ raises the node 'B' to $3V_{DD}$. At this time, a voltage as high as $3V_{DD}$ is stored across $C3$. At the next phase-II, $C3$ raises the node 'C' up to $4V_{DD}$. By doing so, the

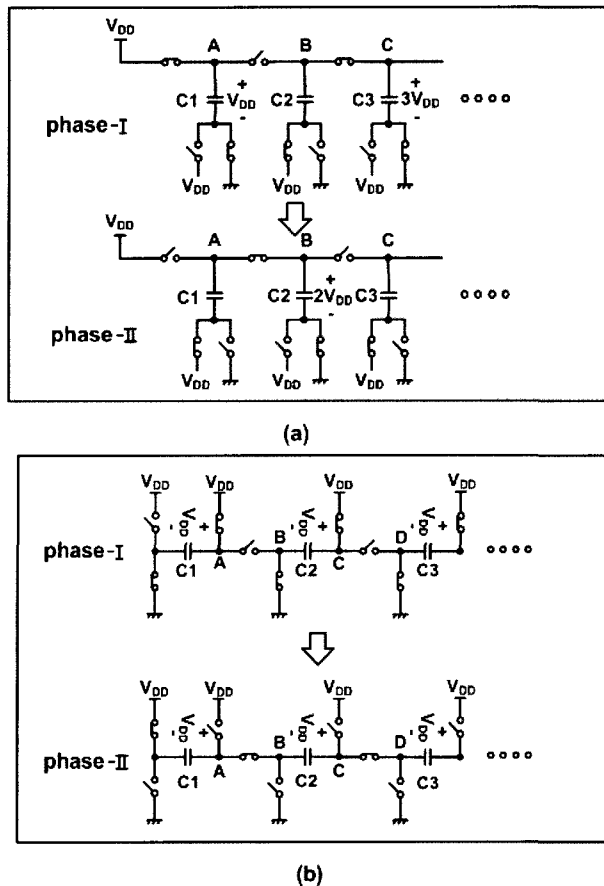


Fig. 1. (a) A conceptual diagram of the conventional charge pump (b) A conceptual diagram of new charge pump.

pump circuit can generate V_{PP} higher than V_{DD} . As mentioned earlier, one should note that C2 and C3 suffer the voltage stress as high as $2V_{DD}$ and $3V_{DD}$, respectively. The pumping capacitor with thin oxide can not tolerate the voltage stress higher than V_{DD} so that C2 and C3 in Fig. 1(a) have to be made with thick-oxide devices.

Fig. 1(b) shows a diagram of new architecture of low-area pump circuits where all the pumping capacitors suffer the stress only as high as V_{DD} . Instead of the pumping capacitors, however, the switches in Fig. 1(b) tolerate the stress higher than V_{DD} . Hence the pumping capacitors are C1, C2, and C3 as shown in Fig. 1(b) can be made with the thin-oxide transistors. By doing so, the layout area of C1, C2, and C3 becomes smaller compared with that of thick-oxide transistors. Because the area of the pumping capacitors takes the largest part of the total pump area, it is very helpful to make the area of the pumping capacitors small for reducing the total pump area. For example, when a 0.18- μm process is

used, the area of pumping capacitors takes more than 90% of the total pump area.

Now let's discuss the switches in Fig. 1(b). Here the switches should be made with the thick-oxide transistors because there is the voltage stress higher than V_{DD} unlike the pumping capacitors of C1, C2, and C3. Generally the layout area of switches is much smaller than that of pumping capacitors. Thus using the thick-oxide transistors as the switches does hardly increase the total pump area. And, using them does not give a serious impact on the performance of pump. The performance of charge pump depends on the size of pumping capacitor much more than the size of transistor as the switch.

The Schematics of Modified Dickson-based Charge Pump (MDCP) [4] and Voltage-Doubler-based Charge Pump (VDCP) [1], [3] are shown in Fig. 2(a) and (b), respectively. Both circuits have 3 stages where they can generate V_{PP} as high as $\sim 4V_{DD}$. In Fig. 2(a), MC1, MC2, MC3, and MC4 act as the pumping capacitors and MT1, MT2, MT3, MT4, and MT5 are the charge-transfer switches. MD1, MD2, and MD3 are the diode-connected transfer switches. MP1, MN1, MP2, MN2, MP3, and MN3 which drive the gates of charge-transfer switches are the control switches. The charge-transfer switches can be fully turned on through MP1 and turned off through MN1 according to the clock signal. MT5 does not deliver the output current to the load capacitor (C_L). Instead, MT5 is used to deliver an over-drive voltage to the gate of MT3. The pumping capacitors of MC2, MC3, and MC4 in Fig. 2(a) suffer the voltage stress higher than V_{DD} should be made with the thick-oxide devices if the MOSFET capacitors are used. The switches, however, can be implemented by the thin-oxide transistors.

In Fig. 2(b), MC1, MC2, MC3, MC4, MC5, and MC6 all are representing the pumping capacitors. MN1 and MP1 are responsible for precharging the pumping node and transferring the charges into the following stage, respectively. MN1 and MP1 connected to MC1 are cross-coupled with MN2 and MP2 connected to MC2. This cross-coupled architecture repeats at the following two stages in Fig. 2(b). Like Fig. 2(a), MC3, MC4, MC5, and MC6 in Fig. 2(b) suffer the voltage stress higher than V_{DD} . To operate reliably under the condition of high stress, MC3, MC4, MC5, and MC6 are made with

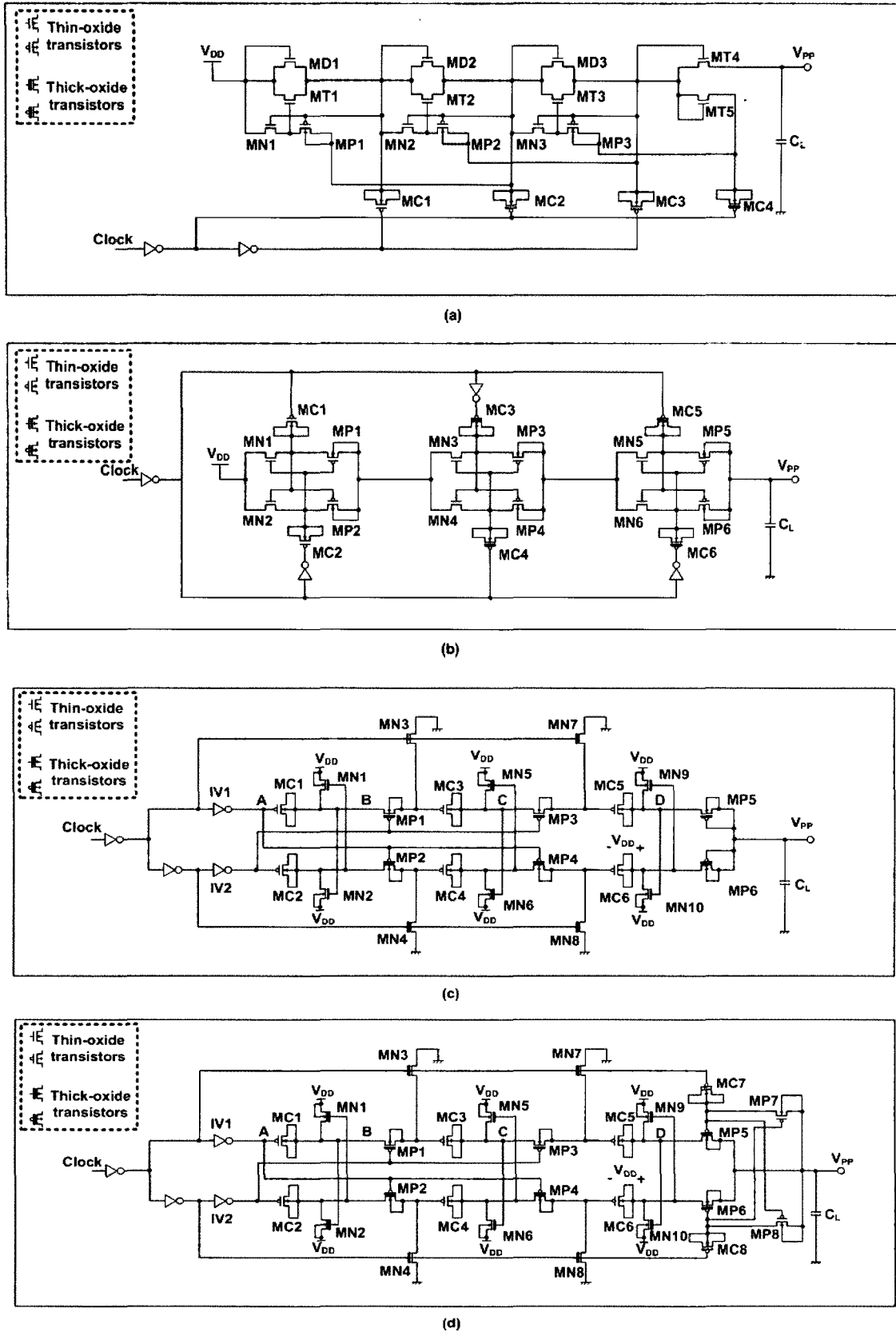


Fig. 2. Schematics of (a) Modified Dickson-based Charge Pump circuit (MDCP), (b) Voltage-Doubling-based Charge Pump circuit (VDCP), (c) New Charge Pump-1 circuit (NCP-1), and (d) New Charge Pump-2 circuit (NCP-2). They are 3-stage pumps.

the thick-oxide transistors but the switches can be made with the thin-oxide ones in Fig. 2(b).

Fig. 2(c) shows a New Charge Pump (NCP-1), where all the pumping capacitors of MC1, MC2, MC3, MC4, MC5, and MC6 have the same stress as high as V_{DD} [5]. When the clock signal is low, MN1, MN3, MN5, MN7, and MN9 are turned on so that MC1, MC3, and MC5 have the same voltage as high as V_{DD} across themselves. At this time, MP1 and MP3 are turned off. At this precharge phase, the stored voltages across MC1, MC3, and MC5 are as high as V_{DD} . And, when the clock signal becomes high, IV1 drives the node 'A' from V_{SS} to V_{DD} . The node 'A' raises the node 'B' from V_{DD} to $2V_{DD}$ and the node 'B' raises the following node 'C' from V_{DD} to $3V_{DD}$. Simultaneously, the node 'C' raises the node 'D' from V_{DD} to $4V_{DD}$. Of course, at this time, MN1, MN3, MN5, MN7, and MN9 are turned off by their cross-coupled nodes and MP1 and MP3 are turned on to transfer the charges with high voltages to the following stages. In the same manner, MC2, MC4, and MC6 work together to generate V_{PP} as high as $4V_{DD}$. As shown in Fig. 2(c), MC1, MC3, and MC5 with their control switches are crossly coupled with MC2, MC4, and MC6 with the switches. MP5 and MP6 are the diode-connected transistors, which lose their output voltage as much as their threshold voltage. Here MC1, MC2, MC3, MC4, MC5, and MC6 can be made with the thin-oxide transistors because their voltage stress is the same as V_{DD} , thus making it possible to reduce the area of pumping capacitors very much compared with Fig. 2(a) and (b).

As mentioned earlier, there is a voltage drop as much as the threshold voltage through the diode-connected MP5 and MP6 of NCP-1 shown in Fig. 2(c). To avoid this voltage loss, NCP-2 in Fig. 2(d) is also proposed in this paper. As you can see in Fig. 2(d), the diode-connected PMOSFETs in Fig. 2(c) are replaced with the auxiliary pump that is composed of MP5, MP6, MP7, MP8, MC7, and MC8. Here MP5 and MP6 act as the final transfer switches that deliver the pumping current to the load without any voltage loss unlike Fig. 2(c). MP5 and MP6 in Fig. 2(d) are controlled by the MC7, MC8, MP7, and MP8. Though MC7 and MC8 should be made with the thick-oxide devices because they suffer the stress higher than V_{DD} , their sizes can be very small

because they drive only the gates of MP5 and MP6. The area of this auxiliary pump increases the total pump area very little. And, because MC7 and MC8 do not act as the pumping capacitors, their small size does not degrade the pumping capability. Here, the capability is determined mainly by the size of pumping capacitor.

III. SIMULATION AND COMPARISON

Fig. 3(a) and (b) compare the pumping speeds of MDCP, VDCP, NCP-1, and NCP-2 which are shown in Fig. 2(a), (b), (c), and (d), respectively. Fig. 3(a) is for $V_{DD}=1.8V$ and Fig. 3(b) for $V_{DD}=1.5V$. The comparison is done by SPICE simulation, where the 0.18- μm SPICE model obtained from the industry is used and the temperature is kept at 25 °C. The SPICE model includes both the thin-oxide and thick-oxide transistors. The thin-oxide transistor operates with $V_{DD}=1.8V$, but the thick-oxide one can cover a wide range of voltages from

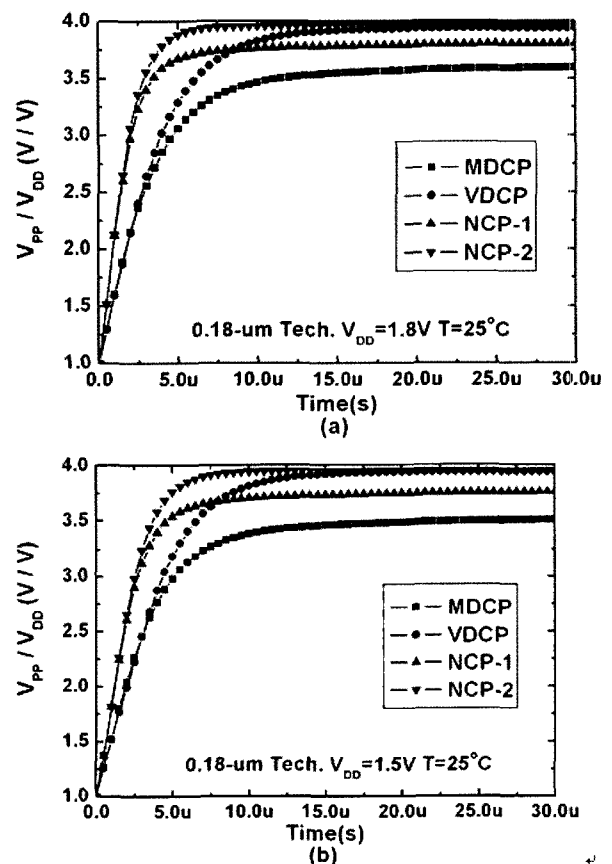


Fig. 3. (a) Comparison of the pumping speeds of MDCP, VDCP, NCP-1, and NCP-2 at $V_{DD}=1.8V$ (b) Comparison of the pumping speeds of MDCP, VDCP, NCP-1, and NCP-2 at $V_{DD}=1.5V$.

V_{SS} to $4V_{DD}$. Of MDCP, NCP-2, the pumping speeds of NCP-1 and NCP-2 seem faster than MDCP and VDCP especially when the pumping operation starts. This is because NCP-1 and NCP-2 deliver their output currents larger than those of MDCP and VDCP at the pumping start-up. Here NCP-1 and NCP-2 use the thin-oxide capacitors as their pumping capacitors, while MDCP and VDCP use the thick-oxide ones. As indicated in Fig. 3(a) and (b), V_{PP} of NCP-1 seems to saturate below $4V_{DD}$. This is because NCP-1 loses its output voltage as much as the threshold voltage when NCP-1 delivers its output voltage to the load. This voltage loss also occurs in MDCP, because the diode-connected MT4 is used as the final transfer switch. To overcome this voltage loss, as mentioned earlier, NCP-2 with the auxiliary pump to control the final transfer gates is proposed. In Fig. 3(a) and (b), NCP-2 shows a non-saturated characteristic and the V_{PP}/V_{DD} ratio of NCP-2 reaches to 4 when its number of stages is 3.

Fig. 4(a) and (b) compare the power efficiency of 4 pump circuits. Here, the power efficiency is defined by an I_{PP}/I_{DD} ratio, where I_{PP} and I_{DD} are the amount of current delivered to the load and the amount of current supplied from V_{DD} , respectively. Of 4 charge pumps, MDCP shows the sharpest degraded efficiency as the V_{PP}/V_{DD} ratio becomes closer to 4. The efficiency of NCP-1 is little degraded compared with that of VDCP when the V_{PP}/V_{DD} ratio is in between 1 and 3.5. When this ratio is larger than 3, however, the efficiency of NCP-1 becomes worse than that of VDCP. This is due to the loss of output voltage of NCP-1, as indicated in Fig. 3(a) and (b). NCP-2 that does not lose the output voltage has the same power efficiency with that of VDCP, even when the V_{PP}/V_{DD} ratio is over 3. One more comment here is that the power efficiency of VDCP and NCP-2 becomes worse rapidly when their V_{PP}/V_{DD} ratio becomes larger than 3.5. As the V_{PP}/V_{DD} ratio goes closer to 4, the output currents of VDCP and NCP-2 decrease rapidly, thus their efficiency being degraded,

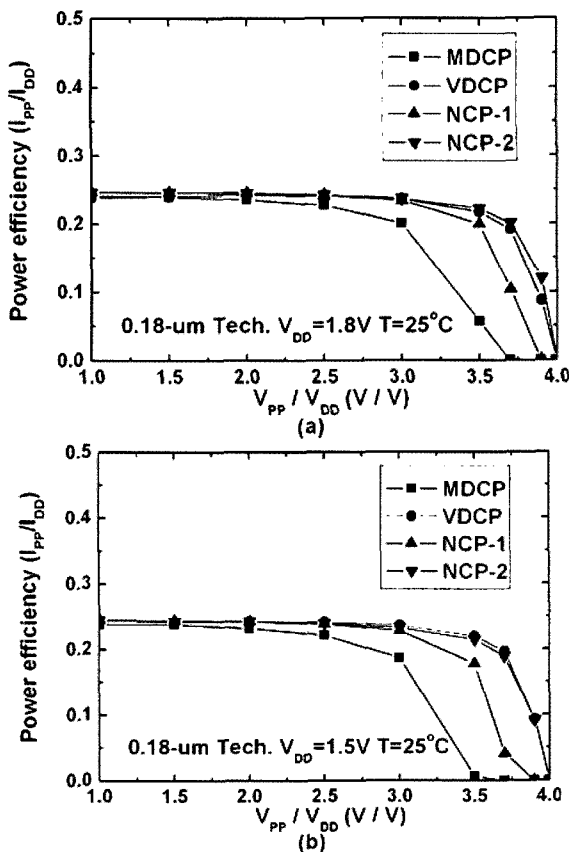


Fig. 4. (a) Comparison of the power efficiency of MDCP, VDCP, NCP-1, and NCP-2 at $V_{DD}=1.8\text{V}$ (b) Comparison of the power efficiency of MDCP, VDCP, NCP-1, and NCP-2 at $V_{DD}=1.5\text{V}$.

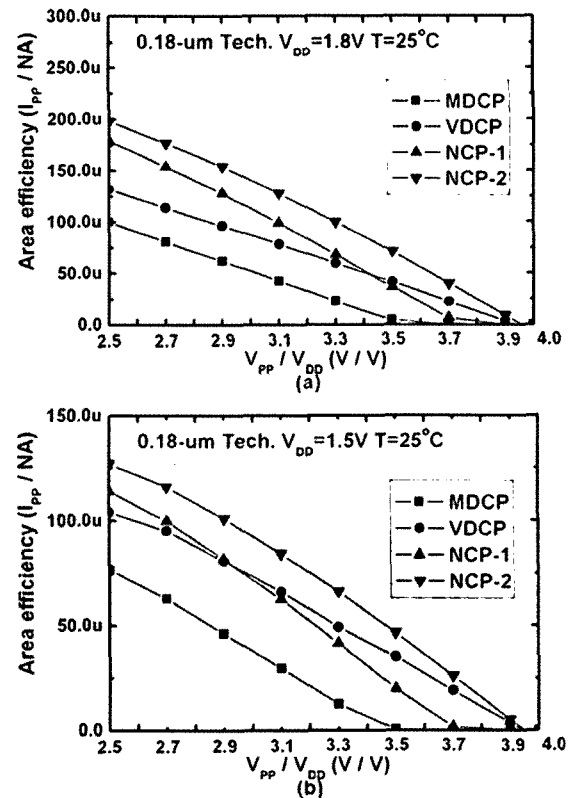


Fig. 5. (a) Comparison of the area efficiency of MDCP, VDCP, NCP-1, and NCP-2 at $V_{DD}=1.8\text{V}$ (b) Comparison of the area efficiency of MDCP, VDCP, NCP-1, and NCP-2 at $V_{DD}=1.5\text{V}$.

too. For the 3-stage pump circuits, the ratio of V_{PP}/V_{DD} is practically chosen between 3 and 3.5, since their efficiency goes very worse if the ratio becomes larger than 3.5.

Fig. 5(a) and (b) compare the area efficiency of 4 charge pumps. Here, the area efficiency is defined by an I_{PP}/NA ratio, where NA is a normalized value of charge pump area. The pump area mainly depends on the area of its pumping capacitors. Of 4 pumps, NCP-1 and NCP-2 use the thin-oxide transistors as their pumping capacitors, while MDCP and VDCP use the thick-oxide capacitors. Thus NCP-1 and NCP-2 can deliver the output currents larger than those of MDCP and VDCP, when the areas of the pumping capacitors of NCP-1 and NCP-2 are the same with those of MDCP and VDCP. Comparing NCP-1 with VDCP shows, however, the area efficiency of NCP-1 becomes worse than VDCP when the ratio of V_{PP}/V_{DD} is over 3.5 and $V_{DD}=1.8V$. This is due to the loss of output voltage of NCP-1. When $V_{DD}=1.5V$, the crossover between the efficiency of NCP-1 and VDCP occurs earlier than $V_{DD}=1.8V$. In Fig. 5(b), the V_{PP}/V_{DD} ratio corresponding to the crossover point is around 2.9. For NCP-2, the area efficiency is improved by eliminating the sacrificial voltage loss. The area efficiency of NCP-2 seems better than those of VDCP and NCP-1 in the entire range of V_{PP}/V_{DD} ratio, as shown in Fig. 5(a) and (b).

Fig. 6 compares the layout areas of pumping capacitors in Fig. 2(a), (b), and (c). Fig. 6(a) is the layout of thick-oxide capacitor for MDCP and VDCP. Fig. 6(b) is the layout of thin-oxide capacitor for NCP. Though

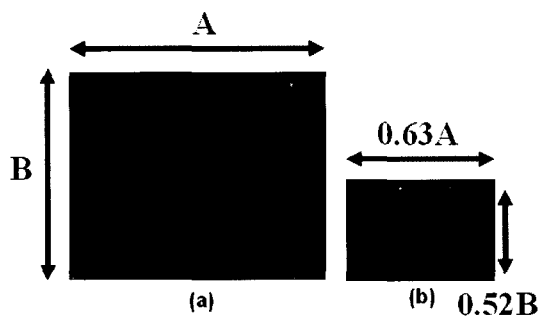


Fig. 6. (a) A layout of thick-oxide capacitor for MDCP and VDCP with their capacitance as large as 5.5pF (b) A layout of thin-oxide capacitor for NCP-1 and NCP-2 with their capacitance as large as 5.5pF.

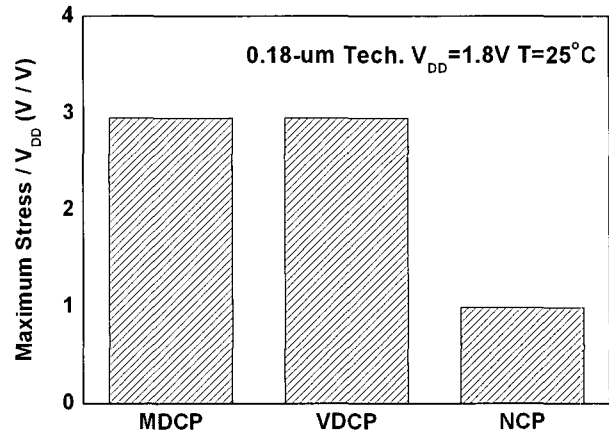


Fig. 7. (a) Comparison of the maximum voltage stress of MDCP, VDCP, NCP-1, and NCP-2 at $V_{DD}=1.8V$.

their capacitance values are the same, the area of Fig. 6(b) is only 33% of the area of Fig. 6(a). Here the capacitors are drawn by 0.18- μm design rules and their capacitance values are predetermined as 5.5pF.

Fig. 7 shows the maximum voltage stress across the pumping capacitor of NCP-1 and NCP-2 does not exceed V_{DD} . However, the stress of the MDCP and VDCP is estimated as high as almost $3V_{DD}$ when their stage number is assumed 3.

IV. CONCLUSIONS

New charge pump circuits with low area and high power efficiency are proposed and verified in this paper. These pump circuits do not suffer the voltage stress higher than V_{DD} across their pumping capacitors. Thus they can use the thin-oxide MOSFETs as their pumping capacitors. Using the thin-oxide capacitors can reduce the area of charge pump circuits greatly. Comparing NCP-2 using the thin-oxide capacitors with the conventional pumps using the thick-oxide capacitors shows that the power efficiency of NCP-2 is the same but the area efficiency is improved as much as 71.8% than VDCP, when the V_{PP}/V_{DD} ratio is 3.5. And, the area efficiency of NCP-2 shows 50% better than VDCP when the V_{PP}/V_{DD} ratio is 2.5.

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low-power circuit design.

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