InGaAs Nano-HEMT Devices for Millimeter-wave MMICs

Sung-Won Kim, Dae-Hyun Kim, Seong-Jin Yeon, and Kwang-Seok Seo

Abstract—**To fabricate nanometer scale InGaAs HEMTs, we have successfully developed various novel nano-patterning techniques, including sidewall-gate process and e-beam resist flowing method. The sidewall-gate process was developed to lessen the final line length, by means of the sequential procedure of dielectric re-deposition and etch-back. The e-beam resist flowing was effective to obtain fine line length, simply by applying thermal excitation to the semiconductor so that the achievable final line could be reduced by the dimension of the laterally migrated e-beam resist profile. Applying these methods to the device fabrication, we were able to succeed in making 30nm $In_{0.7}Ga_{0.3}As$ HEMTs with excellent f_T of 426GHz. Based on nanometer scale InGaAs HEMT technology, several high performance millimeter-wave integrated circuits have been successfully fabricated, including 77 GHz MMIC chipsets for automotive radar application.**

Index Terms—**InGaAs, HEMT, nano-patterning, MMIC, automotive radar**

I. INTRODUCTION

To meet the increasing demand for high speed applications such as high-frequency wireless systems and high-speed optical-fiber communication systems, InAlAs/InGaAs High-Electron-Mobility-Transistor (HEMT) is one of the promising device technologies because of its high carrier mobility and large sheet carrier concentration achieved by this material system. These kinds of material systems have been grown either InP substrate or GaAs substrate. Recently, InGaAs/InAlAs HEMT on GaAs substrate, so called metamorphic HEMT (MHEMT), has emerged as a cost-effective technology for the next-generation high speed systems. Fig. 1 shows Hall mobility ($\mu_{n,Hall}$) and conduction band discontinuity (ΔE_C) as a function of the used indium content in both InGaAs HEMTs, at room temperature. While InP-based InGaAs HEMTs is limited to the narrow range of indium content, GaAs-based InGaAs HEMTs (M-HEMTs) have a wider range of indium compositions that are available and thereby enable customization of the device's properties specific to each application.

In addition to these applications, InGaAs HEMTs have also been marked by a promising candidate of the future logic technology beyond CMOS roadmap. Recently it was demonstrated that non-optimized 50nm $In_{0.7}Ga_{0.3}As$ HEMTs provided high speed performance with 15 times lower DC power dissipation and at least 2.7 times higher cutoff frequency (f_T) at equivalent DC power dissipation level, compared with state-of-the-art Si MOSFETs [1].

Recently, the speed of InGaAs HEMTs has been remarkably boosted up [2-3]. A current record of cutoff frequency (f_T) for HEMT is 562 GHz with L_g of 25 nm [2]. This was achieved with state-of-the-art electron beam lithography machine having high acceleration voltage, such as 100 keV to define fine line as small as 25 nm. On the other hand, a great deal of our effort has gone into obtaining high f_T InGaAs HEMTs without the aid of state-of-the-art electron beam lithography machine, by utilizing novel fabrication techniques such as the sidewall gate process and the e-beam resist flowing technique [4-5].

Based on the enormous improvement in InGaAs HEMT technology, various ultra-high-speed integrated circuits (ICs) have been widely explored and successfully developed in recent years [6], which include millimeter-

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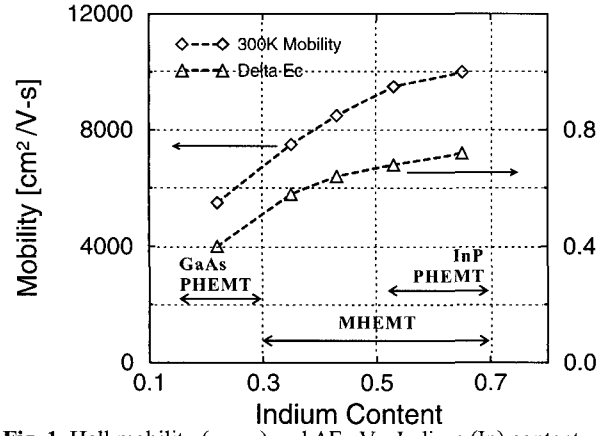


Fig. 1. Hall mobility ($\mu_{n,Hall}$) and ΔE_C Vs. Indium (In) content.

wave MMICs and ultra-high-speed ICs for optical fiber communication system. Table 1 summarizes the reported various IC results, based on InGaAs HEMT technology.

In this paper, nanometer scale InGaAs HEMT fabrication technologies, beyond conventional electron beam lithography limitation, are described. Based on these InGaAs HEMT technologies, we demonstrate several millimeter-wave MMICs, such as 77 GHz MMIC chipsets.

Table 1. Reported various ultra high-speed ICs.

IC function	Technology	Institute	Year
100 Gb/s MUX/DEMUX	0.1 μm $In_{0.53}Ga_{0.47}As$	NTT	2004
180~205 GHz MMIC	0.1 μm $In_{0.53}Ga_{0.47}As$	HRL	2001
160~215 GHz MMIC	0.07 μm $In_{0.7}Ga_{0.3}As$	TRW	2002
220~230 GHz LNA MMIC	0.05 μm $In_{0.65}Ga_{0.35}As$	Fraunhofer	2005

II. NANO-PATTERNING TECHNIQUES

In order to achieve finer line length, we applied simple but attractive several nano-patterning techniques: the sidewall gate process, the e-beam resist flowing and sloped RIE etching method. The sidewall process has been widely employed to overcome conventional lithography limitation. Finer line can be achieved through the formation of sidewall spacers, which result from the sequential procedure of initial dielectric etch, dielectric re-deposition, and final etch-back of the re-deposited film. Recently, resist thermal flow and chemical shrink technique has gained much attention, because it could simply offer finer lines without state-of-the-art lithography machine.

We have realized nanoscale gate length with the novel sidewall process, in which two dielectric layers of SiN_x and SiO are properly utilized and each layer is etched by different plasma gas chemistry [4]. The actual etch selectivity of the oxide layer over the nitride is over 20 in our process. This feature does ensure the reproducibility of the proposed sidewall gate process. Applying the developed sidewall process to the initial line length of about 60 nm, we could achieve gate length (L_g) as small as of 30 nm.

Fig. 2(a) and (b) show conceptual schematics of line length reduction by resist thermal flow and sloped-etching method. After defining narrow line by conventional e-beam process on single resist layer, we apply thermal heating in order to make the defined edge of e-beam resist to flow. And then, dielectric etching by SF_6-based RIE with some degree of an-isotropy is applied, in which the final line length on the semiconductor surface is shrunk further by the degree of an-isotropy in this RIE etching process. Fig. 3(a) shows the dependence of the obtained line length size on the thermal flow temperature. The initial 100 nm line can be easily shrunk to less than 35 nm

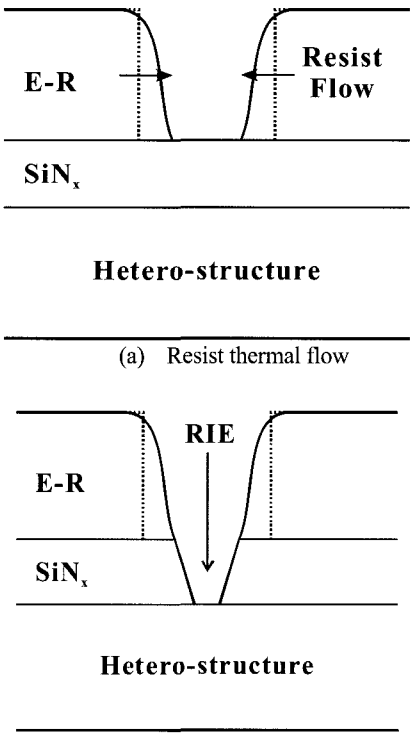
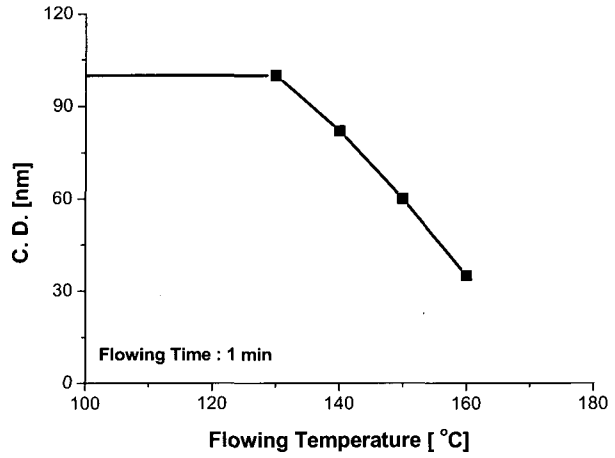
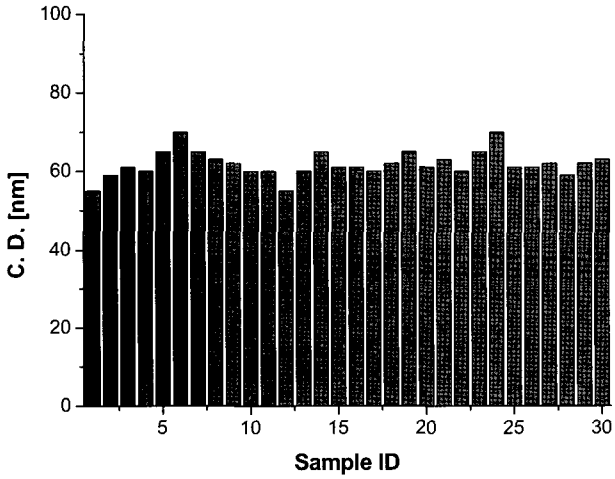


Fig. 2. Conceptual schematics for line length reduction.

after a simple thermal excitation at 160°C. Fig. 3(b) shows the uniformity data of the achieved line length, and we can see that standard deviation (δ) is less than 4 nm, which is quite acceptable to be applied for the device fabrication.



(a) Line opening vs. flow temp



(b) Uniformity of line length

Fig. 3. Resist thermal flow & chemical shrink technique.

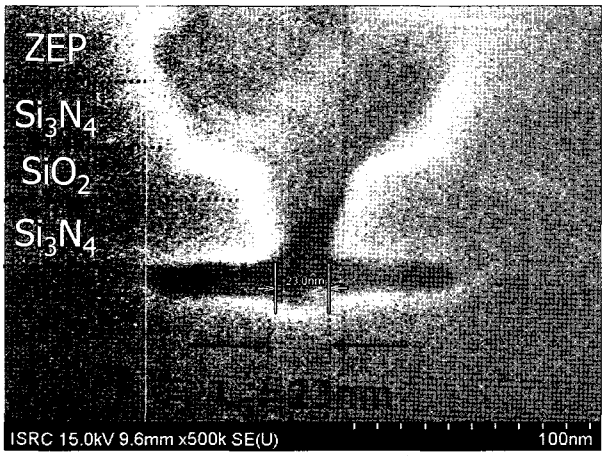


Fig. 4. SEM image of 23nm opening with sloped-etching method.

By exploiting sloped plasma etching method with deliverately employed SiN_x and SiO_2 dielectrics and SF_6 and CF_4 plasma etching, very fine nano-scale opening can be fabricated. By using $SiN_x/SiO_2/SiN_x$ triple dielectrics, SF_6 and CF_4 plasma etching, and ZEP electron beam photo-resist, we could define the fine openings as small as 23nm with 130nm initially defined patterns, which is shown in Fig. 4.

III. CHARACTERISTICS OF INGAAS NANO-HEMTS

In order to fabricate high performance and high yield HEMT devices, we should carefully optimize the gate processing steps which are the most important and delicate processes in HEMT fabrication. Wet or dry gate recess etching process should be developed to provide uniform and controllable etching profiles and good etching selectivity for capping layer with minimal surface damage. In nanoscale T-gate HEMT devices, new issues are arising such as complete gate metal filling, reduction of the gate metal capacitance, and structural stability of nanoscale T-gate metals.

Partly due to the lack of proper dry etch process, wet gate recess etch is normally employed in the InGaAs HEMT process. Two-step gate recess etch [7] with InP etch stopper is found to be effective to reduce Kink phenomena. To improve the uniformity and yield in wet-processed HEMT devices, we introduced ultrasonic-assisted recess method. Through optimization of etch conditions for 100nm gate devices, we could achieve HEMT device yield higher than 99% with reduced standard deviation of threshold voltage of 20mV. The 100nm $In_{0.65}GaAs/In_{0.52}AlAs$ HEMT devices fabricated with citric-acid based selective etchant showed good DC and microwave performances with a transconductance of 1.2 S/mm, a maximum saturated drain current of 800 mA/mm, a cutoff frequency f_T of 250 GHz .

Surface treatment before Schottky metal deposition could change Schottky barrier height (SBH), affecting gate leakage characteristics. Ar plasma treatment was found to be effective for Schottky barrier height enhancement on InAlAs, thereby improving the device characteristics of InAlAs/InGaAs/InP HEMTs and $In_{0.4}AlAs/In_{0.35}GaAs$ MHEMTs [8]. We established the technology for high performance 100 nm MHEMTs by

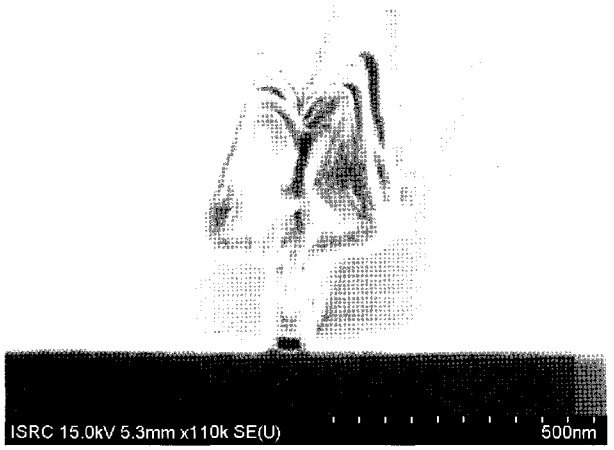


Fig. 5. SEM image of 70nm T-gate.

employing Ar surface treatment before gate metal deposition, with high extrinsic transconductance of 700 mS/mm and high f_T of 210 GHz [8].

In order to get high performance of MHEMTs, 70nm T-gate was fabricated by bi-layers of ZEP and UV5 [Fig. 5]. The devices with 70 nm T-gate exhibit good characteri stics such as high extrinsic transconductance of 850 mS/mm and high f_T of 235 GHz.

For 30nm HEMT fabrication, we employed MBE-grown InGaAs/InAlAs epitaxial layer structure on InP substrate with channel indium content of 70 % (Fig. 6), in order to enhance the carrier's transport property. We also used 4 nm thin InP layer, which acts as a good gate recess etch-stopper as well as a good surface passivation layer. Device fabrication began with mesa isolation through wet chemical etching, and then Ni/Ge/Au was evaporated and lifted off to form source and drain alloyed ohmic contact with 2 μm spacing.

n+ Cap	InGaAs, x = 0.53	20 nm
Stopper	InP	4 nm
Barrier	InAlAs, x = 0.52	6 nm
δ-doping	Si	-
Spacer	InAlAs, x = 0.52	4 nm
Channel	InGaAs, x = 0.53	3 nm
	InGaAs, x = 0.7	8 nm
	InGaAs, x = 0.53	4 nm
Buffer	InAlAs, x = 0.52	500 nm
3 Inch S. I. InP Substrate		

Fig. 6. Epitaxial Layer Structure grown by MBE.

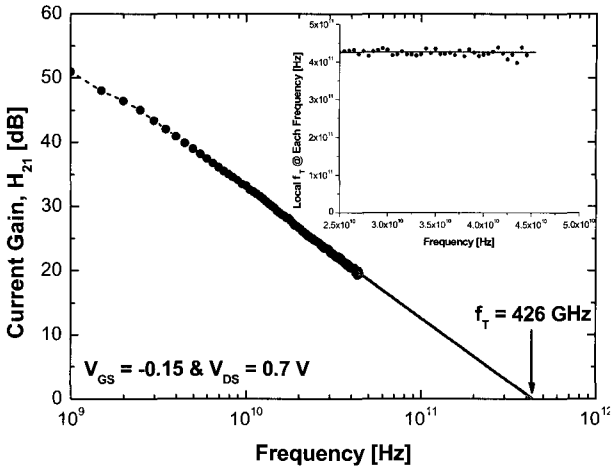


Fig. 7. Output characteristics of 30 nm $In_{0.7}Ga_{0.3}As$ HEMTs.

T-gate with 30 nm gate opening was fabricated by forming narrow single lines by means of resist thermal flow and sloped-etching method. Bi-layers of ZEP and PMGI were used to form wide T-gate head. Then, a gate recess process had been done by sequential procedure of selective wet etching of InGaAs cap by citric acid and an-isotropic etching of InP stopper by Ar-based RIE.. The output characteristics of the fabricated 30 nm $In_{0.7}Ga_{0.3}As$ HEMTs exhibited excellent pinch-off behavior up to high drain bias of 1 V, and good modulation capability. Typical maximum transconductance ($G_{m,max}$) and off-state break-down voltage ($BV_{GD,OFF}$) were 1.3 S/mm at the V_{DS} of 0.5 V and -1.4 V, respectively.

The small signal scattering-parameters (S-parameters) of 2 × 50 μm $In_{0.7}Ga_{0.3}As$ HEMTs were measured using the 8510C network analyzer (1-40 GHz). Shown in Fig. 7 is the plot of short-circuit current gain (H_{21}) and unilateral gain as a function of the measured frequency, biased at V_{GS} of -0.15 V and V_{DS} of 0.7 V. Extrapolating H_{21} to

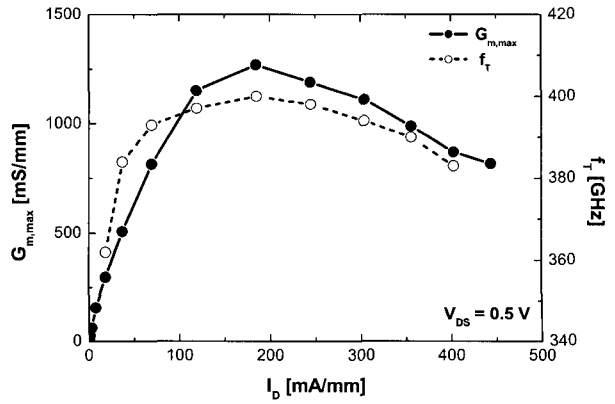
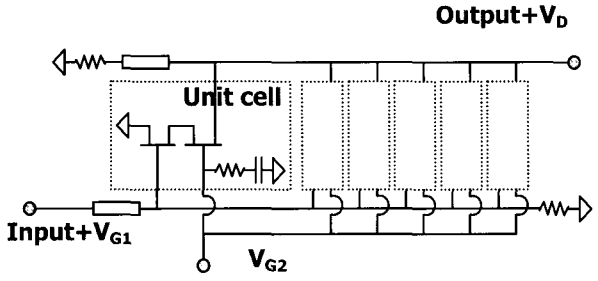


Fig. 8. Bias dependent $G_{m,max}$ and f_T characteristics of 30 nm $In_{0.7}Ga_{0.3}As$ HEMTs at the V_{DS} of 0.5 V.

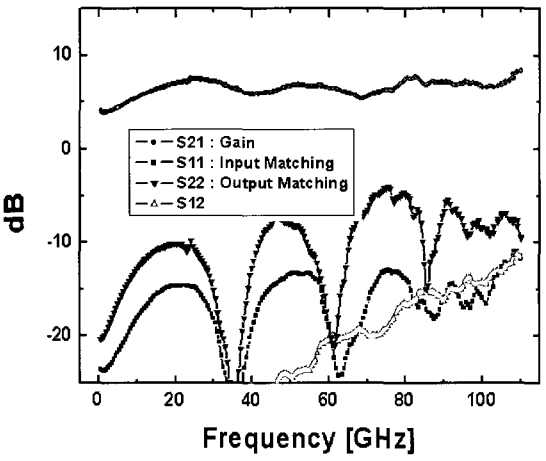
zero gain with - 6 dB/octave slope, an estimation of 426 GHz was achieved for f_T. This result indicates excellent InGaAs nano-HEMTs with little short channel effects without the aid of state-of-the-art e-beam lithography equipment. Fig. 8 shows bias dependent f_T and G_m characteristics as a function of V_{GS} at the V_{DS} of 0.5 V. It is clear that very excellent DC and RF characteristics could be maintained even at the very small V_{DS} of 0.5 V.

IV. Application to Millimeter-Wave MMICs

Increasing efforts are currently being made to develop ultra-high-speed ICs with nanoscale HEMTs. We have developed the device technologies for InGaAs HEMTs on InP as well as MHEMTs on GaAs for high speed ICs. We designed and fabricated W-band analog MMICs using 60 nm $In_{0.53}Ga_{0.47}As$ HEMT technology [9]. Various W-band MMICs have been built with the developed MHEMT technology.



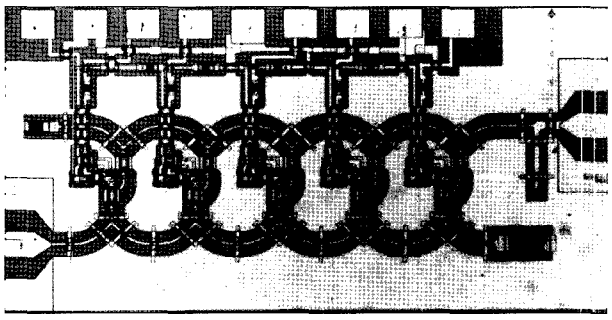
(a) Schematic of the distributed amplifier



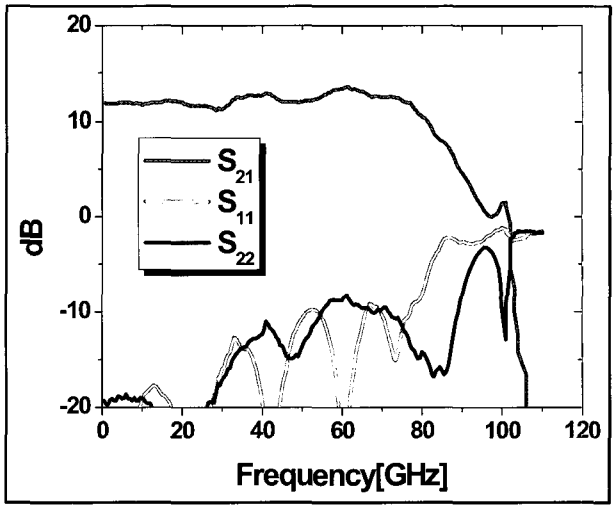
(b) measured performance

Fig. 9. Ultra-wide-bandwidth 60nm InGaAs HEMT distributed amplifier MMIC.

Ultra-wide-bandwidth distributed amplifier CPW (coplanar wave-guide) MMICs have been successfully developed by 60nm gate length InGaAs HEMT technology, in whuch 60nm gate was defined by previously mentioned Si_3N_4/SiO_2 sidewall process. The 60nm devices exhibited good DC and microwave characteristics of V_{th} = -0.65 V, breakdown voltage = -4.1 V, and extrinsic $G_{m,max}$ = 1.15 S/mm. To improve the uniformity and yield of HEMTs, the cap layer of device was selectively wet etched by the solution of succinic acid and hydro-peroxide. The photograph and the measured s-parameter of the fabricated distributed amplifier are shown in Fig. 9. By cascading six cascode connected HEMT stages, 6.6 dB small signal gain up to 110 GHz was obtained. W-band CPW distributed amplifier MMICs has been also developed with low-cost 100nm MHEMT technology with Ar plasma surface treatment. As shown in Fig. 10, excellent characteristics such as 12.45dB small signal gain and 3dB bandwidth of 82.5GHz were realized by cascading 5-stage cascade connected HEMT stages.

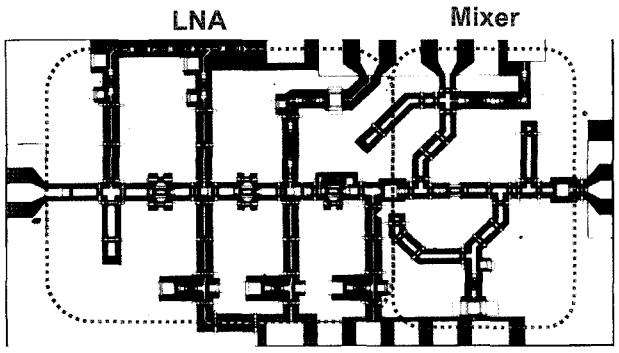


(a) Chip microphotograph

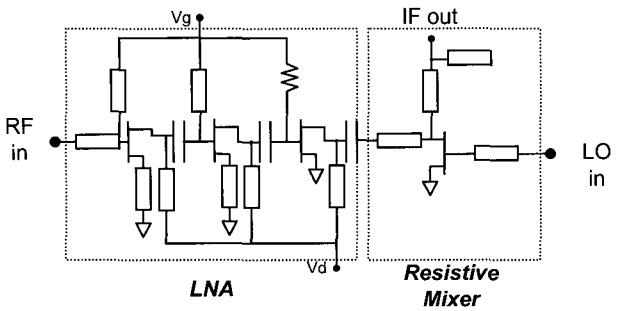


(b) measured performance

Fig. 10. W-band 100nm MHEMT distributed amplifier.



(a) Chip microphotograph



(b) Schematic of receiver sub-block MMIC

Fig. 11. 77GHz Receiver Sub-block MMIC.

To improve the driver safety, about 100 million automotive radars [10] are expected to be installed by 2010. We designed and fabricated W-band CPW MMIC chipsets for car radar applications with developed 100nm MHEMT technology. Low noise receiver sub-block MMIC was built with 3 stage LNA and resistive mixer, as shown in Fig. 10 with the chip size of 2.5 x 1.25 mm^2. Resistive mixer was chosen for FMCW radar due to its good low frequency noise characteristics despite of high conversion loss. The measured conversion gain of receiver sub-block was higher than 11dB at 77 GHz RF and 500 kHz IF. Transmitter sub-block MMIC was also built with driver stage amplifier and power stage amplifier, with the chip size of 2.5 x 1 mm^2, the measured small signal gain higher than 15dB for 70-78 GHz, and the output power of 10dBm at 77 GHz.

V. CONCLUSIONS

In summary, various nano-patterning techniques have been successfully developed for nanometer scale InGaAs HEMTs, such as sidewall-gate process, resist thermal flow, and sloped RIE etching method. Applying these methods to the device fabrication, we were able to succeed in making 30nm $In_{0.7}Ga_{0.3}As$ HEMTs with excellent f_T of 426GHz. Based on nanometer scale InGaAs HEMT technology, several millimeter-wave MMICs have also been successfully fabricated, such as 77 GHz MMIC chipsets for automotive radar application. With further device optimization, InGaAs HEMTs could well be the choice of technology for the next-generation ultra-high-speed integrated circuit applications.

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