Manufacturing of GaAs MMICs for Wireless Communications Applications

Wu-Jing Ho, Joe Liu, Hengchang Chou, Chan Shin Wu, Tsung Chi Tsai, Wei Der Chang, Frank Chou, and Yu-Chi Wang

***Abstract*—Two major processing technologies of GaAs HBT and pHEMT have been released in production at Win Semiconductors corp. to address the strong demands of power amplifiers and switches for both handset and WLAN communications markets. Excellent performance with low processing cost and die shrinkage features is reported from the manufactured MMICs. With the stringent tighter manufacturing quality control WIN has successfully become one of the major pure open foundry house to serve the communication industries. The advancing of both technologies to include E/D-pHEMTs and BiHEMTs likes for multifunctional integration of PA, LNA, switch and logics is also highlighted.**

***Index Terms*—GaAs, HBT, pHEMT, Switch, Power Amplifier**

I. IINTRODUCTION

In the past year, global handset industry has experienced rapid growth of the demand. Early this year, market analysts ever optimistically predicted that handset demands would grow annually from 810M units in Y2005 to 1B units in Y2006 [1]. The projected compound annual growth rate is more than 15%. Furthermore, they predicted the handset demand would continue to grow rapidly in the next 2-3 years as part of the reasons that both low and high-end handsets are emerging into the marketplaces. The low-end handsets happen to be demanded in the densely populated developing regions while the high-end units are well received in the established industrial countries. Note that the low end handsets provide only the basic function to the users such as local cellular access, voice and possibly news flash services while the high end tends to provide multi-mode, multi-band and multi-function cellular phone services such as GSM/GPRS, CDMA/WCDMA, EDGE, WLAN, Bluetooth, GPS and Multimedia services.

It is noticeable that the increase of handset demands has led to significant demands of GaAs based MMIC chips and thus wafers. The actual increase of GaAs MMIC demands however, is more than that of handsets. This can be attributed to two major reasons described as follows. Besides the increase of handset demands itself, the high-end, high performance handsets have used more GaAs based MMIC components in the RF front-end modules (FEM) of cellular phone units such as HBT PAs, pHEMT antenna/TR switches, and multifunctional chips using E/D-mode pHEMT or BiFET (or BiHEMT). In addition, the high-end handsets have required high performance, low power drain, high integration level and small die size pHEMT switches, which have replaced conventional silicon PIN diode switches.

In view of rapid demand of GaAs MMIC components, the emerging WLAN technology has also contributed to a great part of it. The WLAN product was first attached or embedded in the personal computer product where it provides wireless internet services. Recently, WLAN has expanded its application scope to cellular phones,

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VOIP, home/office appliances and play stations. Both handset and WLAN prosperities have made the demand of GaAs MMIC chips to grow over 25% annually this year and expects to maintain 15-20% growth rate in the next 2-3 years. Note that the estimated total output of GaAs IC wafers delivered in Y2005 was 30,000 to 35,000, 6 wafers equivalent.

Since established in 1999, WIN semiconductors Corp. has grown as one of the largest pure play GaAs IC manufacturing foundry service companies in the world. To satisfy customer demands, WIN has developed over 15 technologies for customers to develop and produce their MMIC products. The technologies include two major branches- HEMT and HBT. HEMT portion contains high-end 0.15um pHEMT and mHEMT (ka-band or above, power and low noise), c-band to ku-band 0.5um high power, high linearity pHEMT and HFET, and multi-functionality e/d mode and switch pHEMT for commodity wireless product use (handset and WLAN). HBT portion mainly includes a variety of 2um HBT technologies for use as high power, high linearity and high ruggedness power amplifiers in handset and WLAN product applications and 1um HBT for high frequency power and VCO applications

To cope with high performance and low cost requirement for both HBT PA and pHEMT switch, WIN has optimized technologies from both process and epi areas. For instance, WIN developed an ultra- thin silicon nitride process to reduce MIM capacitor size in order to shrink effectively the total chip size. WIN optimizes the HBT epi structures in order to meet stringent ruggedness specification of handset PA. In this paper, we will focus on the discussion of both HBT PA and pHEMT switch technologies for handset and WLAN applications.

II. Manufacturing of InGaP HBTs for Wireless PA Applications

To meet the performance with low cost requirements for both WLAN and wireless handset power amplifiers applications a non-self-aligned InGaP HBT process (HBT2) has been developed and released for production at WIN Semiconductors, Co. This process implements total of 14 masking levels with additional optional Schottky diode layer to complete a two-level-metal interconnects, MIM capacitor, thin-film resistor and

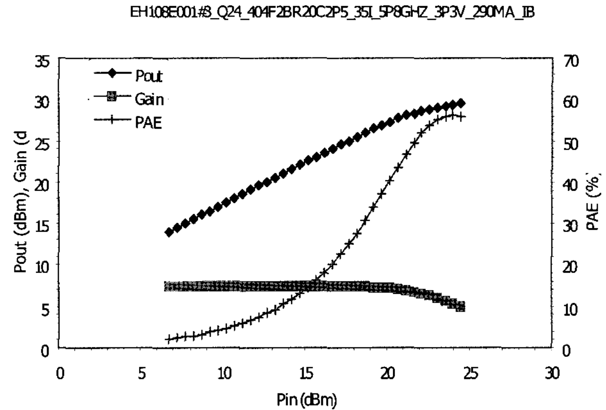


Fig. 1. Load-pull results of a 1536um^2 PA achieved over 59% power added efficiency at 5.8GHz.

Table 1. EVM of 3% has been achieved at 5.8GHz with 802.11a PA.

Company/ Product ID	Technology	Frequency (GHz)	P_{out} (dBm)	Gain (dB)	EVM	Power Consumption
Customer A	WIN InGaP HBT	4.9-5.85	P1dB > 26dBm	23 dB @ 5.25GHz & P_{out}=19dBm	3% for 64 QAM/54Mbps & P_{out}=19dBm	200 mA for P_{out}=19dBm at 5.25GHz
Customer B	WIN InGaP HBT	5.25	P1dB = 22.8 dBm	33.5 dB @ 5.25 GHz	NA	NA
Intersil (ISL3990)	AlGaAs HBT	5.25	P1dB = 20.2 dBm	29.6 dB @ 5.25 GHz	NA	NA
Hittite (HMC415LP3)	InGaP HBT	4.4-6.0	P1dB = 20 dBm	19	NA	200mA for P1dB=20dBm
Maxim MAX2841	SiGe HBT	NA	NA	23	4% @ P_{out}=18dBm	NA

100um thinned backside vias for power amplifier circuits manufacturing. A Pt sink-in refractory base metal scheme has been implemented to alloy through the InGaP layer to achieve the excellent contact resistance for the base contact. This alloy through contact scheme offers the simplicity for the process without relying on the relatively less controllable InGaP etching step to form the direct ohmic contact to GaAs base layer. Excellent specific contact resistance of 10^{-7} ohm.cm^2 has been achieved. A typical Au/Ge/Ni/Au ohmic metal is used for making the collector contact and the Boron-implant is used to effectively isolate the device. To further reduce the processing cost a refractory 1st level metal is making a direct emitter contact without the additional emitter ohmic metal contact step. TaN thin film resistor and 2000A of PECVD SiNx with 300pf/mm^2 MIM capacitor are implemented for this application. Cycle time of 28 days have been offered for the standard production delivery. This process has been released in production for more than four years with the volume of up to 2000 wafers per month capability for manufacturing both WLAN (802.11a,b&g) and handset (GSM and CDMA) PAs.

Excellent line yield of more than 90% has been achieved and one of the PA load-pull result at 5.8GHz is demonstrated in Fig. 1. Comparing with other technologies offered for WLAN PAs manufacturing WIN's performance advantage is listed in the Table 1.

To meet further higher performance especially on the higher VSWR ruggedness and chip size reduction thus lowering the cost an advanced process (HBT3) has also been developed and released in the production line [2]. The major advancement in this process is to achieve robustness withstanding higher VSWR ruggedness as required by the handset PAs applications. This process implements more advanced epitaxial structure designs with higher on-state breakdown characteristics for highly saturated power GSM PA and high linearity CDMA PA applications. Epitaxial structures with different safe-operation-area (SOA) measured when the current collapse occurs have been characterized and their SOAs are shown in Fig. 2. Epitaxial structure B was selected for the baseline release for GSM PA applications as it offers higher SOA with demonstrated power performance. Table 2 lists the device parameters with three selected epitaxial structures for targeted WLAN, CDMA and GSM applications.

This advanced process directly places the 2nd metal on top of the emitter fingers and also shunts the emitter fingers from unit device to device for the typical output power array layouts. The shunting essentially improves the device thermal characteristics and enhances the device performance. Fig. 3 shows the fabricated device schematics with 2nd metal shunting configuration on a three-emitter finger device. Relatively larger device size

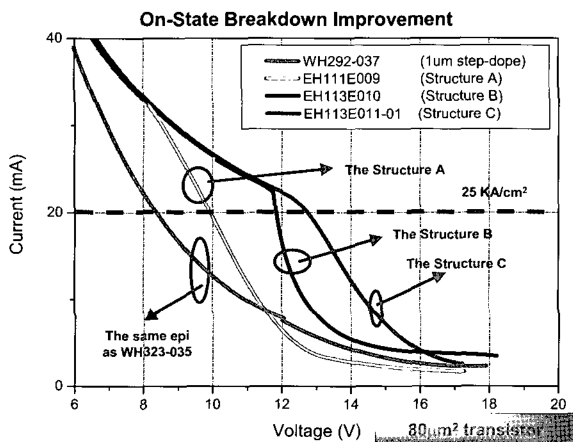


Fig. 2. SOA measurements from the 80um^2 devices fabricated with various epitaxial structures.

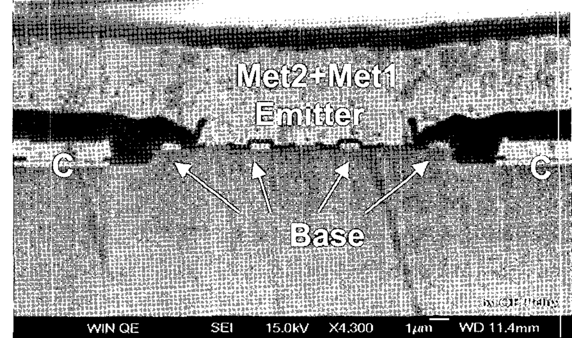


Fig. 3. SEM of a fabricated HBT device cross-section with three-emitter fingers and shunted with 2 um emitter metal.

Table 2. Device Parameters from Various released technologies at Win.

Parameter Description	Param_ID	Unit	HBT2 (15V) H02U-00	HBT3 WLAN H02U-01	HBT3 CDMA H02U-31	HBT3 GSM H02U41
Current gain cutoff frequency @ Vce=3.6V and Ic=20mA	ft	GHz	35	35	31	31
Maximum frequency of oscillation @ Vce=3.6V and Ic=20mA	fmax	GHz	100	100	110	110
C-B Junction Breakdown Voltage @ 1mA/mm	BK_CB	V	22	22	27	30
E-B Junction Breakdown Voltage @ 1mA/mm	BK_EB	V	9	9	9.5	7
E-C Junction Breakdown Voltage @ 1mA/mm	BK_EC	V	15	15	16.5	17
DC Current Gain@ 1mA	BT_1m	N/A	75	75	70	75
CM-M1 MIM Capacitor Unit Capacitance @1MHz,10V	CP_CM_10	pF/mm²	300	300	300	300
M1-M2 MIM Capacitor Unit Capacitance @1MHz,10V	CP_M2_10	pF/mm²	150	600	600	600
Isolation Current @ 20V	IS_DEV	nA	25	25	25	25
Base Sheet Resistance @1mA	RS_PW_B2	ohm/sq	195	195	190	185
Collector Sheet Resistance @1mA	RS_PW_C2	ohm/sq	15	15	15	16.5
Emitter Sheet resistance @1mA	RS_PW_E	ohm/sq	40	40	36	36
TFR Sheet Resistance @1mA	RS_PW_TR	ohm/sq	50	50	50	50

Test transistor: 2um x 20um x 2 emitter area

is implemented as a unit cell for making GSM PA power output arrays as it could significantly reduce the number of units required for producing sufficient power with relatively more compact size.

To further compact the size for PA application additional polyimide layer as a conformal coating layer has been added in between the two metal interconnects to planarize the circuit topology and allows the 2nd metal interconnect directly connects to the active device in any direction without encountering the unfavorable GaAs etching slope issue. This additional layer will improve the 2nd metal continuity crossing over the thick 1st metal line and ensure its current handling capability. The polyimide layer electrically separates the output bus line and ground plane with the backside via connected and allows the direct overlap of these two layers to compact the chip size. Another chip size reduction by up to 20% is through the development and release of the thinner nitride of 1000A for the MIM and stacked capacitors.

To overcome the intrinsic HBT's thermal collapsing issue, one of standard approaches is to implement dc resistor on emitter or base and rf resistor on base in series with feedback capacitor to increase the onset of the thermal collapsing and reduce the thermal coupling between unit cells used in the output stage array. The use of the ballastors could increase the usable power but with minor penalty in the drop of the rf gain and those values could be optimized to achieve the best results to meet both ruggedness and performance requirements [3]. To demonstrate its advantage of the newly released technology a macrocel with 11520um^2 emitter area is designed as shown in Fig. 4. A much higher than 12:1 VSWR ruggedness at 5V and phased to all angle without spurious has been achieved at 37 dBm output power and its power performance is shown in Fig. 5. The macrocell ruggedness performance comparison with the old process (HBT2) is listed in Table 3. Excellent rf performance and circuits ruggedness have been achieved for the manufacturing of EDGE, quad band GSM/GPRS and GSM PAs. The clear HBT3 advantage over the HBT2 for the ruggedness improvements could be demonstrated from the feedback of Wavics' CDMA designs. Comparing with the same design the PA with new process technology could sustain more than 6.2V under 10:1 VSWR ruggedness condition and its input power could be increased from 5mW to 15mW without failures [4].

Table 3. Ruggedness performance comparison between the devices of a 11520um2 emitter area fabricated with HBT3 technology and HBT3 technology.

Test condition: freq.=900MHz, VCE=3.6V, Quiescent Current=200mA, Pout=35dBm

Technology	Code	Breakdown (BV_{CEO})	Power performances			Ruggedness Performance	
			Pout (dBm) MAX	Linear Gain (dB)	Peak PAE (%)	C.W Mode	C.W Mode Stability under Load Mismatch
HBT2	H02U-00	15V	36	15.8	60	Failed at 3.6V, VSWR 3:1	NA
	H02U-10	20V	35.77	15.7	58	Pass 3.6V, VSWR 12:1 Failed at 5V, VSWR 3:1	Spurious observed at VSWR 6:1
HBT3	H02U-41	18V	35.38	15.28	60	Pass 5V VSWR 12:1 (Pout=37dBm at 5V matched)	Below -70dBc

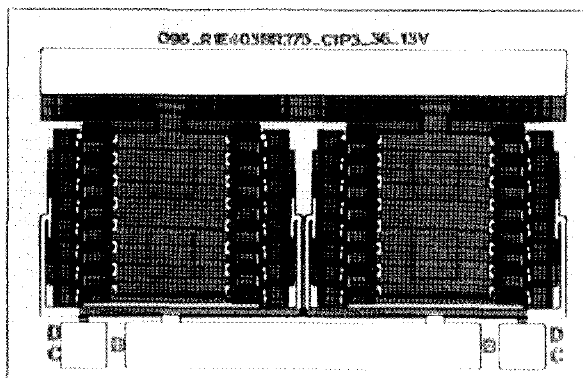


Fig. 4. A macrocell has been designed and fabricated to demonstrate the ruggedness improvements with the devices fabricated in HBT2 and HBT3.

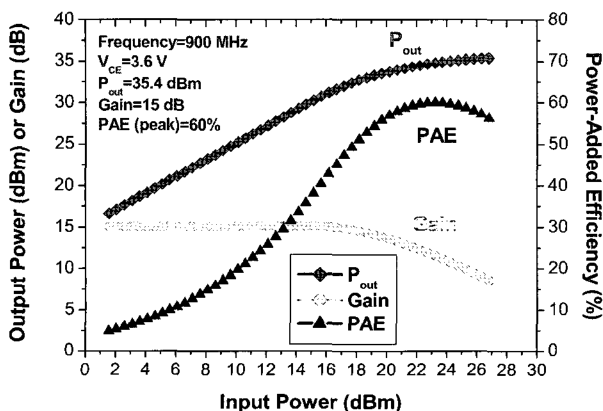


Fig. 5. Higher ruggedness under VSWR of 12:1 at 5V and it power performance has been achieved on a macrocell PA with 11520um^2 emitter area.

III. MANUFACTURING OF pHEMTs FOR WIRELESS SWITCH APPLICATIONS

Duplexing of wireless transmission and reception is often achieved with solid state switches. The demand for low battery drainage and low cost has seen pHEMT switches to replace PIN diode switches in mobile devices. More recently, the need for advanced multi-throw pHEMT switches emerged as one of the key components in the integration of several PA's and receivers into multi-mode cell phones. This expanded need requires low insertion loss and high isolation from a switch while keeping leakage current and non-linear characteristics be minimized. The pHEMT technology WIN has developed strikes a balance between three aspects of manufacturing-performance, cost, and reliability, to meet the present and near future applications in mobile and handheld devices.

The layout of a demonstration SP2T pHEMT switch is shown in Fig. 6. The features of a typical PHEMT switch that can be seen here are the stacking of gates, the use of high resistivity resistors for gate isolation, and the absence of backside via hole [5].

Gate stacking is an approach to isolation of high power RF when the DC control is from a low voltage supply such as in a cell phone. Stacking of gates is achieved by using multiple-gate transistor or by connecting several

transistors in series. The multiple-gate approach [6] has the advantage of a smaller chip size while the serial connection approach has higher isolation. A mix of both is used for optimized result.

An SEM of the multiple-gate structure is shown in Fig. 7. This shows three 0.5um gates meandering between the 5um drain/source ohmic metal comb-like structure.

The clean definition of multiple gate lines is the key to a high yield switch process. The spacing between gates is set to 1.5um to keep Ron low and isolation high. The diagram in Fig. 8 highlights the key dimensions and performance parameters.

The key parameters including pinch-off voltage, IDSS, and gate breakdown are monitored in the fabrication process. The list in Table 4 shows their nominal value. In additional to the baseline resistor and MIM capacitor as listed, options are provided for resistors with 600 ohm/sq sheet resistance and capacitors with 600 pF/mm2.

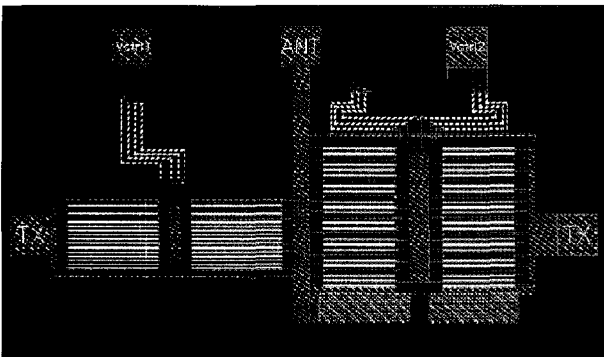


Fig. 6. Layout of a SP2T PHEMT switch designed as a demonstration vehicle.

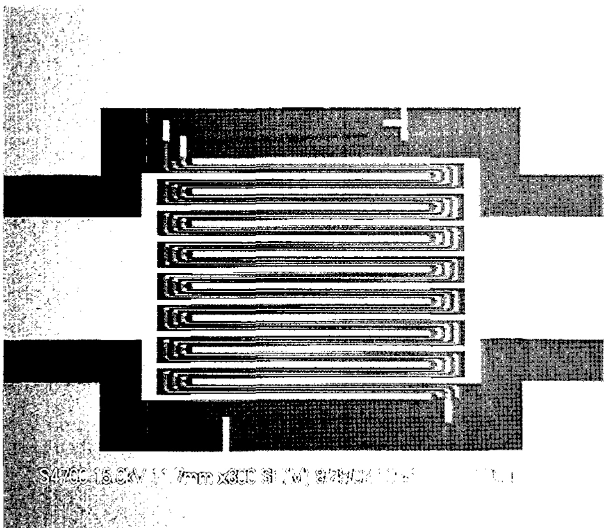
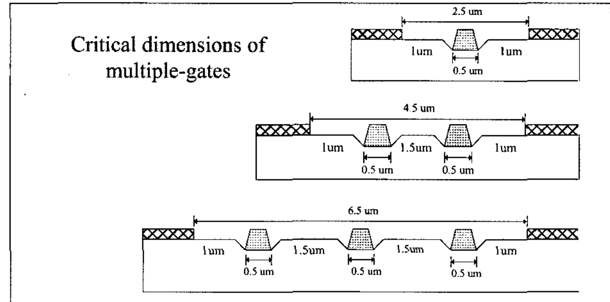


Fig. 7. SEM of quadruple gate fingers.



Gate Fingers	Ron (Ohm-mm)	Insertion Loss (dB) at f=1 GHz	Isoaltion (dB) at f= 1 GHz
1	1.6	0.25	20
2	2.2	0.4	25
3	2.8	0.5	30

Fig. 8. Critical dimensions designed for multiple-gates.

Table 4. The nominal values of critical parameters measured for the device with 2 gate fingers of 0.5um gate length and 75um width.

Parameter Description	Unit	Value
Extrinsinic Transconductance (GM_PEAK)	mS/mm	330
Gate Voltage of peak GM (V_GMPEAK)	V	-0.24
Maximum Drain Current (IDmax) @ Vds= 3 V	mA/mm	375
Drain Saturation Current (Idss) @ Vgs = 0 V	mA/mm	235
Gate-Drain Breakdown Voltage @ I_{GD}=1mA/mm	V	16
Pinch-off voltage (Vto) @ Ig=1 mA/mm	V	-1.0
Turn-on resistance (Ron)	ohm-mm	1.6
Cut-off frequency (ft) @ Vds=1.5 volt	GHz	32
Epi. Sheet resistance	Ohm/sq.	165
MIM capacitor with 1000A PECVD SiNx	dB	300
Interconnect Crossover		SiNx

Also monitored in the process is the gate reverse leakage current. The typical gate leakage current of no more than 100nA/mm at -5V allows switches to be designed with a few uA of gate current in operation. The non-linear behavior of a switch in the off-state comes from the reverse gate current and therefore a low gate

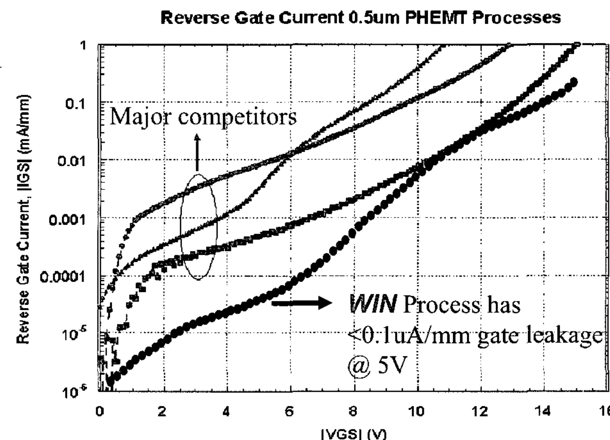


Fig. 9. Lower gate current of PHEMT processed at WIN.

Table 5. RF performance of the switch measured in the transmit state at GSM power level.

GSM SPDT Switch typical performance Freq ~900MHz, VC=2.5V		T-Comp.	*WIN*
TX Insertion Loss (dB)		0.4	0.3
TX 2nd Harmonic (dBc)	Pin=28 dBm	-81	-93
	Pin=35 dBm	-75	-82
TX 3rd Harmonic (dBc)	Pin=28 dBm	-84	-84
	Pin=35 dBm	-75	-78
Control current		--	< 1uA

current would result in low harmonic generation and high ACPR for the switch [7]. The chart in Fig 9 shows the Gate current of the PHEMT process at WIN. This low current results in a reduced harmonics of better than 75dBc for the demonstration SP2T switch. Table 5 shows the RF performance of the switch in the transmit state at GSM power level.

The Switch process uses 6 mask layers in all and they are all for the front side of the wafer. There is no mask required for the backside since there is no backside metallization and via holes in the switch process. For the front-side, the ohmic contact layer defines the drain/source for the transistors, and the mesa isolation layer defines the active channel area as well as the mesa resistor. Mesa isolation is done with ion implantation. The gate layer defines the gate metal as well as the gate recess etch. The process uses a single gate-recess to achieve low on resistance with optimized breakdown voltage of 16 volts at 1mA/mm reverse gate current. The gate layer also defines the bottom metal of the MIM capacitor. After the gate metal step, the device is

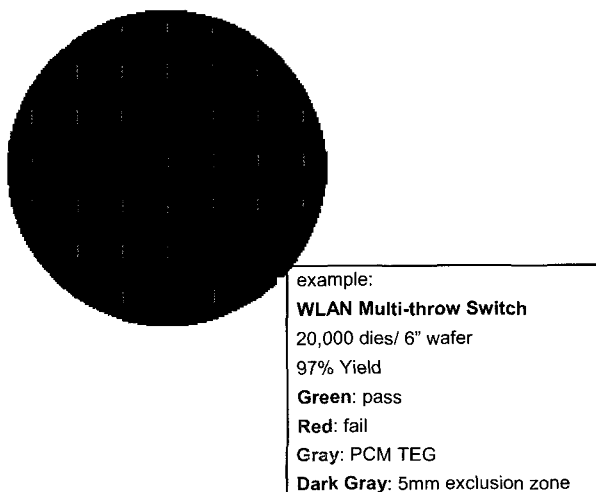


Fig. 10. A typical 97% yield result of a WLAN multi-throw switch fabricated at WIN.

passivated with silicon nitride and this nitride is also used as the dielectric for the MIM capacitor. The via opening in the nitride layer allows a top metal to contact the gate metal and this via opening also requires a mask layer. The next mask layer is used to define the top metal. Then the wafer is covered with protection silicon nitride. Finally, the last mask layer creates opening in the protection nitride for the contact pad and the die street.

For known good die manufacturing, 100% DC and/or RF test can be applied to the whole wafer before die singulation. The test produces a die map tabulated for the inker and the subsequent packaging process. A typical result can be seen in Fig. 10.

In the figure, the red color identifies the fail dies and the green ones are good. The PCM area is shown in grey. The 5mm exclusion zone at the edge of the wafer is the keep-out region.

IV. MANUFACTURING QUALITY CONTROL

WIN utilizes high-throughput, highly automated modern processing tools to produce high quality, low cost HBT/HEMT MMICs. Short cycle time manufacturing is achieved in a dedicated 6-inch GaAs processing line aided by the application of computer integrated manufacturing (CIM) technology, Statistical process control SPC techniques, and quality assurance discipline. A technical review board (TRB) operates to ensure process control and continual engineering improvement. WIN's quality system has been audited by customers and has been certified for QS9000/ISO9001 quality certificates.

WIN's HBT/HEMT MMICs are fabricated in State-of-the-art clean room with class one mini-environment, highly automated, cassette- to-cassette 6" manufacturing tools. Our CIM system is cable to perform real-time shop floor management for planning, scheduling, dispat- ching, and reporting. It could execute data collection and integration with on-line SPC and Fab/equipment automation. SPC activity includes automatic rule checking and violation detection, with statistical data analysis for control limit and process capability. Routine SPC review is performed for continual process improvement. Documentation is

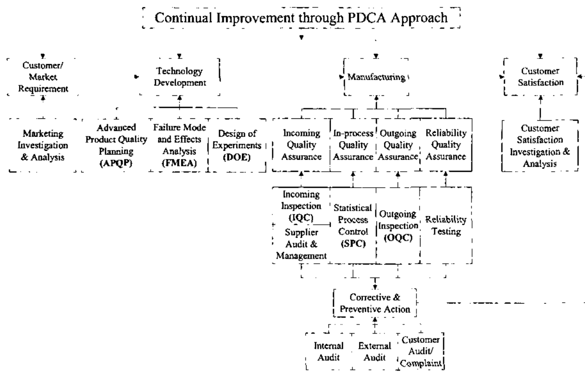


Fig. 11. WIN's quality system.

controlled and updated for process and equipment operation instruction (OI) and standard operation procedure (SOP). Internal quality audit is pursued for corrective action and continual improvement.

WIN's quality is measured by Customer satisfaction, and exists in the processes that achieve it. We commit a dedication to manufacturing innovation and technology development to provide a superior, compound semiconductor device and integrated circuit manu facturing foundry service. This is achieved by a constant pursuit of perfection demonstrated by providing high-quality products characterized by the employment of "Plan→Do→Check→Act" cycles for continuous improvement. WIN has received the QS-9000 and ISO 9001:2000 Quality Certifications and set the standard for GaAs MMIC Foundry Service Industry (Fig 11).

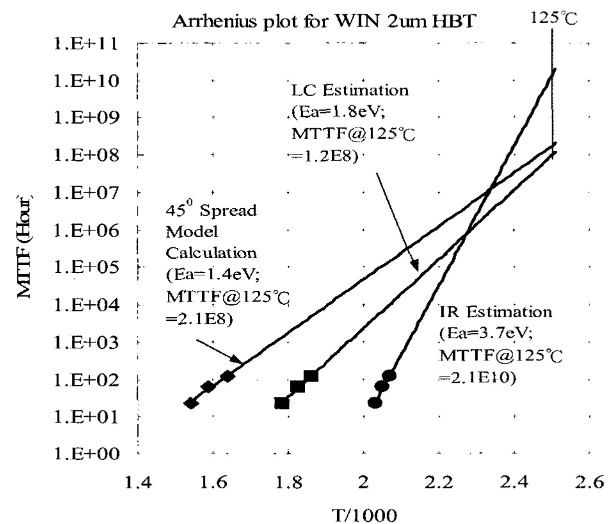
V. RELIABILITY

WIN's reliability assurance testing is to assure high-level device performance through- hout the intended life of the devices and products. Each manufacturing phase is subject to continuous review, analysis, and evaluation to ensure quality and reliability. Our reliability system is based on three important sources of reliability evaluation, including the Release qualification tests, Routine monitor and conformity tests, and Failure analysis.

WIN's reliability programs begin prior to a new process technology becoming available. Each new technology must pass a rigorous qualification procedure based on some of the highest industry standards before it is released to mass production. Table 6 shows a typical reliability test plan to qualify a new process technology. Once in production, every process is constantly

Table 6. WIN's reliability test plan to qualify a new process technology.

	Test Description	Purpose	Specification – Method or Conditions
HTOL	Bias Life test	Determine the effect of bias and temp on the device over time	MIL-STD-883E Method 1005.8 , 500hours @ Bias & Ambient Temp. to 165℃
MTTF	Accelerate Life test	Determine the active energy, MTTF, and FIT rate	JEDEC JEP118
Environmental	1.THB	Determine the effect of temp & humidity on the device under bias.	JESD22-A101-B-1000 hr 85℃-85RH with Bias
	2.Temperature Cycle	Determine the effect of temp on material thermal mismatch.	JESD22-A104 Cond G -40℃ to +125℃ 1000 Cycles
ESD	1.HBM ESD Sensitivity	Determine the sensitivity of the device to levels of ESD.	HBM per MIL-STD-883E method 3015.7
	2.MM ESD Sensitivity	Determine the sensitivity of the device to levels of ESD.	MM per JESD22-A115



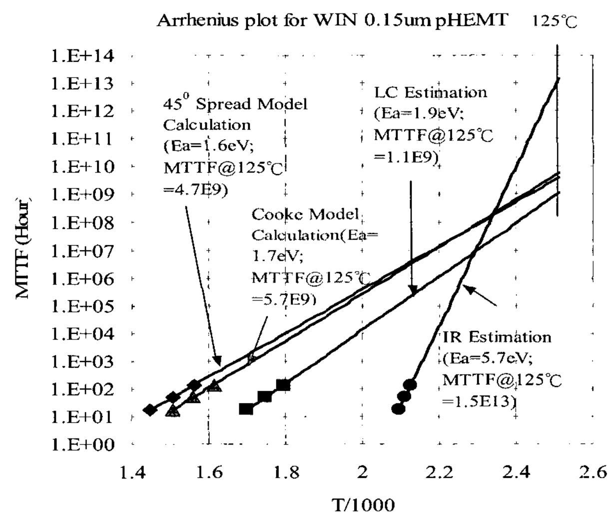


Fig. 12. Arrhenius plots to compare techniques for (a) WIN's 2μm InGaP HBT, and (b) WIN's 0.15μm power pHEMT.

monitored against a pre-determined set of standards. The results are published monthly.

To determine an accurate junction temperature (Tj) is extremely important for reliability test and lifetime estimation, which gives users critical knowledge of operation condition and device life. WIN has demonstrated several techniques for Tj estimation and compared their effects on the reliability life test results through devices fabricated at WIN's 6-inch GaAs foundry. From the reliability results of Arrhenius plots, the 45° spread model WIN Semiconductors used to obtain Tj matched well with liquid crystal thermography (LC) and Cooke model, but the infrared microscopy (IR) shows its space resolution limitation on the small area devices (Fig. 12) [8, 9].

To determine the cause of device/product failures and propose corrective action Failure analysis is an important part of quality and reliability assurance. At WIN, scanning electron microscopes, diagnostic probe stations, optical microscopes, and many other instruments and techniques internally and through outsourcing to professional FA laboratories /companies are used to perform failure analysis on devices/products.

VI. Developments of Multifunctional Integration Technologies

Density improvements with the die size reduction and performance enhancements are our primary focuses to release the 1st generation GaAs IC processes for the foundry services. As the wireless industry is moving toward more data and internet-enabled architectures more advanced process with multifunctional integration capabilities will be very significant to drive its applications and markets. To advance the processes for the multifunctional integration WIN has released an E/D-pHEMT process by adding an E-mode Schottky gate to the existing switch D-mode process for the integration of switch and low noise amplifier application with logic capability. Win is also in the process to add the HBT functionality into the E/d-pHEMT process to complete the BiHEMT integration with high yielded HBT PAs pHEMT switches and E-mode pHEMT LNA capability. The developments of the integration technologies for the entire system-on-chip RF front-ends will potentially open up more marketing opportunities for the wireless communication industry.

VII. Summary

Win Semiconductors has successfully released two major technologies to serve as a pure open foundry service house to address the PA and switch markets for handset and WLAN applications. High performance and low cost requirement is the key driving force for the process developments and releases. Under the stringent quality control numerous products manufactured at Win with the volume throughput of up to 1500 wafers per month and high than 90% line yield have been delivered to customers for to address the wireless communication component markets. The processes, key devices parameters, some of the manufactured PAs and switches performance and the quality control system including the device reliabilities are presented for the reference. The developments of the GaAs IC processes for multifunctional integration with E/D-pHEMT, and BiHEMT technologies are also highlighted for the advanced applications.

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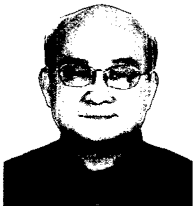
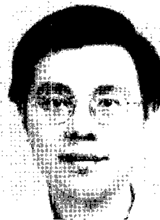


Wu-Jing Ho is the Vice President of WIN Semiconductors Corporation, Taiwan, the world's largest GaAs pure play open foundry service company. He has been involved in the technology developments and manufacturing of both silicon and compound semiconductors for over 25 years. Before joining WIN in 2004 Dr. Ho has co-founded Network Device Inc. in 1997 to offer the GaAs MMICs manufacturing foundry services. In year of 2000 NDI was successfully merged with Alpha Industries, Inc., then merged with Conexant Wireless Communication Division to form Skyworks Solutions Inc., in 2002. Dr. Ho has spent 10 years working on GaAs technology developments at Rockwell Science Center and 3 years working on silicon process developments at Rockwell Microelectronics Center since 1984. Dr. Ho earns his Ph.D degree in the Department of Materials Science and Engineering from University of Southern California, USA in 1981 and B.S degree in Chemistry from Nation Tsing Hua University, Taiwan in 1973. Dr. Ho has published more than 80 technical papers and holds several technical patents.

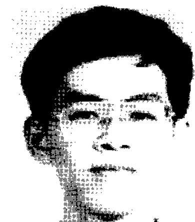
Joe Liu is the Vice President of WIN Semiconductors Corporation in Taiwan. He has been involved in GaAs MMIC and device technologies and manufacturing the compound semiconductors technology developments for over 20 years. Before joining WIN Semiconductors, he had served his career in GaAs MMIC industry, working for Sanders, Lockheed Martin on advanced microwave devices for 15years. Dr. Liu earns his Ph.D degree in Electrical Engineering from Penn State University, USA in 1986 and B.S. degree in Electrical Engineering from National Taiwan University, Taiwan in 1980. He has published more than 60 technical papers and received several patents.



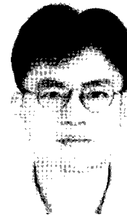
Hengchang Chou is the Associate Vise President of WIN Semiconductors Corporation. He has been involved in GaAs MMIC and Compound Semiconductor technologies and manufacturing for over 15 years. Before joining WIN Semiconductors, he had served his career at Microwave Technology Center in Agilent Technologies (Hewlett-Packard Company), USA. Dr. Chou earned his Ph.D. degree in Electrical and Computer Engineering from Georgia Institute of Technology, USA and M.S. and B.S. in Electrical Engineering from National Tsing Hua University, Taiwan. He has published more than 30 technical papers and publications. He is currently a member of IEEE.

Chan Shin Wu is the president/CEO of WIN Semiconductors Corporation, Taiwan, the world's largest GaAs MMIC pure play foundry service company. He has been involved in GaAs MMIC and device technologies and manufacturing for over 20 years. Before founding WIN Semiconductors, he had served his career in GaAs MMIC industry, working for AT&T Bell Laboratories at Murray Hill, Hughes Aircraft Company at Torrance, TI at Dallas and TRW at Redundo Beach consecutively. Dr. Wu earned his Ph.D. degree in Electrical Engineering from UC, San Diego and M.S. and B.S. in Physics from National Tsing Hua University and National Cheng Kung University, Taiwan, respectively. He has published more than 100 technical papers and received 12 patents. He is a senior member of IEEE, served as a member of honorary editorial advisory board of Solid-State Electronics and a member of the Bömische Physical Society.

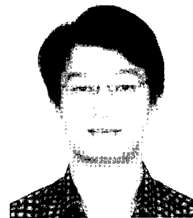
Tsung Chi Tsai is the Department Manager of HBT product technology development department of WIN Semiconductors Corporation, Taiwan, the world's largest GaAs MMIC pure play foundry service company. Dr. Tsai earned his M.S and Ph.D. degree in Materials Since and Engineering from Rutgers University in 1995 and 1999, and B.S. in Materials Science and Engineering from National Tsing Hua University, Taiwan in 1990.



Wei Der Chang graduated from the Department of Materials Science and Engineering (MSE) of National Tsing Hua University (NTHU), Taiwan with BS, MS and ph. D degree at 1990, 1992, and 1995, respectively. After graduation, Wei Der joined Synchrotron Radiation Research Center (SRRC) to develop X-Ray magnetic scattering, high reflection multiplayer analysis, and real-time X-ray study on thin film growth. Then Dr. Chang joined WIN semiconductor since 2000 and worked for epi wafer qualification and 6 inch wafer backside process development. Since 2002, Wei Der has developed 0.5 um pHEMT switch, 0.15 um mHEMT, and 0.5 um E/D-mode pHEMT technologies for mass production and was assigned as Manager of Fab engineering group since 2006, focusing on new process development and yield improvement.



Frank Chou is the quality engineering department manager of WIN Semiconductors Corporation. He has been involved in GaAs MMIC and Silicon semiconductor on relia- bility and failure analysis for 12 years. Before founding WIN Semiconductors, he had served his career in Silicon semiconductor industry, working for NANYA technology, FICTA technology at Taiwan. Frank Chou earned his Master degree in Electrical Engineering from Chung-Hwa university, Taiwan.



Yu-Chi Wang received the B.S. degree in physics from the National Central University, Chung-Li, Taiwan, R.O.C., in 1989, and the Ph.D. degree in materials science and engineering from Rutgers University, New Brunswick, NJ, in 1998. His doctoral dissertation concerned the device and circuit design, MBE growth, fabrication, and characterization of $In_{0.5}(Al_xGa_{1-x})_{0.5}P$ power HEMTs. In 1998, he joined Bell Laboratories, Lucent Technologies, Murray Hill, NJ, where he was a Member of Technical Staff, involved in the device design and process development of GaAs MOSFET, 0.1-μm InAlAs-InGaAs HEMTs, and high-performance InP DH-HBT for 40-Gb/s lightwave circuits. In December 1999, he joined the WIN Semiconductors Corporation, Taoyuan, Taiwan. He is currently the Associate Vice President of WIN's Technology Development Division.