Nanoscale Floating-Gate Characteristics of Colloidal Au Nanoparticles Electrostatically Assembled on Si Nanowire Split-Gate Transistors

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***Abstract*—Nanoscale floating-gate characteristic of colloidal Au nanoparticles electrostatically assembled on the oxidized surface of Si nanowires have been investigated. The Si nanowire split-gate transistor structure was fabricated by electron beam lithography and subsequent reactive ion etching. Colloidal Au nanoparticles with ~5 nm diameters were selectively deposited onto the Si nanowire surface by 2 min electrophoresis. It was found that electric fields applied to the self-aligned split side gates allowed charge to be transferred on the Au nanoparticles. It was observed that the depletion mode cutoff voltage, induced by the self-aligned side gates, was shifted by more than 1 V after Au nanoparticle electrophoresis. This may be due to the semi-one dimensional nature of the narrow Si nanowire transport channel, having much enhanced sensitivity to charges on the surface.**

***Index Terms*—Nanoparticle, SOI, Si nanowire, electrostatic assembly**

I. INTRODUCTION

Flash memories are one of the most widely manu factured nonvolatile memory structures in today's semiconductor industry. Nanoscale processing technology has enabled current flash type floating-gate memories to be integrated at densities far exceeding GBits per chip. To further increase device density and reduce device dimensions, many obstacles must be overcome. The capacitance per floating-gate should be reduced to minimize parasitic coupling between adjacent floating-gates, and capacitive coupling between the floating-gate and the channel should be enhanced [1]. A nanofloating-gate nonvolatile memory structure utilizing nanocrystals was first demonstrated by Tiwari et al, where they used Si nanocrystals with ~ 5 nm diameters on top of gate oxides grown using CVD[1, 2]. However, growth of Si nanocrystals on oxide surfaces yields a distribution of diameters leading to different island capacitances and gate coupling. Furthermore, due to the reduced nanoscale dimensions, energy level spacing between adjacent electron energy states may increase leading to reduced number of charge per nanocrystal and also higher than channel energy levels which may also increase leakage [3]. For large scale integration it is desirable to have uniform pre-synthesized nanocrystals for device-to-device reliability and reduced leakage and enhanced retention time [4]. Also a device structure where the Si transport channel is more strongly affected by the floating-gate charge than the conventional Flash EEPROM structure should be considered [5].

In this paper, we investigated the nanofloating-gate characteristics of colloidal Au nanoparticles electrostatically assembled on Si nanowire split-gate transistors (Fig.1). The use of pre-synthesized nanocrystals allows pre-selection of nano-floating gate diameters enabling uniform charge storage characteristics. The one-dimensional nature of the Si nanowire may enhance the

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gating effect of the charge stored on the Au nanocrystals, thereby enabling memory operation at reduced floating-gate densities. By using the nanowire and the side-gates as electrodes, nanocrystals are electrostatically assembled directly on the oxidized Si nanowire surface, giving self-alignment. Also in terms of process efficiency, electro static assembly of nanocrystals, compared to conventional surface functionalized nanocrystal assembly[4] or template assisted assembly[8] methods produced high density distribution of Au nanocrystals (~10^{11} cm^{-2}) at far less (2 min compared to several hours) processing time. We were able to achieve close to ~1.4 V shift in the depletion mode cutoff voltage of the Si nanowire conductance using 5 nm diameter Au nanocrystals at ~10^{11} cm^{-2} density. The results show that it may be possible to incorporate pre-synthesized nanocrystals on Si nanowires using electrostatic assembly for nano-floating gate memory operation.

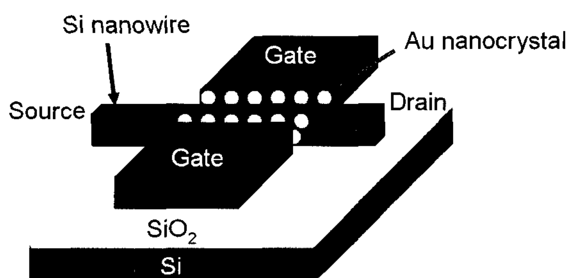

Fig. 1. Schematic diagram of the Si nanowire split-gate transistor with Au nanoparticle electrostatically assembled nanofloating-gate.

II. DEVICE FABRICATION

We used a highly n-type doped (10^{14} cm^{-2}) Si-on-insulator (SOI) wafer. The top Si layer is 70 nm thick with the oxygen implanted SiO_2 layer 100 nm thick. The implanted insulator layer allows electrical isolation of the transport channel from the side-gates. To define the 50 nm Si nanowire structure, electro-beam lithography followed by reactive ion etching(RIE) was performed. A 4% 950k poly(methylmethacrylate) (PMMA) was spin-coated at 500 rpm for 30 s on the wafer surface to act as the e-beam resist and dry etch mask. High resolution electron-beam lithography (70 kV, 10 pA, < 5 nm spot size) was used to define the self-aligned split-gate nanowire transistor pattern[5]. Then the pattern was

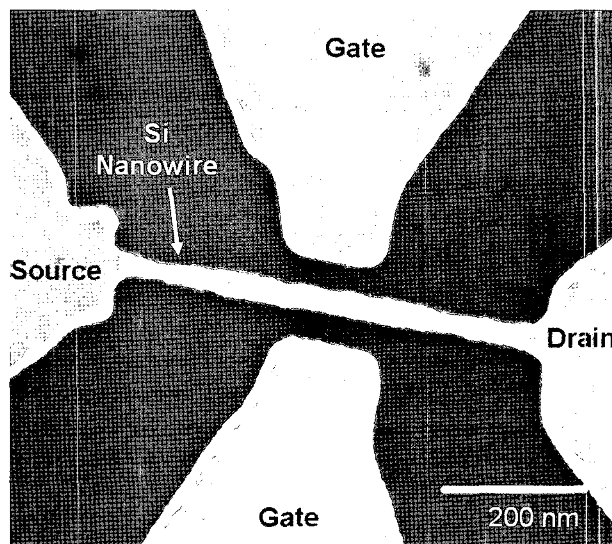

Fig. 2. SEM image of the Si nanowire device structure. The Si nanowire was 50 nm in average width with the narrowest region being 30 nm.

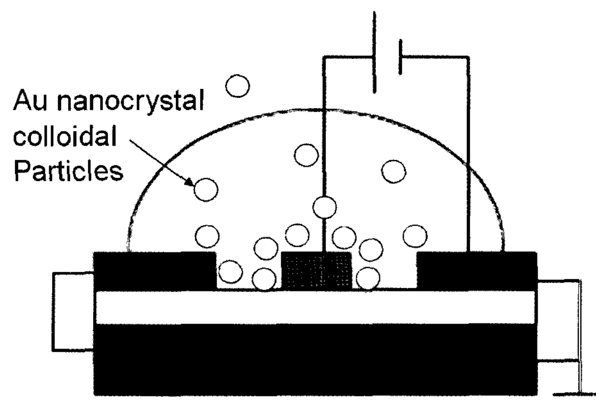

Fig. 3. Schematic diagram of the Au nanoparticle electrophoresis. Electrostatic field is applied between the side-gates and the Si nanowire channel.

transferred to the top Si layer by RIE[6]. RIE condition was 10 sccm, $SiCl_4$ at 300 W. The ~300 nm thick PMMA layer was enough to with stand the 30 s RIE process. SEM image of the Si nanowire split-gate transistor structure is shown in Fig. 2. It can be seen that the nanowire transport channel is ~ 50 nm and split-gates form ~50 nm gaps with the nanowire. Since the nanowire and the side-gate structures were fabricated in a single lithography step, the self-aligned side-gates pakes perfect alignment with the nanowire and the distance between the nanowire and the side-gates are identical on either wide. The colloidal Au nanoparticles with ~ 5 nm diameters were assembled on the top of the oxidized Si surface by dielectrophoresis. Using the Si

nanowire as the anode and the split-side gate and the substrate as the cathodes, 10 V dc electric-field was applied for ~ 2 min between the Si nanowire channel and the gates with a 0.4 μl of the Au colloidal nanoparticle solution dropped on the device structure (Fig. 3). This process time was considerably lower than self-assembly methods used to assemble nanoparticles on chemically functionalized structured surfaces, which requires more than 6 hours for the nanoparticles to assemble [3]. Fig. 4 shows an SEM image of 10 nm Au nanocrystals electrostatically assembled on Si surface. The top Si layer of an SOI wafer was etched to form a 2 μm wide wires. It can be seen that the Au nanocrystals were mostly deposited on the Si surface (with native oxide), with a far lower density on the SiO_2 surface. This selective assembly was due to the electrostatic field applied to the Si wire which allowed the negatively charged Au nanocrystals to be attracted toward the Si surface. There was a higher concentration of nanocrystals around the edges of the Si wires which may be the result of geometrical field enhancement.

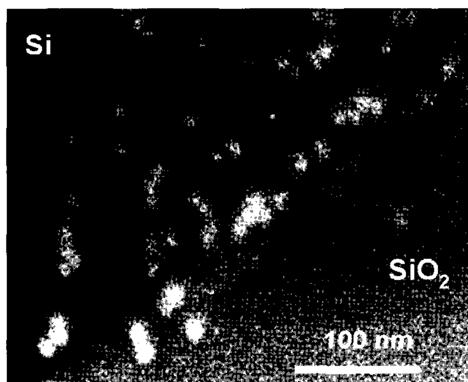

Fig. 4. SEM image of 10 nm Au nanoparticles electrostatically assembled on top of the Si surface. The SiO_2 surface was exposed by etching the top Si layer of an SOI wafer.

III. Measurement Results and Discussion

To evaluate the dependence of the Au nanoparticle characteristics are shown in Fig. 5. It can be seen that the backgate dependent onset of carrier depletion had shifted by ~ 0.2 V. Since the bare Si wire structure did not show noticeable hysteresis when measured without the nanocrystals, this was seen as evidence that the attached nanocrystals were acting as charge traps and were acting

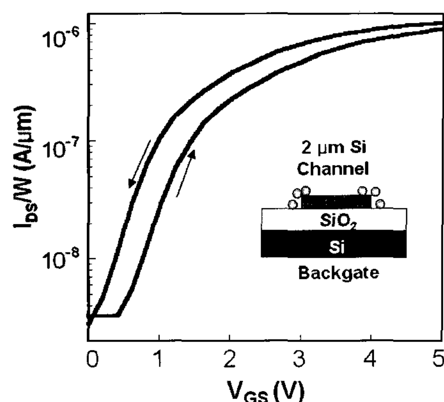

Fig. 5. Ttransfer characteristics of 2 μm wide Si channel with Au nanoparticle nanofloating-gates. The source-drain voltage was 2 V.

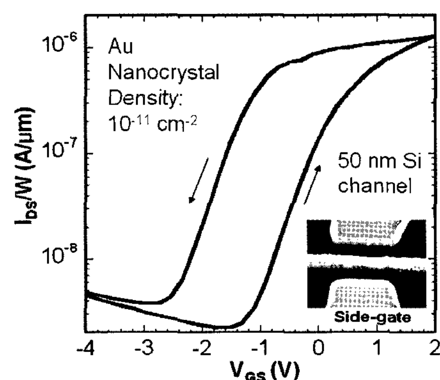

Fig. 6. Transfer characteristics of 50 nm Si nanowires with Au nanoparticle nanofloating gates. The source-drain voltage was 2 V. The nanocrystal density was $\sim 10^{11}$ cm^{-2}.

to deplete surface carriers from the Si wires. The transfer characteristics measurement results on the 50 nm Si nanowire split-gate transistor is shown in Fig. 6. The measurement results show that the depletion mode cut-off voltage was shifted from -1.2 V to -2.6 V resulting in a voltage shift of ~ 1.2 V indicating far enhanced charge coupling between the Au nanocrystals and the transport channel. This may be due to the one-dimensional nature of the Si nanowire, where increased ratio between channel surface area to channel cross section resulted in the charge states of surface assembled Au nanoparticles having enhanced scattering effect on the channel transport. Since the nanocrystals were exposed to the environment and also there is no way to ensure separation between adjacent nanocrystals the retention time of the Au nanocrystals were very pore at less than 1 s. To overcome this drawback, core/shell type nanocrystals may be more effective.[3] This may reduce percolation driven

leakage currents in the nanocrystal floating-gate resulting in longer retention times. Also utilizing structured templates for nanocrystal assembly along with electrophoresis, higher density assemble may be possible, which may increase hysteresis in the transconductance [8].

IV. SUMMARY

We have investigated the nanoscale floating-gate characteristics of colloidal Au nanoparticles electrostatically assembled on Si nanowire split-gate transistor surfaces. Electrostatic assembly produced 10^{11} cm^{-2} density Au nanocrystal assembly on charged surfaces at ~2 min process time, which was a significant improvement to existing methods. The 5 nm Au nanoparticles on the surface oxide of 50 nm Si nanowires enabled the cutoff voltage of the nanowire to shift by more than 1.2 V. The enhanced gating effect may be due to the narrow channel cross section increasing the gate dependent scattering.

ACKNOWLEDGMENTS

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