Low Voltage Program/Erase Characteristics of Si Nanocrystal Memory with Damascene Gate FinFET on Bulk Si Wafer

Jeong-Dong Choe*, Kyoung Hwan Yeo*, Young Joon Ahn*, Jong Jin Lee*, Se-Hoon Lee*, Byung Yong Choi*, Suk Kang Sung*, Eun Suk Cho*, Choong-Ho Lee*, Dong-Won Kim*, Ilsub Chung, Donggun Park*, and Byung-Il Ryu***

***Abstract*—We propose a damascene gate FinFET with Si nanocrystals implemented on bulk silicon wafer for low voltage flash memory device. The use of optimized SRON (Silicon-Rich Oxynitride) process allows a high degree of control of the Si excess in the oxide. The FinFET with Si nanocrystals shows high program/erase (P/E) speed, large V_{TH} shifts over 2.5V at 12V/10μs for program and -12V/1ms for erase, good retention time, and acceptable endurance characteristics. Si nanocrystal memory with damascene gate FinFET is a solution of gate stack and voltage scaling for future generations of flash memory device.**

***Index Terms*—FinFET, Si-nanocrystal, SRON(Si-Rich Oxynitride), flash memory device**

I. INTRODUCTION

The new storage node concept is required for dielectric and voltage scaling in non-volatile memories (NVM) to meet the reliability and performance requirements of future products. A Si nanocrystal flash memory devices has been recently proposed and extensively studied due to low power consumption, inherent scalability, smaller lateral leakage currents, and good endurance to program/erase cycles[1~8]. Si nanocrystals are used as charge storage elements embedded in the oxide layer between the control gate and silicon channel. One of the main challenges is producing uniform Si nanocrystals with high cell current.

For the purpose of these issues, we have fabricated the damascene gate Si nanocrystal FinFETs with optimized SRON process. Damascene gate FinFET has been considered as one of the most promising candidates to overcome the difficulties of CMOS scaling because of their good short channel effect (SCE) immunity and compatibility with the conventional process with high cell current[9]. Damascene gate process is also a simple way to overcome scaling limit because of its own merit such as easiness for metal gate application and clearness for gate etch burden[10]. SRON process is an attractive technique because it allows a high degree of control of the Si content in the oxide by simply changing the feeding gas ratio of O_2/SiH_4, post-annealing time, and temperature. We prepared SRON layer by newly employed Cyclic–CVD technique with N_2O/NH_3 gas.

II. EXPERIMENTS

The process sequence, schematic diagram, and process results for the fabrication of Si nanocrystal memory with damascene gate FinFETs on bulk Si wafer are shown in Fig. 1. Silicon wafer was prepared with conventional shallow trench isolation including fin trimming

Manuscript received Apr. 13, 2006; revised May 30, 2006.
* Device Research Team, R&D Center, Samsung Electronics Co., Kyungki-Do, KOREA,
** School of Information and Communication Engineering, Sungkyunkwan University, KOREA
E-mail : ivo.choe@samsung.com

processes. After the deposition of masking materials, damascene gate was patterned and its spacing was reduced by controlling the inner spacer thickness. And then, a 120nm-thick field oxide was anisotropically removed for fin formation followed by tilted and local channel implantation through the open window. After growing 3 nm-thick tunnel oxide layer, 5 nm SRON layer was formed with appropriate feeding gas ratio (O_2/SiH_4). Desired SRON layer and film thickness can be obtained by controlling feeding gas ratio and pressure. After deposition of 7 nm control oxide layer, SRON post-annealing was performed. High density ($\sim 7.5\times10^{12}/cm^2$) Si nanocrystal dots were successfully formed with the diameter of 1.5~2 nm. The N^+ polysilicon was deposited for control gate material. Gate CMP and silicon nitride removal process were followed. Thereafter, the fabrication was completed by performing tilted halo and SDE implantation, spike annealing, spacer formation, S/D implantation, and Co salicidation. Fig. 2. shows the TEM images of damascene gate FinFET structure with uniformly distributed Si nanocrystal dots embedded between tunnel oxide and control oxide layer. From Fig. 2., the newly fabricated devices have W_{fin}=30 nm and L_G=60 nm after the full process. Fin height is 120 nm. Total dielectric thickness including SRON layer is less than 15 nm. Nitrogen content in the SRON layer is about 18% from XPS analysis.

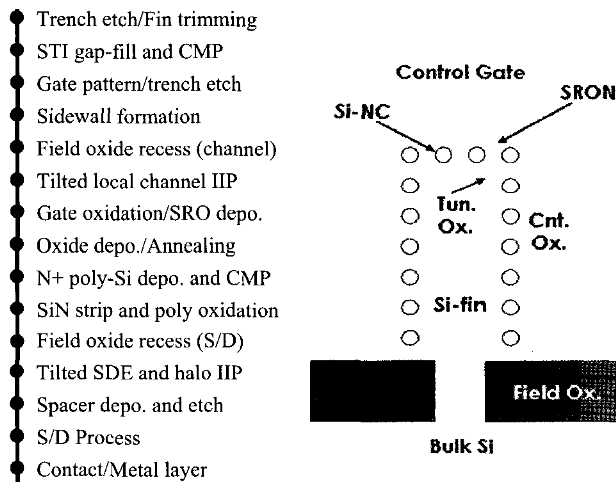


Fig. 1. Fabrication process flow and schematic diagram of damascene gate Si nanocrystal FinFET device.

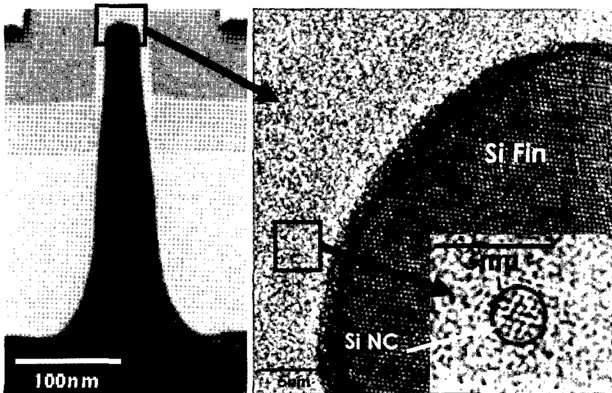


Fig. 2. TEM images of damascene gate Si nanocrystal FinFET device show the fin width of 30nm, tunnel oxide thickness of 3nm, and Si nanocrystal dot diameter of 2nm.

III. RESULTS AND DISCUSSION

The I_d-V_g characteristics of programmed and erased states of Si nanocrystal FinFET after 1, 10^3, 10^5 cycles are plotted in Fig. 3. It can be seen that threshold voltage shifts are over 2.5V after P/E cycles. The distance between the trap charge and the gate electrode is 7 nm, so that the number of electrons trapped in the Si nanocrystals was estimated to be $7.5\times10^{12}cm^{-2}$. From Fig. 3., it was found that the threshold voltage shift between the two states could be as high as 2.5V, sufficient for read operation of memory arrays. We calculated the number of stored electrons per nanocrystal dot (*f*) for this experiment as follows;

$$\Delta V_T = \frac{qfn_{nc}}{\varepsilon_{ox}}\left(t_{Box} + \frac{1}{2}\frac{\varepsilon_{ox}}{\varepsilon_{Si}}t_{nc}\right)$$

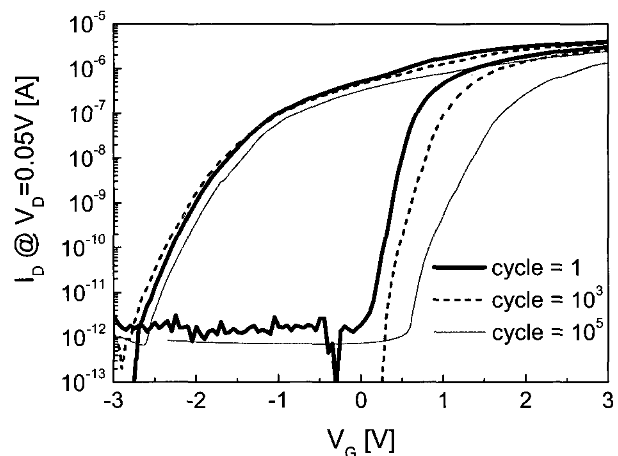


Fig. 3. Id-Vg characteristics after various P/E cycles. Threshold voltage shifts are measured over 2.5V after P/E cycles.

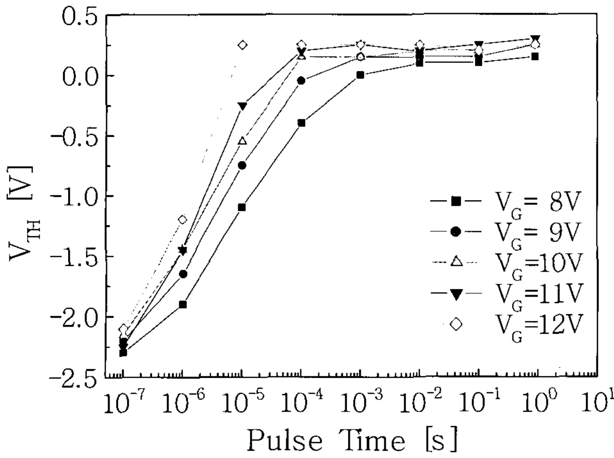


Fig. 4. Programming characteristics of FinFET structure show that threshold voltage shift of 2.5V was achieved with 12V/10μs program pulse.

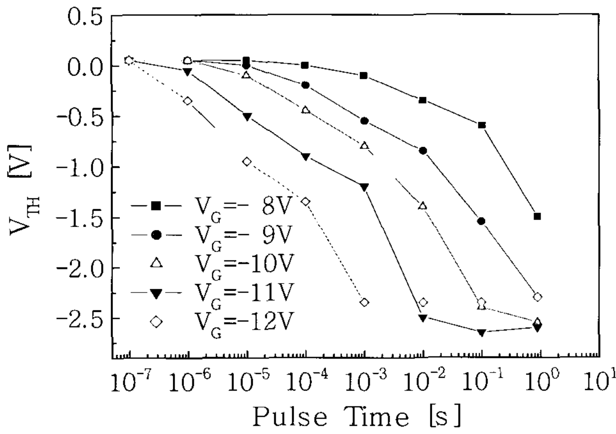


Fig. 5. Erasing characteristics of FinFET structure show that threshold voltage shift of 2.3V was achieved with -12V/1ms erase pulse.

where ΔV_T is the threshold voltage shift, q is electron charge, n_{nc} is dot density, f is an effective factor and means the number of electron charges per dot. t_{Box} is barrier oxide thickness between silicon nanocrystal and gate material. t_{nc} is the diameter of dot [4~6]. With H_2 alloying process we removed the interface trap of SiO_2/Si effectively. Calculated effective factor f for this experiment is 1.86 electrons/dot which is over 1. $f>1$ means a few of nc-dot/SiO_2 interface trap sites is existed due to surface roughness and non-uniform concentration. Therefore we have to reduce interface trap density in the nc-dot/SiO_2 interface to control threshold voltage shift effectively. Fig. 4. and Fig. 5. show the program and erase transient characteristics with various program/erase voltages from +8V/-8V to +12V/-12V. Program speed is 10μs at +12V with 2.5V V_{TH} shift and erase speed is 1ms at −12V with -2.3V V_{TH} shift, respectively. Threshold voltage shift saturates as the P/E time increases and also as the P/E voltage increases. Distributions of the threshold voltages for gate length with 100nm and 120nm measured in wafer level are shown in Fig. 6. The endurance characteristics were tested using 12V, 10ms program pulse and -12V, 100ms erase pulse at room temperature as shown in Fig. 7. Even with a 3 nm tunnel oxide thickness, Si nanocrystal FinFET shows good endurance to P/E cycles. Fig. 8. shows the measured retention time for various P/E voltages from +10V/-10V to +15V/-15V. There is no initial degradation of programmed threshold voltage, and V_{TH} window reduction is found to be less than 15% up to 10^5 s.

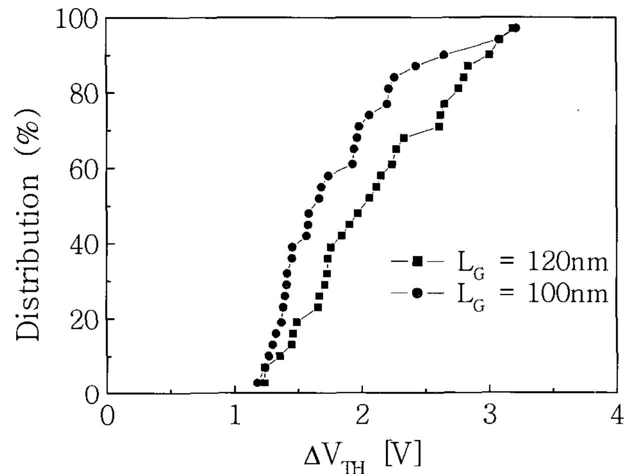


Fig. 6. Distributions of the threshold voltages for gate length with 100nm and 120nm measured in wafer level.

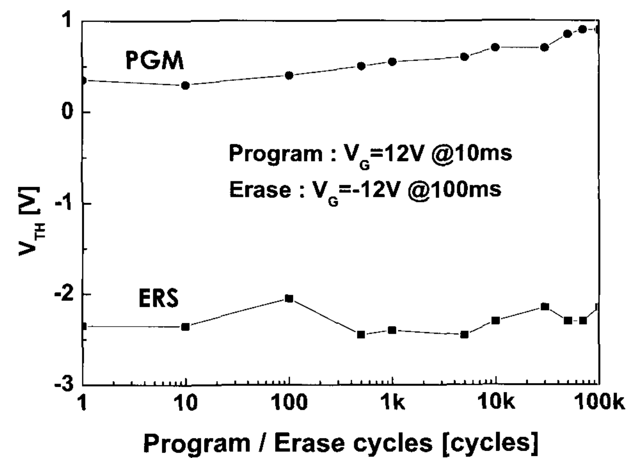


Fig. 7. Endurance characteristics show that it can reach 10^5 cycles with no degradation when tunnel oxide thickness is 3 nm.

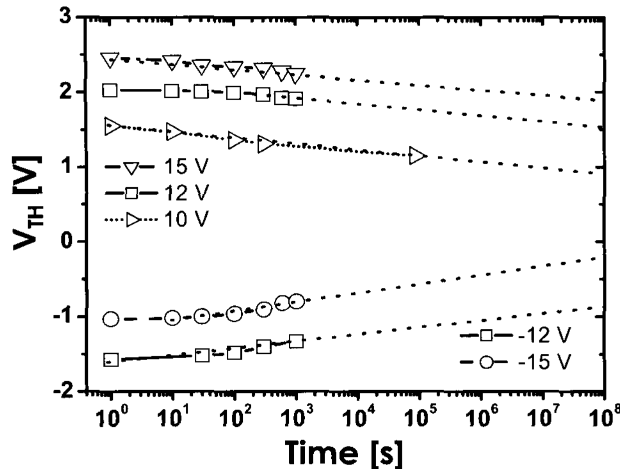


Fig. 8. Retention characteristics for various P/E voltages show that no initial degradation of programmed threshold voltage is found up to 10^5 s.

IV. CONCLUSIONS

We have demonstrated the Si nanocrystal memory with damascene gate FinFET for low voltage application. Density and size of Si nanocrystal dots can be controlled by SRON process. With this novel memory structure we obtained excellent characteristics in the threshold voltage shift, endurance and retention. We expect that Si nanocrystal memory with damascene gate FinFET is a solution of gate stack and voltage scaling for future generations of flash memory device.

REFERENCES

[1] K. H. Park, Y. Kim, T. H. Chung, H. J. Bark, J. Y. Yi, W. C. Choi and E. K. Kim, "Electrical and Structural Properties of Si nanocrystals Prepared by Ion-Beam-Assisted Electron Beam Deposition," *JKPS*, vol. 39, pp.283-286, 2001.

[2] Sung Kim, Hyung-Sun Hwang, Suk-Ho Choi and Kyung Joong Kim, "Nonvolatile Memory Properties of Thin Oxides with Single- and Multi-Layered Si nanocrystals Obtained by Ion Beam Sputtering," *JKPS*, vol. 48, pp.108-111, 2006.

[3] Jae Kwon Kim, Hea Jeong Cheong, Kyung Hwa Park, Yong Kim, Jae-Yel Yi, Hong Jun Bark, S. H. Bang and J. H. Cho, "Rapid Thermal Annealing Eect on Charge Storage Characteristics in MOS Capacitor with Ge nanocrystals," *JKPS*, vol. 42, pp. 316-319, 2003.

[4] Sandip Tiwari, Farhan Rana, Hussein Hanafi, Allan Hartstein, Emmanuel F. Crabbé, and Kevin Chan, "A silicon nanocrystals based memory," *Appl. Phys. Lett.* vol. 68, pp.1377-1379, 1996.

[5] De Salvo B., "How far will silicon nanocrystals push the scaling limits of NVMs technologies?" *2003 Electron Devices Meeting, IEDM '03 Technical Digest. IEEE International*, pp. 26.1.1-26.1.4 Dec. 2003.

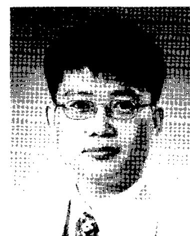
[6] Chungho Lee, Tuo-hung Hou and Edwin C. Kan, "Metal nanocrystal/nitride heterogeneous-stack floating gate memory," *2005 Device Research Conference Digest, DRC '05. 63rd*, vol. 1, pp.97-98, June 2005.

[7] Jong Jin Lee, Weiping Bai and Dim-Lee Kwong, "Dielectric engineering in nanocrystal memory devices for improved programming dynamics," *2005 Reliability Physics Symposium, Proceedings. 43rd Annual. 2005 IEEE International*, pp.668-669, April 2005.

[8] Brault, J., Saitoh, M. and Hiramoto, T., "Channel width and length dependence in Si nanocrystal memories with ultra-nanoscale channel," *Nanotechnology, IEEE Transactions,* vol. 4, issue 3, pp.349-354, May 2005.

[9] Chang Woo Oh, "Damascene gate FinFET SONOS memory implemented on bulk silicon wafer," *2004 Electron Devices Meeting, IEDM Technical Digest. IEEE International*, pp.893-896, Dec. 2004.

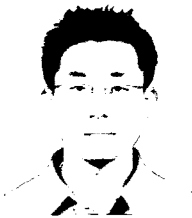
[10] Jeong-Dong Choe, Chang-Sub Lee, Sung-Ho Kim, Sung-Min Kim, Shin-Ae Lee, Shin, Y.-G, Donggun Park and Kinam Kim, "A 22-nm damascene-gate MOSFET fabrication with 0.9-nm EOT and local channel implantation," *Electron Device Letters, IEEE*, vol. 24, issue 3, pp.195-197, March 2003.



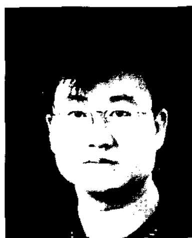
Jeong-Dong Choe received the B.S. degree from Yonsei University in 1992 and the M.S degree in materials science and engineering from Yonsei University in 1994. From 1994 to 1999, he worked at LG Electronics Co., Ltd., where he researched plasma processing. In 2000 he joined Samsung Electronics Co., Ltd. where he has been

involved in the development of DRAMs. His current major activity is focused on the development of technologies for nano-scale Flash memory device.

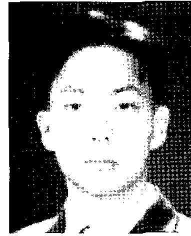
Kyoung Hwan Yeo received the B.S. degree in materials science and engineering from Pohang University of Science and Technology (POSTECH), Korea, 1992 and the M.S. degree in information and communication engineering at the Sungkyunkwan University, Korea, 2004. After graduation from POSTECH, he has worked at Samsung Electronics since 1995. He worked on the dry etch process development for DRAM, SRAM, and FLASH memory devices. His current research is the fabrication and characteristics analysis of new structure transistor, especially transistor with gate all around structure.



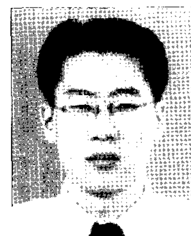
Young Joon Ahn received the B.S.degree in electrical and electronic engineering from Ajou University, Gyoung-gi, Korea, in 2001 and the M.S degrees in electrical and electronic engineering from at KAIST, Daejeon, Korea, in 2003. Since 2003, he has been with Samsung Electronics, Kyungki-Do, Korea. His research interests include nano scaled NVM cell structure and technology, reliability.



Jong Jin Lee received the B.S. and M.S. degrees in electrical and computer engineering from the Korea University, Seoul, Korea, in 1990 and 1992, respectively, the Ph.D degree in electrical and computer engineering at the University of Texas, Austin, TX, in 2005. His Ph.D study was for the Nanocrystal memory device using high-k dielectrics. Since he joined Samsung Electronics in 1992, he involved in Process Architecture team as a senior engineer for 64M and 256M DRAM development until 2001. After his Ph.D degree, he rejoined Samsung Electronics, where he is now a technical manager of Flash Device Research Group in R&D center. His current research interests are in the areas of deep submicron CMOS technology, novel high-k devices, and Discrete Trap Memories for the future Flash technology.



Se Hoon Lee was born in Seoul, Korea, on January 11, 1978. He received the B.S.degree in materials science and engineering from Korea University, Seoul, Korea, in 2003 and the M.S degree in materials science and engineering from at Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2005. In 2005, he joined Samsung Electronics, Kyungki-Do, Korea, where he has been engaged in the research and development of nano scaled NVM and DRAM cell structure and technology.



Byung Yong Choi received the B.S. degree in electronic engineering from Kyungpook National University, Taegu, Korea, in 1998. He received the M.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2000. He is currently working toward the Ph. D. degree at the same university and also with Samsung Electronics Company, Kyungki-Do, Korea, from 2004. His current research interests are nanoscale CMOS devices, and non-volatile memories (NVMs) using discrete trap charges.

Suk Kang Sung was born in Korea, in 1973. He received the B.S., M.S., and Ph.D. degrees from School of Electrical Engineering, Seoul National University, Seoul, Korea, in 1997, 1999, and 2004, respectively. Since 2004, he has been with Samsung Electronics, Kyungki-Do, Korea. His current research interests are nano-scale CMOS devices and future nonvolatile memories including SONOS, nano crystal memory.

Eun Suk Cho was born in Seoul, Korea, on October 20, 1972. He received the B.S.degree in materials science and engineering from Hanyang University, Seoul, Korea, in 1996 and the M.S degrees in electrical engineering from at SungKyunKwan University, Kyungki-Do, Korea, in 2005. Since 1999, he has been with Samsung

Electronics, Kyungki-Do, Korea. His research interests include nano scaled NVM and DRAM cell structure and technology, reliability, and field.

Choong Ho Lee has been working at Samsung electronics since 1988 with responsibility of process integration, and device research. His research activity involved, high-k gate oxide, process induced damage, process integration for the memory devices. He is presently a project leader of the device research team at Samsung Electronics and working on device technology for sub 50nm. He majored Electrical Engineering at Inha university, Korea and received B.S. in 1987. And he received the M.S. and Ph. D from the Electrical and Computer Engineering, the university of Texas at Austin, in 1999 and 2003.

Ilsub Chung was born in Jinju, Korea, in 1957. He received the B.S. degree in electronic engineering from SungKyun-Kwan University, Kyungki-Do, Korea, in 1981, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Texas at Austin in 1988 and 1992, respectively. In 1993, he joined the FRAM project team of the Samsung Advanced Institute of Technology, Giheung, Korea. In 2001, he joined SungKyunKwan University, where he is currently a Professor in the School of Electrical and Computer Engineering. In addition, he currently serves as a secretary of TC47/IEC. His main research area is the characterization of nonvolatile memories such as FRAM, MRAM, and SONOS.

Donggun Park received the B.S., M.S., degrees from Sogang University, Seoul, Korea, and Ph. D. degree from the University of California, Berkeley all in electrical engineering. His Ph.D. study was for the plasma charging damage and reliability of thin gate oxides. Since he joined Samsung Electronics in 1983, he involved in the diffusion process development of 64K and 256K DRAM, and process integration of 1Mega, 4Mega, 16Mega DRAM developments until 1993. After he finished his Ph.D study in 1998, he rejoined Samsung Electronics where he is now a vice president of Semiconductor R&D center. After the successful development of 0.15 m and 0.13 m 256M DRAMs, 90nm NAND Flash, and 100nm high speed 72M SRAM, in 1999, 2001, 2002, 2003, respectively, he is leading development projects of nano-CMOS transistors such as MBCFET / McFET/FinFET / PiFET / nanowireMOSFET and memory cell&core transistors for DRAM/SRAM/Flash.