# Single-Electron Logic Cells and SET/FET Hybrid Integrated Circuits

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*Abstract*—**Single-electron transistor (SET)-based logic cells and SET/FET hybrid integrated circuits have been fabricated on SOI chips. The input-output voltage transfer characteristic of the SET-based complementary logic cell shows an inverting behavior where the output voltage gain is estimated to be about 1.2 at 4.2K. The SET/FET output driver, consisting of one SET and three FETs, yields a high voltage gain of 13 and power amplification with a wide-range output window for driving next circuit. Finally, the SET/FET literal gate for a multi-valued logic cell, comprising of an SET, an FET and a constant-current load, displays a periodic voltage output of high/low level multiple switching with a swing as high as 200mV. The multiple switching functionality of all the fabricated logic circuits could be enhanced by utilizing a side gate incorporated to each SET component to enable the phase control of Coulomb oscillations, which is one of the unique characteristics of the SET-based logic circuits.**

*Index Terms*—**Silicon single-electron transistor(SET), SET complementary logic cell, SET output driver, SET/FET hybrid integrated circuit, SET/FET literal gate, SET/FET multi-functional logic cell**

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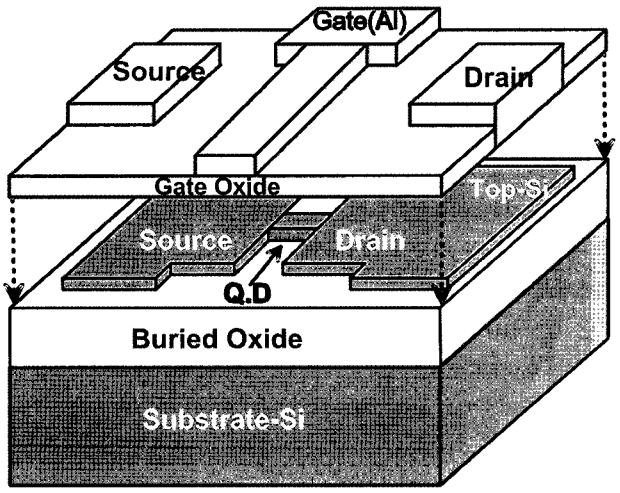
## I. Introduction

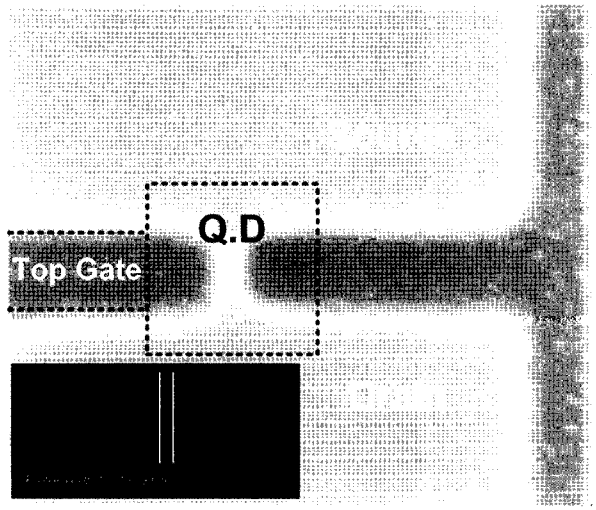
In the future tera-bit-scale integrated circuits the power consumption per chip becomes a critical issue, and an innovative reducing the number of electrons for switching transistor on and off will be inevitable. Single- and few-electron-based switching devices are expected to solve this problem. A variety of single-electron transistor (SET)-based logic schemes have been put forward but relatively few of the proposed single-electron logic cells have been demonstrated experimentally [1-7] since they need more precise nanofabrication processes compared to single-electron memory cells. In particular, silicon-based single-electron logic circuits, combined with FET, could be a highly probable candidate for the post-CMOS in future ultra-large scale integrated circuit since its fabrication process is quite compatible with the conventional CMOS technology. Here, we report a successful fabrication of silicon SETs by pattern-dependent oxidation (PADOX) technique and their applications to a complementary logic cells and SET/FET hybrid integrated circuits, both fabricated on a silicon-on-insulator(SOI) structure.

## II. Complementary SET Logic Cells and SET/FET Output Driver

In-plane type SET devices were fabricated on an SOI structure by PADOX method, by which small quantum islands are formed together with tunnel barriers at both sides in a self-aligned manner [8,9]. The SOI wafer, prepared by unibond method, consists of a p-type Si substrate, 180nm-buried $SiO_2$ and 80nm-top Si. Figure 1



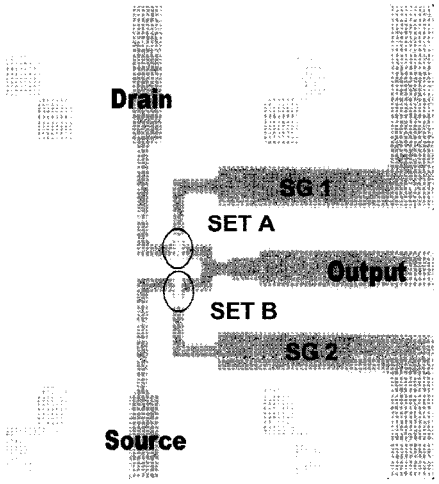

(a)



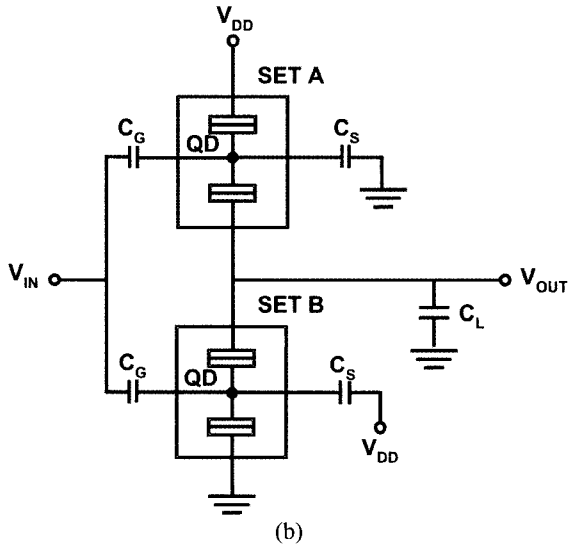

(b)

**Fig. 1.** (a) A schematic diagram of the resulting SET device structure. (b) a scanning electron micrograph picture of the active channel which was first defined to be 50nm-length times 15nm-width by e-beam lithography.

shows a schematic diagram of the resulting SET device structure and a scanning electron micrograph picture of the active channel. The channel was first defined by e-beam lithography and followed by reactive ion etching to a narrow wire of 50nm-length and 15nm-width which abruptly widens into source and drain carrier reservoir. Subsequent PADOX process further reduces the silicon channel. Its SET island is generated by oxidation-induced stress at the central part of the wire and tunnel barriers are formed at both ends of the wire. The resulting fabricated SETs, as previously reported [10], display nearly THz-level ultra-fast intrinsic RC speeds of ~2.THz, which is within an order of magnitude of the theoretical quantum limit. Their drain conductance measured at 4.2K approach to large values of μS order, exhibiting Coulomb oscillations with peak-to-valley current ratios >>1000. Incorporating the SETs as basic elements, in-plane side gate-controlled complementary logic cells and SET/FET output driver were fabricated on an SOI chip. Unlike previously reported device structures using double layered gates [11,12], a Coulomb island and side-gates were all defined in the same plane as the active channel by e-beam lithography and formed by deeply etching into the buried oxide. Such an in-plane structure is very efficient in Si fabrication process and the side gates adjacent to the electron island could easily control the phase of Coulomb oscillations, which plays a crucial role in achieving a complementary SET logic[7]. The resulting complementary SET-based inverter is seen in Figure 2 (a) with its corresponding circuit (Figure 2 (b)),




(a)




(b)

**Fig. 2.** (a) SEM picture of a complementary SET-based inverter fabricated on SOI wafer and (b) its corresponding circuit

in which two SETs operate in a complementary way, as FETs do in the traditional CMOS inverters. Both SET elements, each playing the role of n-SET and p-SET in the logic inverter, need to be in out-of-phase of Coulomb oscillations for operating in complementary manner. With adjusting the side gate voltage the phase of Coulomb peaks was observed to be predominantly shifted, which is seen in Figure 3. This illustrates that the input-output characteristics of the inverter can vary greatly depending on the voltages applied to the tuning side gates, which actually yield the induced charge difference on both SET islands. Out-of-phase of Coulomb oscillations for both SETs can be achieved when the induced charge difference approaches to e/2. Figure 4 (a) shows the input-output voltage transfer characteristic of the inverter with corresponding conductance peaks of two SET elements which display nearly out-of-phase of Coulomb oscillations. The output voltage gain is estimated to be about 1.2 at 4.2K, as determined from the slope of the transitional region, which guarantees possible signal transfer to the next logic gates. Figure 4 (b) shows the inverting operation for a square wave input with an amplitude of 30mV. Low switching speed is not due to the inverter itself, but just limited by slow response of the external circuit due to a large capacitance loading in the measurement system HP4156.

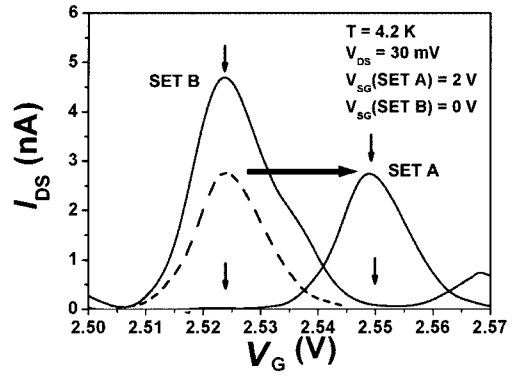
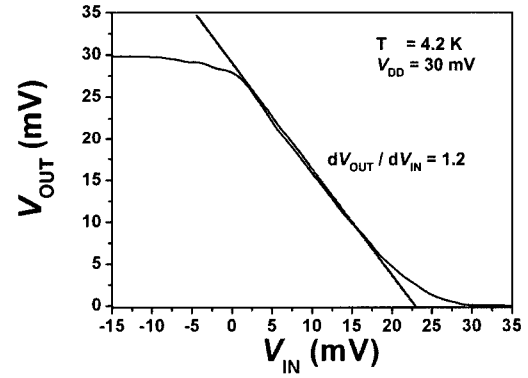
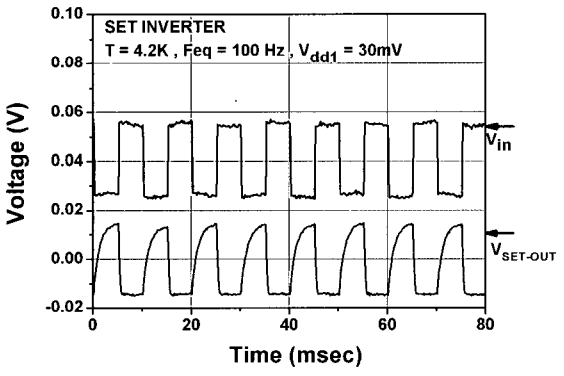



**Fig. 3.** Phase shifts of Coulomb peaks of a SET element with adjusting the side gate voltage

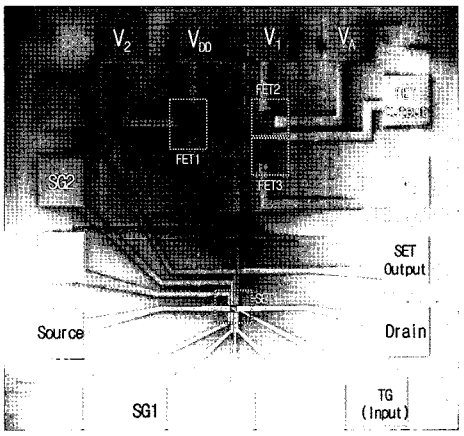



(a)

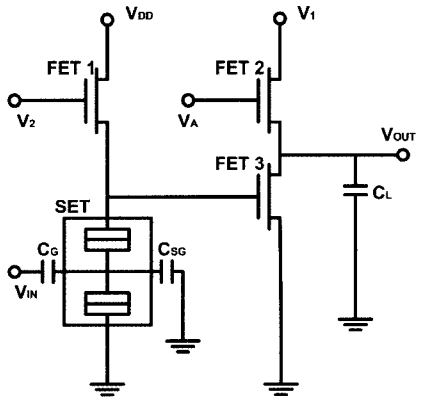



(b)

**Fig. 4.** (a) Input-output voltage transfer characteristic of the inverter, (b) Inverting operation for a square wave input with an amplitude of 30mV




(a)




(b)

**Fig. 5.** (a) SEM picture of the SET/FET hybrid circuit fabricated on an SOI chip as an output driver and (b) its corresponding circuit

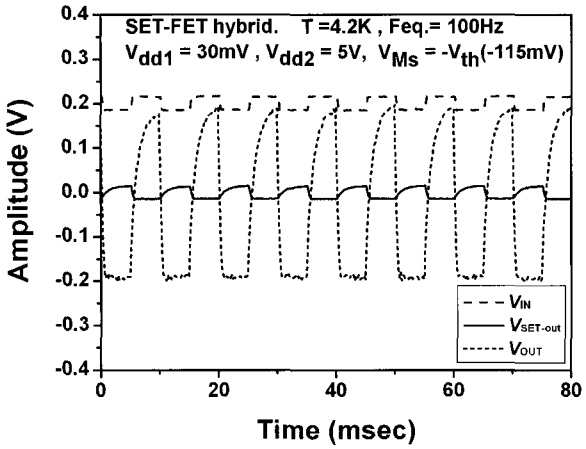



**Fig. 6.** Inverting and amplification behavior of the SET/FET output driver.

The SET/FET hybrid ICs fabricated on an SOI chip and its corresponding circuit is seen in Figure 5 a) & b). It consists of one SET and three FETs, where FET1 plays the role of a load resistor and FET2 & FET3 an output driver. Since the SET component operates only for a bias of 10mV level its output needs to be amplified to 1V level via the integrated FETs in order to drive any external periphery circuits. Figure 6 shows the output voltage of the SET-FET1 hybrid circuit and the FET2-FET3 amplifier as a function of the gate voltage of SET. The low/high levels of SET input gate are selected to be a conductance valley/peak positions of SET, which are set to Vg=0V/30mV. As seen in Figure 6, when the gate voltage is at a low/high level, the output of the SET-FET1 circuit becomes inverted to be at a high/low level, and this output is inverted again and amplified with the FET2-FET3 driver. It yields high voltage gain and power amplification with wide-range output window for driving next circuit. The small SET input gate voltage of 30mV is finally converted to 400mV, corresponding to an amplification ratio of 13. Here we point out again that the actual operating frequency is very low since the measured circuit speed is largely reduced by slow response of the external circuit due to a large capacitance loading in the measurement system.

## III. SET/FET Literal Gates For Multiple-Valued Logic Cell

Incorporating the SET with FET for a multiple-valued

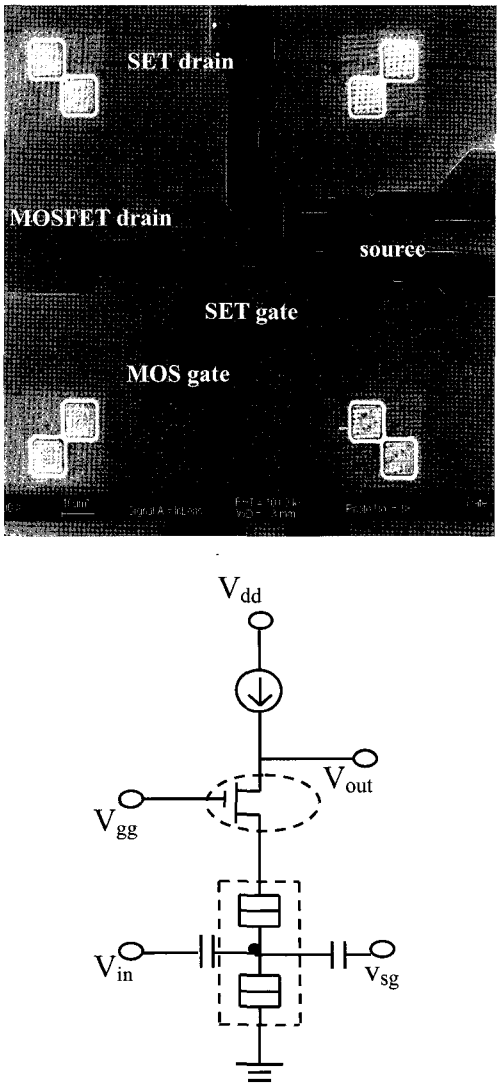



**Fig. 7.** (a) SEM picture of the resulting SET/FET literal gate comprising of an SET, a MOSFET and a constant-current load, (b) its corresponding circuit layout for a multi-valued logic cell.

logic cells, in-plane side gate-controlled literal gates were fabricated on an SOI chip. The resulting SET/FET hybrid circuit comprises of an SET, a MOSFET and a constant-current load, which is seen in Figure 7a), with its corresponding circuit layout of Figure 7b). In the SET part, Coulomb island and a side-gate were both defined in the same plane as the active channel by e-beam lithography and formed by deeply etching into the buried oxide. Such an in-plane structure is very efficient in Si fabrication process and the side gate adjacent to the Coulomb island can easily control the phase of Coulomb oscillations, which enables to achieve the multi-functionality of the output of the SET/FET literal gate. The input-output voltage transfer of the resultant

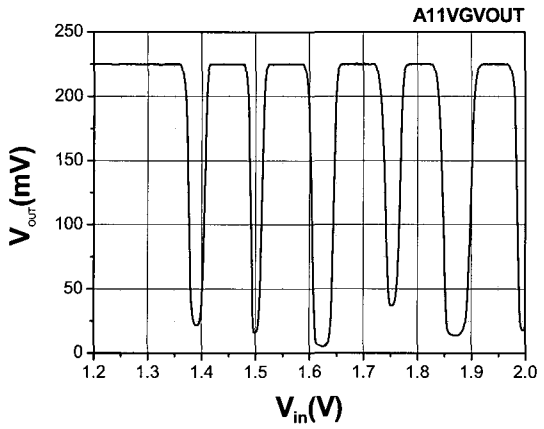



**Fig. 8.** Input-output voltage transfer of the resultant SET/FET literal gate measured at 4.2K, displaying five outputs high/low level multiple switching with a sharp swing as high as 200mV.

SET/FET literal gate measured at 4.2K is seen in Figure 8, displaying a periodic voltage output of high/low level multiple switching with a sharp swing as high as 200mV. A constant-current is 100pA and the $V_{gg}$ for the MOSFET is set to -80mV to attain an SET drain voltage of about 10mV. The multiple switching functionality of the literal gate could be enhanced by utilizing a side gate incorporated to the SET. After applying a proper value of the side gate voltage, the phase of Coulomb peaks of the SET can be shifted by approximately $\pi$ and be out-of-phase of that without applying side gate voltage, which results in transforming the SET current level from high to low. This phase control of Coulomb oscillations by the side gate voltage is one of the unique characteristics of the SET-based logic circuits and is utilized to achieve the complementary SET inverter.

## IV. Summary

We have made Si-based SET logic cells and SET/FET hybrid integrated circuits. The input-output voltage transfer characteristic of the complementary SET logic cell shows an inverting behavior where the output voltage gain is estimated to be about 1.2 at 4.2K. The SET/FET output driver consisting of one SET and three FETs yields a high voltage gain of 13 and power amplification with wide-range output window for driving next circuit. Finally, the SET/FET literal gate for a multi-valued logic cell, comprising of an SET, an FET and a constant-current load, displays a periodic voltage output of high/low level multiple switching with a swing as high as 200mV. The multiple switching functionality of all the fabricated logic circuits could be enhanced by utilizing a side gate incorporated to each SET component to enable the phase control of Coulomb oscillations, which is one of the unique characteristics of the SET-based logic circuits. Increasing the voltage gain as well as operating temperature of single-electron logic cell is very challenging since the gate capacitance should be made larger than the junction capacitance while keeping the total capacitance small. It almost certainly requires an innovative development in nanopatterning technology on sub-10nm scale level. Despite this issue, results of this work demonstrate that the single-electron logic cells and the SET/FET integrated circuits can operate as they were designed to. Since these circuits are core elements in logic integrated circuits, this work will accelerates the development of future high-density and low-power single-electron-based logic LSIs.

## Acknowledgments

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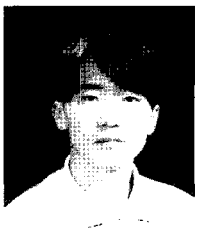

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