Characterization and Design Consideration of 80-nm Self-Aligned N-/P-Channel I-MOS Devices

Woo Young Choi, Jong Duk Lee, and Byung-Gook Park

Abstract—**80-nm self-aligned n- and p-channel I-MOS devices were demonstrated by using a novel fabrication method featuring double sidewall spacer, elevated drain structure and RTA process. The fabricated devices showed a normal transistor operation with extremely small subthreshold swing less than 12.2 mV/dec at room temperature. The n- and p-channel I-MOS devices had an ON/OFF current of 394.1/0.3 μA and 355.4/8.9 μA per μm, respectively. We also investigated some critical issues in device design such as the junction depth of the source extension region and the substrate doping concentration.**

Index Terms—**Self-alignment, I-MOS, fabrication method, subthrehold swing, design, junction depth, substrate doping concentration.**

I. INTRODUCTION

Recently, aggressive scaling-down of metal-oxide-semiconductor field-effect transistors (MOSFETs) has aggravated some important problems [1-3]. For example, in the case of high performance applications, one uses near-constant field scaling to maintain optimized MOSFET behavior as shown in Figure 1. As a result, one can get almost the same ON current in spite of supply voltage reduction. However, OFF current increases exponentially as devices are scaled down. It is due to the fact that the value of subthreshold swing is mostly unchanged during scaling-down. Therefore, reduction of subthreshold swing plays an important role in device scaling-down. Subthreshold swing is defined as the change in the gate voltage V_{GS} required to reduce subthreshold current I_{DS} by one decade, which indicates the gate voltage swing required to reduce the current from its ON value to an acceptable OFF value. For good ON/OFF characteristics, it should be as small as possible. It is widely known that the minimum attainable value of the subthreshold swing is approximately 60 mV/dec at room temperature. However, nonidealities such as a nonzero gate oxide thickness or the presence of interface states lead to a subthreshold swing of more than 60 mV/dec. In addition, high substrate doping concentration to suppress short channel effects accelerates the increase of the subthreshold swing, which means that MOSFETs gradually recede from ideal switches. If one sticks to the p-n junction barrier lowering for carrier

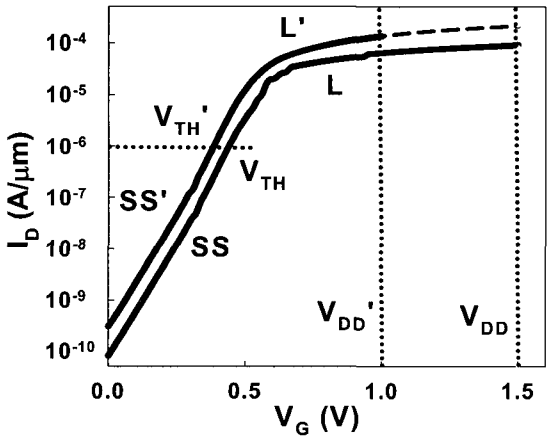

Fig. 1. CMOS scaling-down trend in the case of high performance applications. Almost the same ON current is always achievable in spite of supply voltage reduction. However, exponentially-increasing OFF current is problematic which results from the fact that the value of subthreshold swing is mostly unchanged during scaling-down. Therefore, reducing the value of subthreshold swing plays an important role in device scaling-down.

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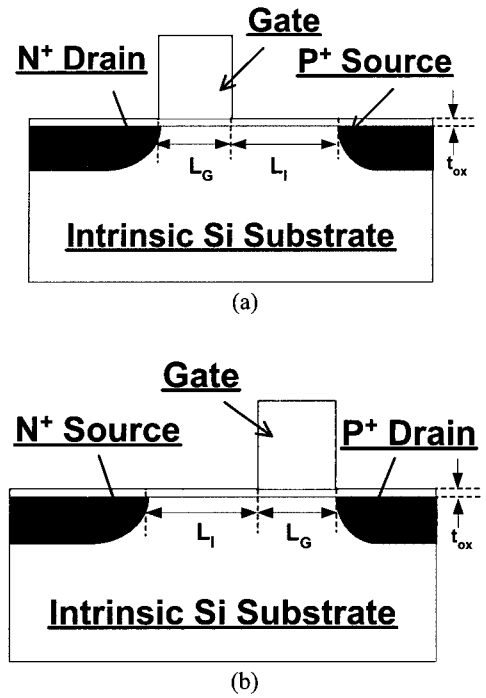


Fig. 2. The basic structure of (a) the n- and (b) the p-channel I-MOS device. The I-MOS device has two major distinctions compared with the MOSFET: opposite kind of dopants in the source and the drain region and an i-region.

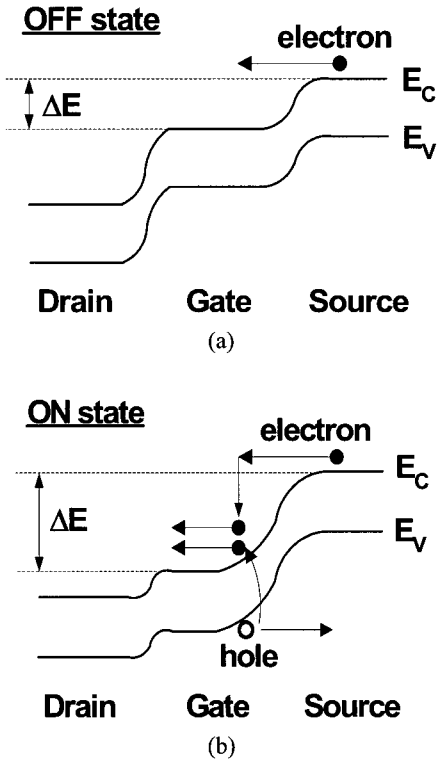


Fig. 3. (a) Band diagram of the I-MOS device structure in OFF state. The energy difference between the channel and the source (ΔE) is not large enough to induce impact ionization. (b) Band diagram of the I-MOS in ON state. The energy difference between the channel and the source (ΔE) is large enough to induce impact ionization, which leads to avalanche breakdown.

injection mechanism, the subthreshold swing can never be reduced below 60 mV/dec at room temperature.

The impact-ionization metal-oxide-semiconductor (I-MOS) device was proposed in order to overcome the problems mentioned above [4]. The basic structure of the I-MOS device is illustrated in Figure 2, which is basically a gated p-i-n diode structure. It has two major differences compared with the MOSFET. One is that the source and the drain have opposite kind of dopants and the other is that there exists an i-region which is not completely overlapped by the gate. This i-region is used to induce avalanche breakdown between the source and the channel. The operating principle of the I-MOS device is the modulation of the avalanche breakdown voltage of a gated p-i-n structure to control the output current as depicted in Figure 3. Although only the case of the n-channel I-MOS device is mentioned, the same is true for the p-channel one. Major difference between the MOSFET and the I-MOS device is the carrier injection mechanism from the source. In the case of the former, carriers are injected thermally. There is a potential barrier between the source and the drain and the gate modulates it to control output current. However, the latter has no potential barrier between the source and the drain. Instead, because carriers of the I-MOS device are injected through avalanche breakdown process, the potential difference between the source and the channel determines whether breakdown occurs or not. The role of the gate is to control the channel potential. In OFF state when gate bias is below the threshold voltage, the potential difference is not large enough to induce avalanche breakdown. However, in ON state when the gate bias exceeds the threshold voltage, the potential difference becomes large enough to induce avalanche breakdown. Then, current starts to flow between the source and the drain. Because the p-n junction barrier lowering is not the mechanism of current flow control in the I-MOS device, it is possible to reduce the subthreshold swing below 60 mV/dec at room temperature.

The I-MOS device has some advantages and disadvantages. In spite of its merits such as the subthreshold swing below thermal voltage and fast switching, a few critical problems have made the I-MOS device difficult to realize: high gate voltage required to

induce avalanche breakdown and difficulty in self-alignment. We have focused on solving these problems. Up to now, we have proposed a novel biasing scheme based on device physics [5] and successfully fabricated a 130-nm n-channel I-MOS device [6] and 100-nm n- and p-channel I-MOS devices [7]. In this paper, we have introduced a new fabrication method featuring double sidewall spacer to form source extension region, elevated drain structure and rapid thermal annealing (RTA). Based on it, we have fabricated 80-nm self-aligned n- and p-channel I-MOS devices and studied some critical issues in device design.

II. Device Fabrication

Figure 4 shows the conventional fabrication method of an n-channel I-MOS device [4]. Following gate oxidation, the gate is defined by photolithography. Then, n- and p-type ion implantation is performed for the source and the drain region formation, respectively. Because the gate, the source and the drain region are formed in turn with separate photomasks, self-alignment is not possible in the conventional case. It means that the gate length (L_G) and the i-region length (L_I) are limited by the alignment error and finally leads to high cost due to increased number of photomasks, performance degradation due to parasitic elements and limit in scaling-down.

For self-alignment, we proposed a new fabrication method and implemented 130-nm and 100-nm I-MOS devices for the first time [6, 7]. However, it was still difficult to apply to sub-100nm region because the source and drain junction can not be made shallow enough to maintain low parasitic resistance. In this study, we improve the fabrication method by adopting double sidewall spacer, elevated drain structure and RTA process as shown in Figure 5. Contrary to the conventional process, the drain region is defined firstly in a mesa shape. Following gate oxidation, the gate is patterned in a sidewall spacer form beside the drain region. A tetraethyl orthosilicate (TEOS) layer on the gate acts as a mask to protect the gate region from counterdoping during p-type ion implantation. The first sidewall spacer formation is followed by low-energy p-type ion implantation for shallow source extension. Subsequently, after the second sidewall formation, high-energy p-type

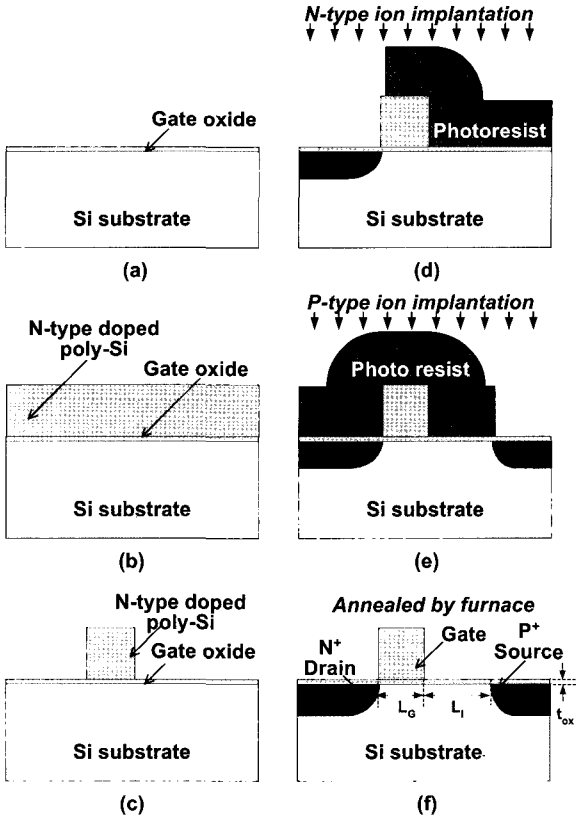


Fig. 4. Conventional fabrication method of an n-channel I-MOS device. The same is the case to a p-channel I-MOS except for the exchange of n-type and p-type. (a) Gate oxidation. (b) n-type doped poly-silicon layer deposition. (c) Gate line definition by photolithography. (d) n-type ion implantation following photolithography in order to form the drain region. (e) p-type ion implantation following photolithography in order to form the source and the i-region. (f) Annealing process by furnace.

ion implantation is done for deep source region in order to minimize the source parasitic resistance. On the other hand, in the drain region, we imitate the elevated source/drain process in MOSFETs [8]. By making the junction depth of the drain similar to the height of the drain mesa, it is possible to get the shallow drain junction with low parasitic resistance. Finally, RTA process is performed at 1000 ℃ for 5 seconds. The merits of the proposed method are summarized as follows. One is that, once the drain region is defined by photolithography step, the gate and the source can be formed with self-alignment. Another is that shallow source and drain can be formed with the aid of the source extension and the elevated drain. The other is that the voltage for avalanche breakdown is reduced. It is related to the radius of curvature of the source extension region and will be discussed in Section IV.

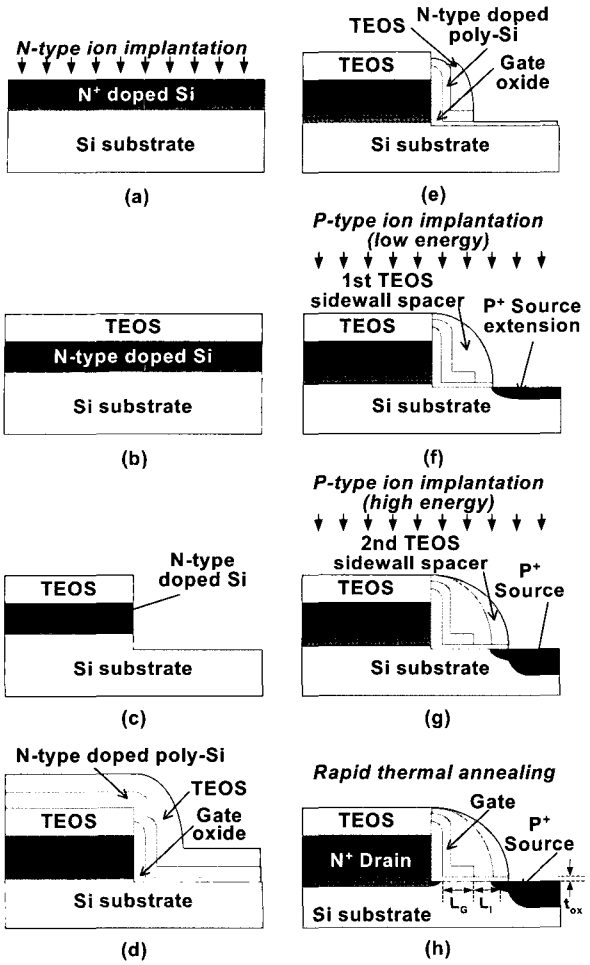


Fig. 5. Novel fabrication method of an n-channel I-MOS device. The same is the case to a p-channel I-MOS one. (a) n-type ion implantation. (b) TEOS layer deposition. (c) Definition of the drain region following photolithography. (d) Gate oxidation followed by n-type doped poly-silicon and TEOS layer deposition. (e) Gate line definition. (f) Low-energy p-type ion implantation in order to form the source extension region following the first sidewall spacer formation. (g) High-energy p-type ion implantation in order to form deep source region following the second sidewall spacer formation. (h) Annealing process by RTA.

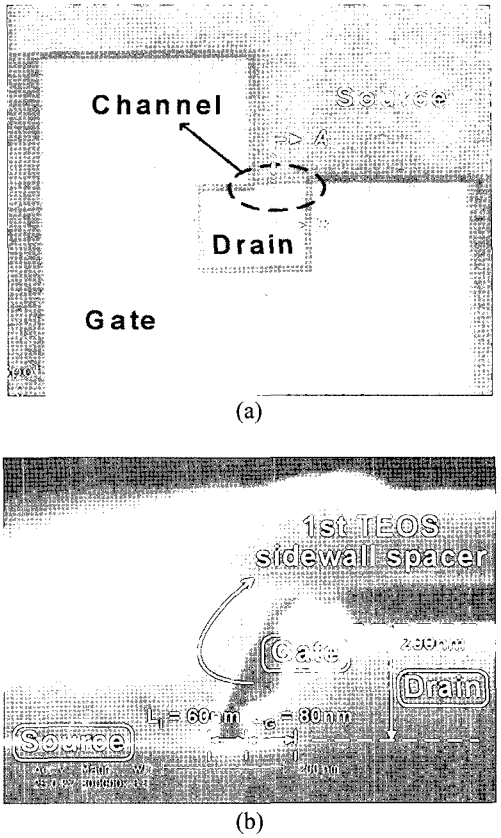
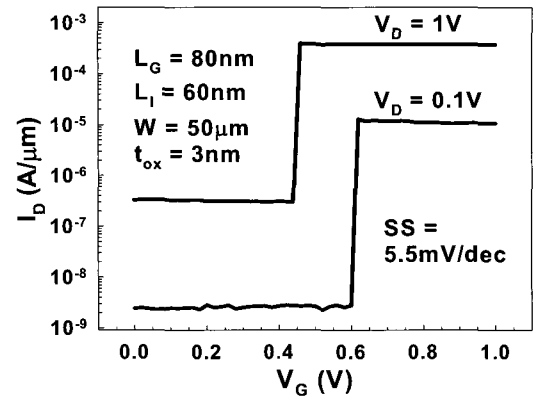


Fig. 6. SEM images of the fabricated I-MOS device. (a) Plan view. Because a ring-shaped gate structure is used, the gate encircles the drain region and the rest of the area becomes the source region. (b) Cross-sectional view. Gate length, i-region length and drain mesa height are 80, 60 and 200 nm, repectively.

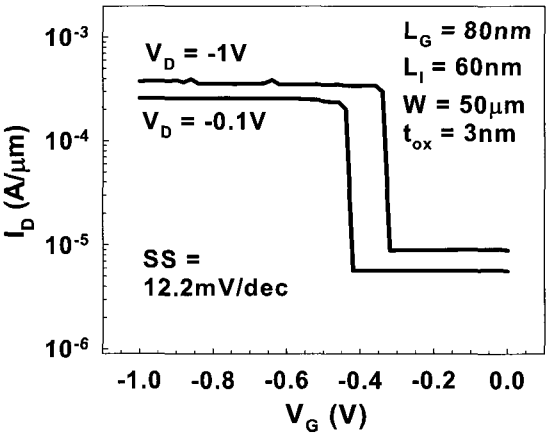
III. Results and Discussions

By using the proposed fabrication method depicted in Figure 5, we have fabricated self-aligned n- and p-channel I-MOS devices whose gate length, i-region length and gate oxide thickness are 80, 60 and 3 nm, respectively. It is realized on a bulk silicon substrate. Figure 6 (a) shows the plan-view scanning electron microscopy (SEM) image of the fabricated device. Because a ring-shaped gate structure is adopted for fabrication convenience, the gate encircles the drain region and the rest of the area becomes the source region. Cutting through the line from A to B, we can get the cross-sectional image shown in Figure 6 (b).

Figure 7 illustrates the transfer curves of the fabricated 80-nm n- and p-channel I-MOS devices. During the measurement, we introduced a novel biasing scheme: negatively biasing the source that induces enough voltage difference between the source and the channel [5]. Thus, the biasing voltages of the source regions were fixed at -5.5 and 5.5 V for n- and p-channel cases, respectively. Both devices show a normal transistor operation with extremely small subthreshold swing, which ranges from 5.5 to 12.2 mV/dec at room temperature. As mentioned in section I, it results from the change in the carrier injection mechanism from the source. Additionally, thanks to the novel biasing scheme, the threshold voltage and the drain voltage are reduced dramatically.



(a)



(b)

Fig. 7. Transfer curve of the fabricated device. (a) n-channel I-MOS device. (b) p-channel I-MOS device. Both devices show a normal transistor operation with small subthreshold swing, which ranges from 5.5 to 12.2 mV/ dec at room temperature.

Table 1. Process conditions of this work compared with previous ones.

	Ref. [4]	Ref. [6]	Ref. [7]	This work
Device type	p-channel	n-channel	both	both
L_G (nm)	2000	130	100	80
L_I (nm)	500	60	60	60
t_{ox} (nm)	20	4	3	3
Self-alignment	X	O	O	O
Double sidewall spacer	X	X	X	O
Annealing	By furnace	By furnace	By RTA	By RTA
Number of photomasks	10	2	2	2

Table 2. Electrical characteristics of this work compared with previous results.

	Ref. [4]	Ref. [6]	Ref. [7]	This work
V_D (V)	20	1	1	1
DICE (mV/V) [6]	Not available	240 (n-channel)	260 (n-channel)	160 (n-channel)
		Not available	140 (p-channel)	120 (p-channel)
SS (mV/dec)	Not available	7.2 (n-channel)	7.5 (n-channel)	5.5 (n-channel)
	10~50 (p-channel)	Not available	11.8 (p-channel)	12.2 (p-channel)
I_{ON} (μA/μm) (V_G-V_T=0.5V)	Not available	44.6 (n-channel)	81.1 (n-channel)	394.1 (n-channel)
		Not available	78.2 (p-channel)	355.4 (p-channel)
I_{OFF} (μA/μm) (V_G-V_T=-0.1V)	Not available	4.9 (n-channel)	2.8 (n-channel)	0.3 (n-channel)
		Not available	3.4 (p-channel)	8.9 (p-channel)

Table 1 and 2 summarize the process conditions and electrical characteristics of this work compared with some previous results, respectively. In terms of theprocess conditions, with the help of the new fabrication method, the gate length and the i-region length are scaled down to 80 and 60 nm, respectively, in this work. Moreover, the number of photomasks is greatly reduced down to 2. With regard to the electrical characteristics, it is observed that most of the performance factors are enhanced. The n- and p-channel I-MOS device have an ON/OFF current of 394.1/0.3 μA and 355.4/8.9 μA per μm, respectively. The novel biasing scheme and device scaling-down reduce the threshold voltage, the drain voltage and drain induced current enhancement (DICE) [6]. In spite of adopting a ring-shaped gate structure which generally suffers from a lot of parasitic elements, we have been able to improve the electrical characteristics by combining the novel fabrication method and the novel biasing scheme. If photomask structure is modified later, it is expected that the electrical performance of the device will be much enhanced.

IV. Design Consideration Of the I-MOS Device

In this section, we consider some issues on the design of the I-MOS such as the source extension junction depth and the substrate doping concentration.

1. Effect of the source extension junction depth

As mentioned in Section II, one of the advantages of

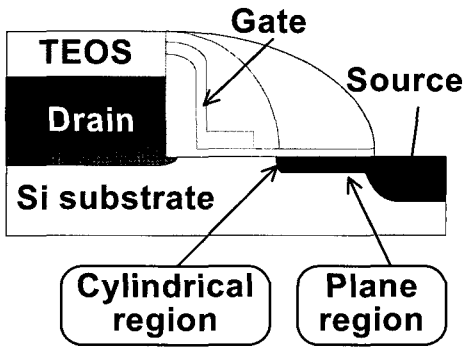


Fig. 8. Plane and cylindrical region of the source extension region. The shallower the source extension is, the smaller the radius of curvature becomes, which leads to the reduction of the avalanche breakdown voltage.

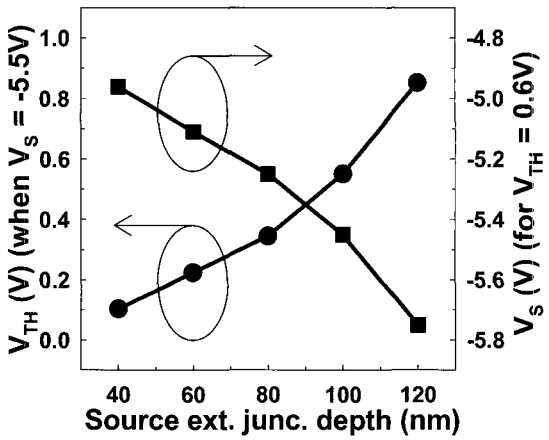


Fig. 9. Dependence of threshold voltage on source extension junction depth, when the source voltage is fixed at -5.5 V and source voltage needed to maintain threshold voltage of 0.6 V.

the novel fabrication method is the reduction of avalanche breakdown voltage. The source extension region consists of plane and cylindrical region as depicted in Figure 8. It is originated from the planar processes. When a p-n junction is formed by implantation or diffusion through a window in a mask layer, the dopants will diffuse downward and also sideways. It has been reported that this cylindrical region has critical effects on junction, especially for the avalanche breakdown process [9]. As the junction depth of the source extension is reduced, the radius of curvature of the cylindrical region decreases and finally the voltage necessary for inducing avalanche breakdown also decreases [10]. This reduction of avalanche breakdown voltage has no apparent theoretical limit [11]. A continuous decrease in the radius of curvature leads to a continuous decrease of the breakdown voltage until other breakdown mechanisms dominate and carrier multiplication is therefore no longer an important factor. Because the proposed fabrication method can form extremely shallow source extension region by adopting double sidewall spacer, the biasing voltage of the source region can be reduced.

In order to investigate the relationship between the junction depth of the source extension region and the source voltage, we performed two-dimensional simulation by ATLAS. The simulated device structure refers to the n-channel version of experimental data in Section III. Figure 9 shows that the threshold voltage and the source voltage to maintain constant threshold voltage strongly depend on the junction depth of the source extension region. As the junction depth of the source extension region is reduced from 120 to 40 nm, the source voltage to maintain the threshold voltage of -0.6 V is reduced from -5.7 down to -4.9 V. If one sticks to the source voltage of -5.5 V, the threshold voltage will be reduced down to 0.1 V. Thus, if we combine the proposed fabrication method with recent shallow junction technology, the voltage for inducing the avalanche breakdown is expected to be further reduced.

2. Effect of the substrate doping concentration

Since the I-MOS device has a gated p-i-n structure, the substrate doping concentration (N_{sub}) influences the device characteristics. Thus, a study on the optimal substrate doping concentration is useful and indispensable to device design. From now on, we will focus on the effect of the substrate doping concentration on the device characteristics particularly in terms of the threshold voltage and ON/OFF current ratio. The simulated device structure also refers to the n-channel version of experimental data in Section III. As a result of the simulation, a unique characteristic of the I-MOS device was found for the first time as shown in Figure 10: the threshold voltage of the I-MOS ($V_{TH,I\text{-}MOS}$) decreases as the substrate doping concentration increases, which is contrary to the that of the MOSFET ($V_{TH,MOS}$). It is easily understood considering the fact that the turn-on mechanism of the I-MOS device is quite different from that of the MOSFET. In the latter, the threshold voltage is defined as the gate voltage when the surface potential reaches twice the potential difference between intrinsic and extrinsic Fermi level [12, 13]. On the other hand, the threshold voltage of the I-MOS is defined as the gate

voltage when the avalanche breakdown begins to occur between the channel and the source. To understand this phenomenon, we have adopted, as a criterion, the maximum lateral electric field (E_{max}) when the gate is biased at 0 V. As it becomes higher, more electrons are supplied into the channel through the avalanche breakdown. Figure 10 shows that the maximum lateral electric field increases with the increase of the substrate doping concentration, which results from the junction abruptness between the channel and the i-region. Therefore, high substrate doping concentration will lead to the increase of the maximum lateral electric field at the same gate bias and finally reduce the threshold voltage of the I-MOS device. For further analysis, we have compared $V_{TH,I\text{-}MOS}$ with $V_{TH,MOS}$ and found that the former is larger than the latter as depicted in the inset of Figure 11. It means that even if the surface potential reaches an inversion point, additional gate biasing ($V_{TH,I\text{-}MOS} - V_{TH,MOS}$) is still necessary to get enough carriers injected from the source in the I-MOS device. Additionally, with the substrate doping concentration increased, it becomes harder to form the inversion layer but easier to induce the avalanche breakdown. Therefore, the additional gate biasing is reduced as the substrate doping concentration becomes higher as shown in Figure 11.

Figures 12 and 13 illustrate the effect of the substrate doping concentration on the output current. In Figure 12, as the substrate doping concentration becomes higher,

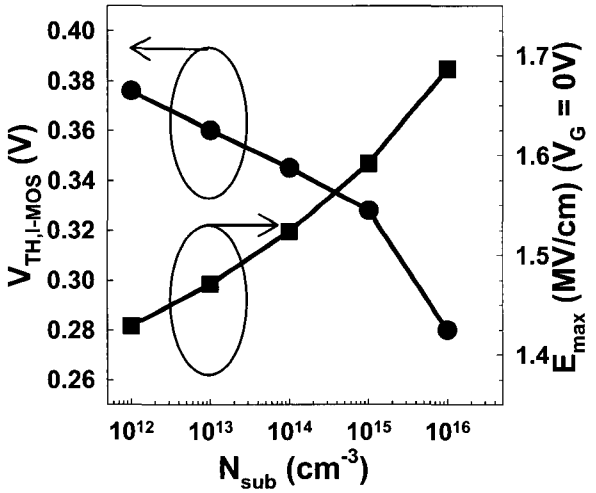


Fig. 10. Threshold voltage and maximum lateral electric field with the substrate doping concentration varied. It is observed that threshold voltage decreases as the substrate doping concentration increases, which is contrary to the MOSFET case.

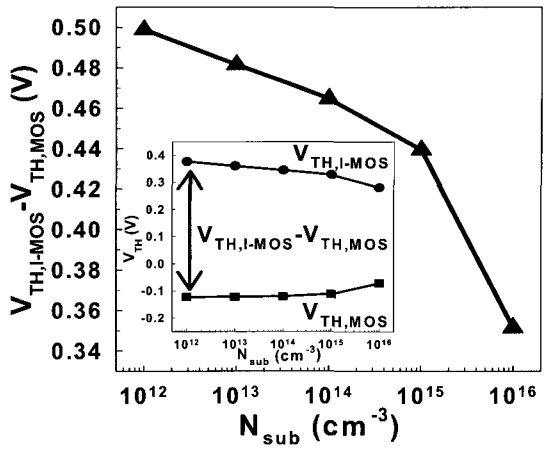


Fig. 11. Additional gate biasing with the substrate doping concentration varied. The inserted figure shows comparison between the threshold voltage of the I-MOS device and the MOSFET as a function of the substrate doping concentration.

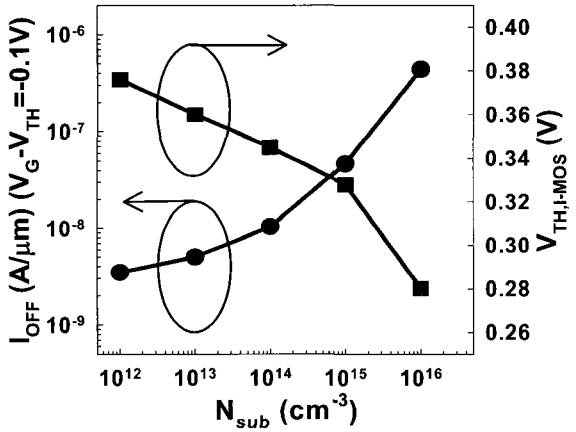


Fig. 12. Threshold voltage and OFF current as a function of the substrate doping concentration. As the substrate doping concentration becomes higher, the OFF current increases more rapidly due to the leakage current between the drain and the substrate.

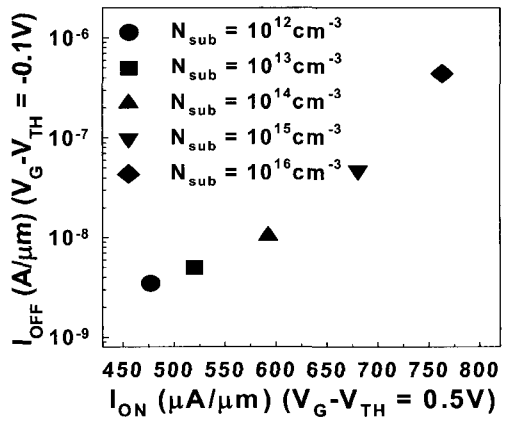


Fig. 13. Dependence of ON and OFF current characteristic on the substrate doping concentration. Both ON and OFF current increase as the substrate doping concentration becomes higher.

the OFF current increases more rapidly due to the leakage current between the drain and the substrate. Figure 13 summarizes ON and OFF current relationship with various substrate doping concentrations. We have found that both ON and OFF current increase and that the $V_{TH,I\text{-}MOS}$ decreases as the substrate doping concentration becomes higher. Therefore, it can be thought that the substrate doping concentration should be determined considering the application for which the I-MOS device is used. For example, high-purity substrate is necessary for low-power consumption (high threshold voltage, low OFF current) and moderately-doped substrate is for high performance (low threshold voltage, high ON current).

We have studied the effect of the substrate doping concentration on the I-MOS device characteristics in terms of the threshold voltage and the ON and OFF current. An interesting relationship between the substrate doping concentration and the threshold voltage was observed, which was explained by the maximum lateral electric field. Additionally, it was also found that the substrate doping concentration was an important design parameter to the device applications: either low power or high performance.

V. Conclusions

80-nm self-aligned n- and p-channel I-MOS devices were fabricated for the first time by adopting double sidewall spacer, elevated drain structure and RTA process. It shows a normal transistor operation with small subthreshold swing less than 12.2 mV/dec at room temperature. We have also studied some device design issues in terms of the junction depth of the source extension region and the substrate doping concentration. It is found that the avalanche breakdown voltage can be significantly reduced by introducing shallow source extension region and that the dependence of the threshold voltage of the I-MOS device on the substrate doping concentration is contrary to that of the MOSFET.

Acknowledgments

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References

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, pp. 259-288, Mar. 2001.

[2] M. Lundstrom, "Device physics at the scaling limit: what matters?" in *IEEE Int. Electron Devices (IEDM) Tech. Dig.*, pp. 789-792, 2003.

[3] S. Borkar, "Circuit techniques for subthreshold leakage avoidance, control, and tolerance," in *IEEE Int. Electron Devices (IEDM) Tech. Dig.*, pp. 421-424, 2004.

[4] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: a novel semiconductor device with a subthreshold slope lower than kT/q," in *IEEE Int. Electron Devices (IEDM) Tech. Dig.*, pp. 289-292, 2002.

[5] W. Y. Choi, J. Y. Song, J. D. Lee, Y. J. Park, and B.-G. Park, "A novel biasing scheme for I-MOS (impact-ionization MOS) devices," *IEEE Trans. Nanotechnology*, vol. 4, no. 3, pp. 322-325, May 2005.

[6] W. Y. Choi, B. Y. Choi, D.-S. Woo, J. D. Lee, and B.-G. Park, "A new fabrication method for self-aligned nanoscale I-MOS (Impact-ionization MOS)," in *62nd Annual Device Research Conference*, pp. 211-212, 2004.

[7] W. Y. Choi, J. Y. Song, J. D. Lee, Y. J. Park, and B.-G. Park, "100-nm n-/p-channel I-MOS using a novel self-aligned structure," *IEEE Electron Device Lett.*, vol. 26, no. 4, pp. 261-263, Apr. 2005.

[8] A. Hokazono, K. Ohuchi, K. Miyano, I. Mizushima, Y. Tsunashima, and Y. Toyoshima, "Source/drain engineering for sub-100nm CMOS using selective epitaxial growth technique," in *IEEE Int. Electron Devices (IEDM) Tech. Dig.*, pp.243-246, 2000.

[9] G. Gibbons, and J. Kocsis, "Breakdown voltages of germanium plane-cylindrical junctions," *IEEE Trans. Electron Devices*, vol. 12, pp. 193-198, Apr. 1965.

[10] R. S. Muller, and T. I. Kamins, *Device electronics for integrated circuits*, New York: John Willey & Sons, 1986.

[11] D. P. Kennedy, and R. R. O'Brien, "Avalanche breakdown calculations for a planar p-n junction,"

IBM Journal of Research and Development, vol. 10, no. 3, pp. 213-219, May 1966.

[12] W. Y. Choi, H. Kim, B. Lee, J. D. Lee, and B.-G. Park, "Stable threshold voltage extraction using Tikhonov's regularization theory," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1833-1839, Nov. 2004.

[13] H.-S. Wong, M. H. White, T. J. Krutsick, and R. V. Booth, "Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFETs," *Solid-State Electronics*, vol.30, no.9, pp.953-968, 1987.

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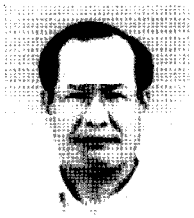
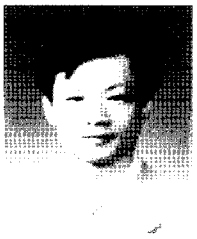


Jong Duk Lee received the B.S. degree in physics from Seoul National University, Seoul, Korea, in 1966, and the Ph.D. degree from the Department of Physics, University of North Carolina, Chapel Hill, in 1975. He was an Assistant Professor in the Department of Electronics Engineering, Kyungpook National University, from 1975 to 1978. In 1978, he studied microelectric technology in HP-ICL, Palo Alto, CA, and soon afterward worked for the Korea Institute of Electronic Technology (KIET) as the Director of the semiconductor division. He established the KIET Kumi Facility and introduced the first polysilicon gate technology in Korea by developing 4K SRAM, 32K, and 64K Mask ROMs, and one-chip 8-bit microcomputers. In July 1983, he moved to the Department of Electronics Engineering, Seoul National University, as an Associate Professor, which has merged with the School of Electrical Engineering in 1992, where he has been Professor since 1988. He established the Inter-University Semiconductor Research Center (ISRC) in 1985, and served as the Director until 1989. He served as the chairman of the Electronics Engineering Department from 1994 to 1996. He was with Samsung Display Devices Co., Ltd., as the Head of Display R&D Center in 1996, on leave from Seoul National University. He concentrated his study on the image sensors such as Vidicon type, MOS type, and also CCDs, for Samsung Display Devices Co. and Samsung Electronics Co. from 1984 to 1991. His current research interests include sub-0.1μm CMOS structure and technology, FEDs, CMOS image sensor, and high speed SRAM design. He published over 130 papers in the major international scientific journals, including over 65 SCI papers. He has presented more than 180 papers including 80 international conference papers. He also has registered 11 U.S., three Japanese, and eight Korean patents.

Dr. Lee is the member of the steering committee for IVMC (International Vacuum Microelectronics Conference) and KCS (Korean Conference on Semiconductors). He was the Conference Chairman of IVMC'97 and KCS'98 who led the IVMC'97 and the KCS'98. He was also a member of the IEDM (International Electron Devices Meeting) Subcommittee on Detectors, Sensors, and Displays operated by IEEE Electron Devices Society from 1998 to 1999. In June 1999, he was elected First President of the Korean Information Display Society.



Byung-Gook Park received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1990. From 1990 to 1993, he was with AT&T Bell Laboratories, Murray Hill, NJ, where he contributed to the development of 0.1-μm CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, Dallas, TX, developing 0.25-μm CMOS. In 1994, he joined the School of Electrical Engineering, Seoul National University, as an assistant professor. He is currently a full professor. He has been in charge of the research of Inter-university Semiconductor Research Center (ISRC) in Seoul National University since 2003 as the chief of the research department. His current research interests are nanoscale CMOS devices, Si single-electron devices, nonvolatile memory devices, and organic electroluminescent displays. Dr. Park was a member of the International Electron Devices Meeting Subcommittee on Solid State Devices from 2001 to 2002 and worked for Silicon Nanoelectronics Workshop 2005 as a program chair.