# 1/f Noise Characteristics of Sub-100 nm MOS Transistors

**Jeong-Hyun Lee*, Sang-Yun Kim*, Ilhyun Cho**, Sungbo Hwang**, and Jong-Ho Lee***

***Abstract*—We report 1/f noise PSD(Power Spectrum Density) of sub-100 nm MOSFETs as a function of various parameters such as HCS (Hot Carrier Stress), bias condition, temperature, device size and types of MOSFETs. The noise spectra of sub-100 nm devices showed Lorentzian-like noise spectra. We could check roughly the position of a dominant noise source by changing $V_{DS}$. With increasing measurement temperature, the 1/f noise PSD of 50 nm PMOS device decreases, but there is no decrease in the noise of NMOS device. RTN (Random Telegraph Noise) was measured from the device that shows clearly a Lorentzian-like noise spectrum in 1/f noise spectrum.**

***Index Terms*—1/f noise, RTN, Fluctuation, sub-100 nm, MOSFET**

## I. INTRODUCTION

Recently, 1/f noise (flicker noise) in MOSFETs is becoming more important as a feature size of the devices is scaled down aggressively. With the decreasing feature size, 1/f noise increases in proportion to $1/L_g^3$[1]. Especially, 1/f noise is an important parameter for analog and RF applications. The increase in 1/f noise is detrimental to the phase noise performance of high-frequency non-linear circuits such as mixers and oscillators[2]. Many kinds of traps exist at the interface between silicon and gate oxide of MOSFETs, and their effects dominate as the gate oxide thickness decreases.

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Trap makes current fluctuation in the channel region of MOSFETs, and this fluctuation generates 1/f noise. There are two scenarios: One is that fluctuation in the total numbers of charge carriers generates 1/f noise; the other is that fluctuation in the mobility of carriers generates 1/f noise[1]. These current fluctuations appear as RTN. RTN is the result of the decomposition of the 1/f spectrum into individual fluctuating components. Conversely speaking, the 1/f spectrum can be viewed as superposition of individual trapping events each of which generates RTN in time domain[7]. The 1/f noise characteristics of long channel MOSFETs have been reported in detail under various kinds of condition [1]-[7]. However, those of sub-100 nm MOS devices have not been reported extensively.

In this work, we measure the 1/f noise characteristics of sub-100 nm MOSFETs under several conditions and report the measurement results.

## II. RESULTS AND DISCUSSIONS

The MOS devices in this work have conventional planar channel structure. NMOS and PMOS devices have $n^+$ and $p^+$ poly-Si gates, respectively. The gate oxide thickness of the MOS devices is 1.6nm thick nitride oxide (NO).

Figure 1 shows the 1/f noise characteristics of n-channel MOSFETs as a parameter of $V_{DS}$. The $V_{GS}$-$V_{th}$ is fixed at 0.2 V. To measure the 1/f noise characteristics between linear and saturation regions, the drain bias is changed from linear region to saturation region. Here the device has a $W/L$ of 150 nm/50 nm. With increasing $V_{DS}$, the $I_D$ increases, resulting in 1/f noise increase. Since the device size is very small, the 1/f noise power shows Lorentzian-like noise spectra. Especially, we can guess approximate position of the traps corresponding to the

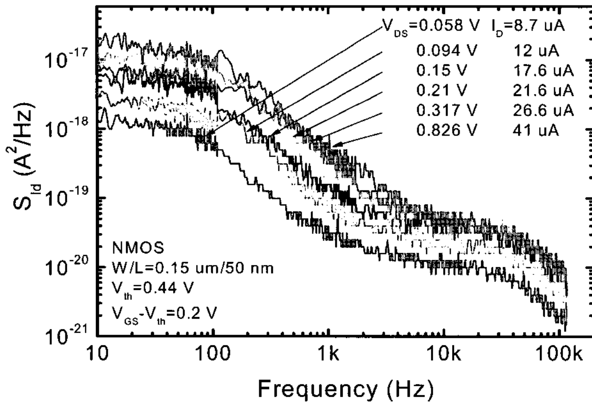


**Fig. 1.** 1/f noise spectra in n-channel MOSFETs with the drain voltage as a parameter. The device has a $W/L$ of 0.15 μm/50 nm. The $V_{GS}$-$V_{th}$ is fixed at 0.2 V.

Lorentzian-like noise humps. There are two humps at ~70 Hz and ~30 kHz. As the $V_{DS}$ increases, the drain-side inversion region is depleted. Since the location of the humps keeps nearly the same position with the $V_{DS}$ change, we can say that the noise sources corresponding to the humps are located at a channel position except near the drain-side.

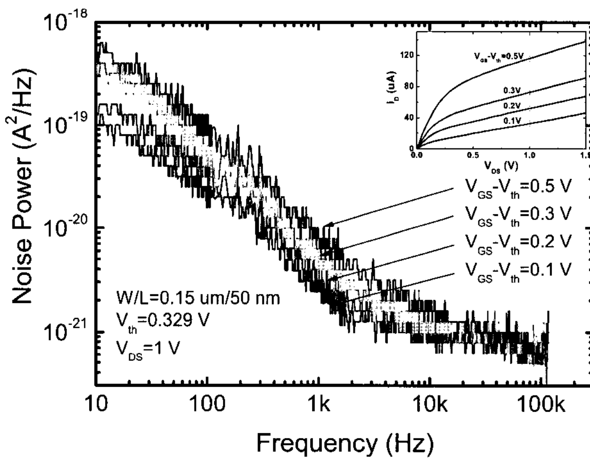


**Fig. 2.** 1/f noise spectra in n-channel MOSFETs with the gate voltage as a parameter. The device has a $W/L$ of 0.15 μm/50 nm. The $V_{GS}$-$V_{th}$ is fixed at 0.2 V.

Figure 2 shows measured 1/f noise power spectra of n-channel device as a parameter of $V_{GS}$ at a fixed $V_{DS}$ of 1 V. We measured another device with the same size ($W/L$ =150 nm/50 nm), and the device shows a big difference in the noise spectra, compared with those in Figure 1. The noise power spectrum density increases since the drain current increases as the $V_{GS}$ increases.

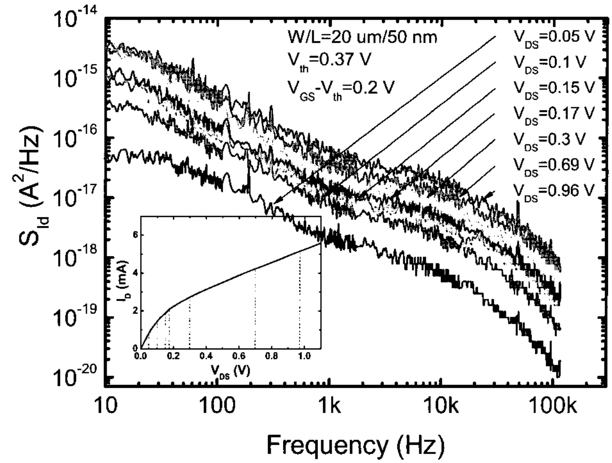


**Fig. 3.** 1/f noise spectra in n-channel MOSFETs with the drain voltage as a parameter. The device has a $W/L$ of 20 μm/50 nm. The $V_{GS}$-$V_{th}$ is fixed at 0.2 V.

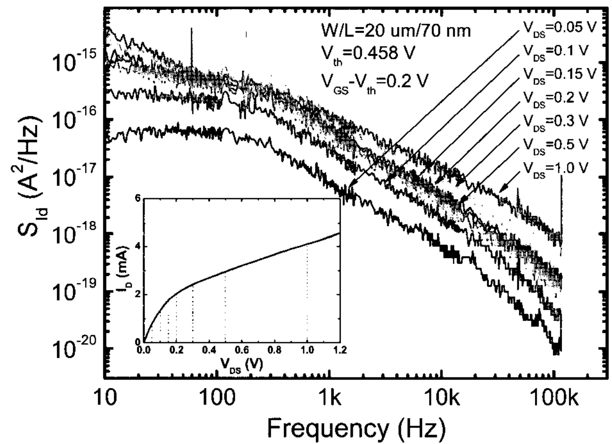


**Fig. 4.** 1/f noise spectra in n-channel MOSFETs with the drain voltage as a parameter. The device has a $W/L$ of 20 μm/70 nm. The $V_{GS}$-$V_{th}$ is fixed at 0.2 V.

Figures 3 and 4 show the 1/f noise power spectra of n-channel devices with different gate length as a parameter of $V_{DS}$. The devices in Figures 3 and 4 have $W/L$'s of 20 μm/50 nm and 20 μm/70 nm, respectively. The 1/f noise of both devices is increased as the $V_{DS}$ increases. We can observe Lorentzian-like noise humps more clearly in the linear region than in the saturation region. These results show a good agreement with previous one [4]. In Figure 4, the hump near ~200 Hz becomes small as the $V_{DS}$ increases, which means the trap is roughly located near the drain-side.

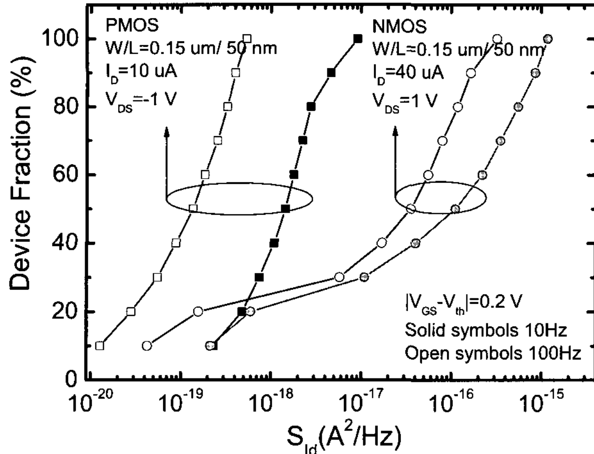


**Fig. 5.** Distribution of 1/f noise power of PMOS and NMOS devices at the same bias condition. The noise powers were sampled at frequencies of 10 Hz and 100 Hz.

Figure 5 shows the distribution of the 1/f noise power sampled at fixed frequencies of 10 Hz and 100 Hz for PMOS and NMOS devices with a *W/L* of 150 nm/50 nm. At fixed $|V_{GS}-V_{th}|$=0.2 V and $|V_{DS}|$=1 V, the PMOS device shows much better distribution and much lower noise power than the NMOS device.

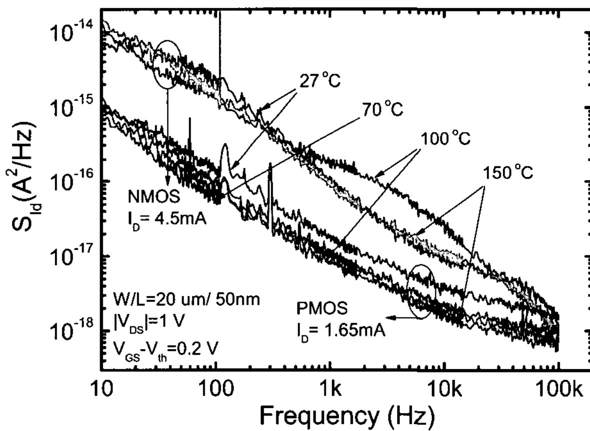


**Fig. 6.** 1/f noise spectra of n-channel and p-channel device for various measurement temperatures.

Figure 6 shows the temperature (*T*) dependence of 1/f noise power measured at $|V_{GS}-V_{th}|$=0.2 V and $|V_{DS}|$=1 V. The 1/f noise power of NMOSFET with a *W/L* of 20 μm/50 nm shows very small change with the *T* change (27~150 °C) [3] and no specific trend. It was reported that the slope of the spectra is decreased from 1.09 at 30 K to 0.84 at room temperature [3]. As the *T* increases, the 1/f noise power of PMOSFET with the same size decreases clearly over the frequency range higher than ~3 kHz at a fixed drain current of 1.65 mA (82.5 μA/μm). The slope of the noise spectra of the PMOS device was increased with increasing measurement *T*. Further study is required to understand those phenomena with *T*, and the noise spectra should be measured extensively.

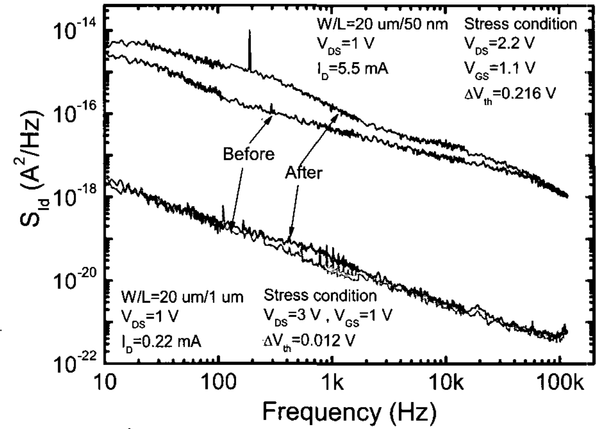


**Fig. 7.** 1/f noise spectra of n-channel device before and after hot carrier stress for two gate lengths. Both devices have the same channel width of 20 μm and different gate lengths (50 nm and 1 μm). The $V_{GS}-V_{th}$ is fixed at ~0.2 V.

Figure 7 shows the 1/f noise power in MOSFET before and after hot carrier stress (HCS) for two different gate lengths. The trapped-oxide charge and interface trap density are increased by the HCS, resulting in the increase of the 1/f noise power [5, 6]. As shown in Figure 7, the 1/f noise power in both devices is increased after the HCS. The increase of the 1/f noise with the HCS is more significant in short channel ($L_g$=50 nm) device than in long channel ($L_g$=1 μm) device since the electric field for hot carrier generation is stronger in short channel device. The $V_{th}$ shifts with the HCS are 216 mV in 50 nm device and just 12 mV in 1 μm device. The device with a *W/L* of 20 μm/1 μm shows ideal 1/f characteristics because the gate area is very large.

In Figure 8, the 1/f noise is shown for different gate lengths. The channel width is fixed at 20 μm and the gate length changes from 50 nm to 90 nm. As shown in Figure 8, the 1/f noise power in the devices is decreased as the gate length increases, which is proportional to $1/L_g^3$ [1]. To show the length dependence of 1/f noise power, the drain current is fixed at 40.5 μA and the drain bias is also fixed at 1 V.

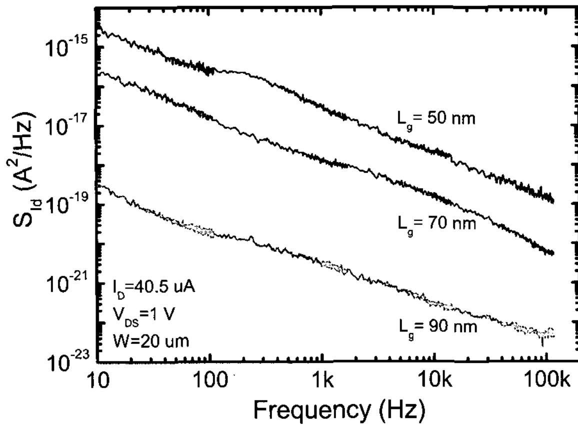


**Fig. 8.** 1/f noise spectra of n-channel device with the gate length as a parameter. The devices have the same channel width of 20 μm and different gate length (50, 70, 90 nm). The $I_D$ is fixed at 40.5 μA.

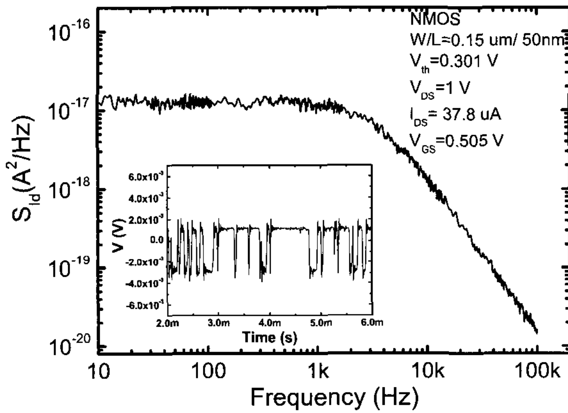


**Fig. 9.** 1/f noise spectrum and RTN of n-channel device with a *W/L* of 0.15 μm/50 nm.

Figure 9 shows the 1/f noise and RTN (Random Telegraph Noise) of the device with a *W/L* of 150 nm/50 nm. Generally, in long channel devices, it is not easy to observe the RTN since there are many kinds of traps. The measured device has a very small size (150 nm/50 nm) and we could find easily a Lorentzian-like noise hump at ~2 kHz in the device. The RTN is shown in the insert. There are two constant voltage levels. High voltage state is caused by emission of the charge in dominant trap and low voltage state is the capture of the charge in trap [3],[7].

## III. CONCLUSIONS

The 1/f noise in nano-scale MOS devices with various conditions was investigated. The Lorentzian-like noise was clearer in linear mode than in saturation mode of the devices. The 1/f noise with bias conditions was investigated as a parameter of device size. The 1/f noise in NMOSFET with a *W/L* of 20 μm/50 nm showed little change as the temperature increases, but the noise in PMOSFET with a *W/L* of 20 μm/50 nm showed clear decrease and slope change. The 1/f noise power with hot carrier stress increased more significantly in short channel devices than in long channel devices. The noise power at the same drain current decreased significantly with increasing gate length at a fixed channel width.

## ACKNOWLEDGMENTS

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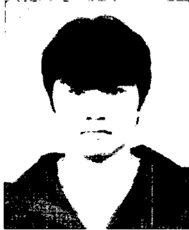

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