Highly Manufacturable 65nm McFET (Multi-channel Field Effect Transistor) SRAM Cell with Extremely High Performance

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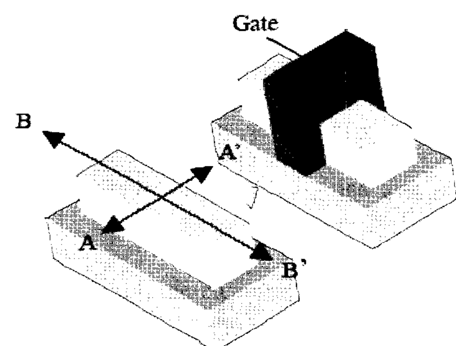
***Abstract*—We demonstrate highly manufacturable Multi-channel Field Effect Transistor (McFET) on bulk Si wafer. McFET shows excellent transistor characteristics, such as 5~6 times higher drive current than planar MOSFET, ideal subthreshold swing, low drain induced barrier lowering (DIBL) without pocket implantation and negligible body bias dependency, maintaining the same source/drain resistance as that of a planar transistor due to the unique feature of McFET. And suitable threshold voltage (V_T) for SRAM operation and high static noise margin (SNM) are achieved by using TiN metal gate electrode.**

***Index Terms*—McFET, SRAM, TiN, workfunction**

I. INTRODUCTION

Due to the high compatibility with conventional device manufacturing process, FinFETs have been on focus among the double-gate transistors[1]. Usually, as a fin width trimming method, a combination of sacrificial oxidation and chemical dry etch has been used. However, these methods inevitably increase the source/drain series resistance by narrowing the width of source/drain region as well as the channel fin region[2]. Moreover, to enhance the drive current, sophisticated multi-fin layout is required[3]. Due to the pitch limit of lithography tools, it is hard to have narrower pitch than design rule that limits the effective use of the active area for the devices using FinFET. In this work, we introduce a novel process architecture of McFET which can be fabricated without lithographical limit of active patterning and propose a method to achieve CMOS transistor characteristics that are suitable to low voltage and high performance operation using highly manufacturable TiN single metal gate process.



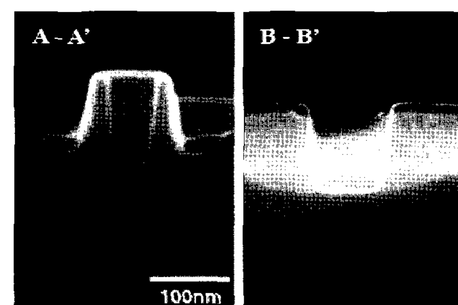


Fig. 1. Schematic illustration and cross-sectional SEM images of channel region of McFET.

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II. Fabrication

Three-dimensional schematic diagrams of the McFET fabrication process flow are shown in Figure 4[7~8]. As shown in Figure 2~5, the thickness of channel body is 12nm and it is uniform in the whole wafer. The nitrided oxide was grown as a gate dielectric. In order to test the intrinsic strength of the McFET architecture to resist short channel effect (SCE) and DIBL, no pocket implantations have been done. Figure 6 is the tilted-view SEM images of McFET in the middle of fabrication after gate spacer formation. To evaluate the threshold voltage (V_T) adjustment using gate workfunction engineering, single metal gate McFET also fabricated using simple replacement gate process. As a gate electrode, W/TiN is used as a gate material. TiN film of 10nm is inserted between the W gate electrode and gate insulator for threshold voltage adjustment. Figure 6 and Figure 7 show SEM and TEM images of successfully fabricated 65nm TiN single metal gate McFET SRAM cell transistors.

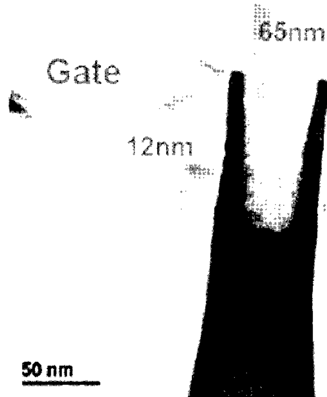


Fig. 2. TEM image of the channel body of fabricated McFET. The height and width of two symmetrical channel bodies are 98nm and 12nm, respectively.

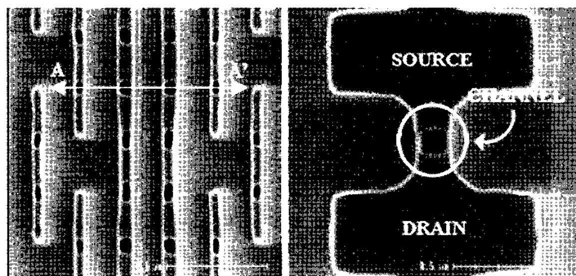


Fig. 3. Top view of McFET active channel formation.

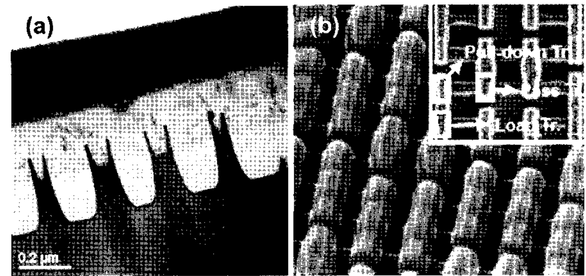


Fig. 5. TEM image of McFET SRAM cell along the 'Cut line A-A' in Figure 3 and tilted SEM view of McFET SRAM cell right after gate spacer formation with top view of 6T-SRAM cell. Channel profiles are uniform and symmetrical in whole wafer.

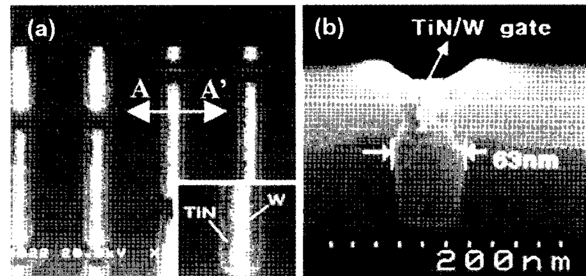


Fig. 6. SEM images of 65nm TiN gate McFET SRAM cell array (a) after TiN/W gate formation by CMP (tilted view), and (b) cross-sectional view cut along A to A'.

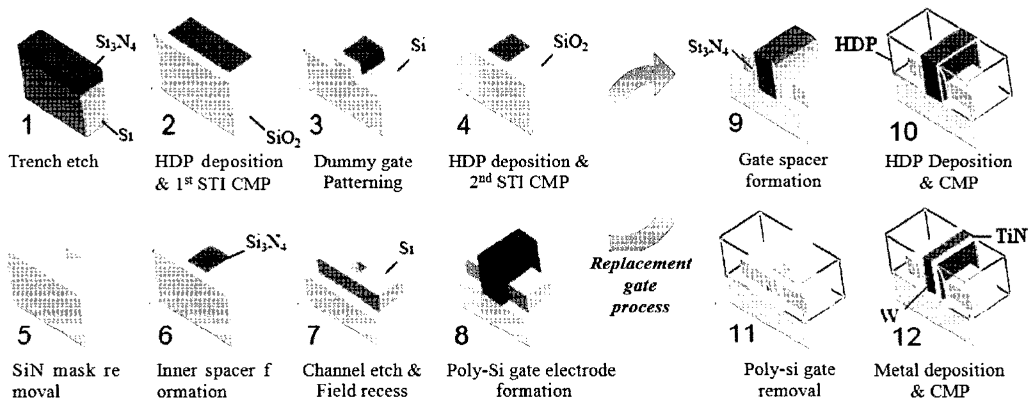


Fig. 4. Process flow sequence and 3-dimentional brief schematic diagram for poly-Si gate McFET fabrication and additional replacement gate process for TiN metal gate McFET.

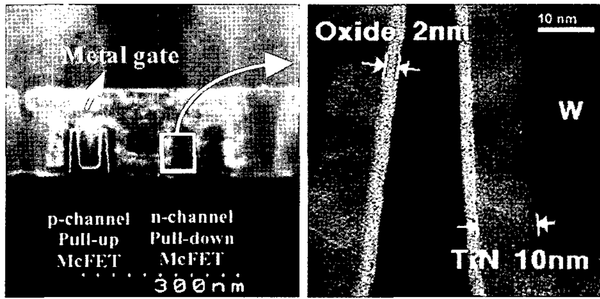
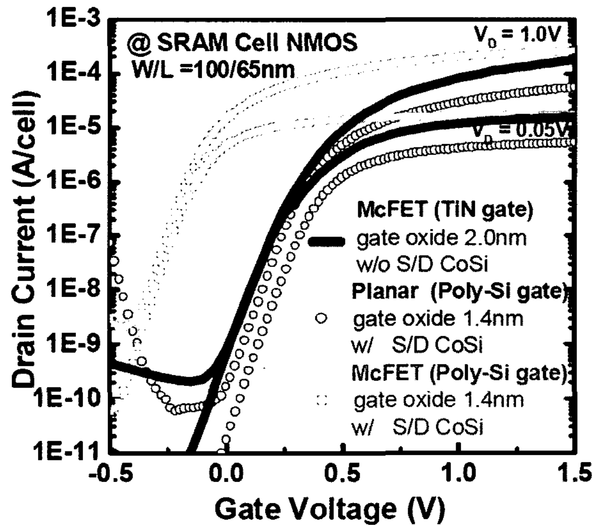


Fig. 7. Cross-sectional SEM and TEM images of 65nm TiN gate McFET SRAM cell transistor. TiN gate electrode is uniformly deposited on the gate oxide of 2nm.



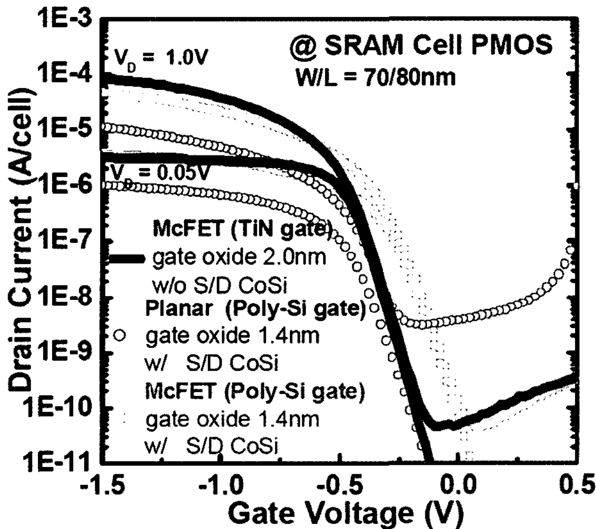


Fig. 8. I_D-V_G characteristics of McFETs and a planar transistor. Thanks to the gate work function matching with thin Si body, TiN gate McFETs show reasonably low threshold voltages with excellent short channel immunities.

III. Electrical Characteristics

Figure 8 shows the I_D-V_G curves for McFETs with TiN gate and poly-Si gate, and poly-Si gate planar MOSFET for SRAM cell application.

Thanks to thin channel body of McFET, SCE is effectively suppressed in spite of absence of pocket ion implantation and on current is enhanced. Due to the mid-gap workfunction of TiN, the V_T of TiN gate McFET increases 450mV for n-channel and 200mV for p-channel with respect to poly-Si gate McFET, which are suitable for the stable CMOS operation below 1.0V. Figure 9 shows no body bias dependency of McFET due to the fully depleted thin channel body. In addition, as shown in Figure 10, McFET shows 5~6 times larger current drivability than planar transistors. Thanks to the elimination of gate depletion using metal gate electrode, the drive currents of TiN gate McFET SRAM cell transistors with 2.0nm gate oxide are higher than that of poly-Si gate McFET and several times larger than that of poly-Si gate planar MOSFET with 1.4nm gate oxide.

Figure 11 shows the distribution data of McFET. Due to the uniform thickness of channel body and unique channel doping, McFET shows good in-wafer uniformity of threshold voltage and nearly ideal sub-threshold swing. Remarkably, thanks to nearly undoped channel and threshold voltage controlled by only gate workfunction engineering, TiN single metal gate McFET shows excellent distribution with optimal electrical characteristics for SRAM operation.

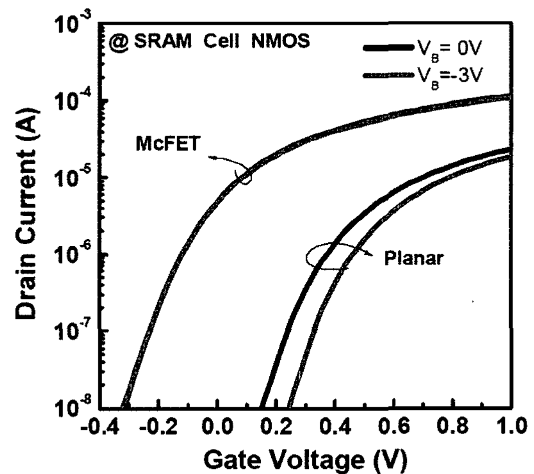


Fig. 9. Body bias dependency of the McFET and the planar transistor. No body bias dependency is observed in McFET.

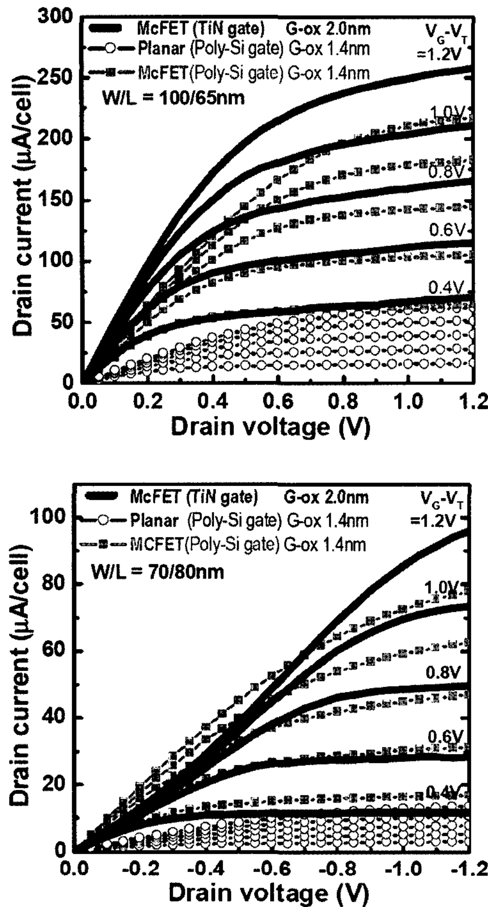


Fig. 10. Drive current of McFET SRAM cell PMOS is 5 times larger than that of planar transistor. Drive current dramatically increases using McFET scheme with TiN metal gate to eliminate poly depletion and effective channel width increase even with thicker gate oxide of 2.0nm.

As shown in Figure 12, the source/drain resistance of McFET is similar to that of planar MOSFET and abo ut 200 times lower than that of the other FinFET fab ricated with active trimming method. This is mainly due to the same source drain region with planar MOSFET, because only the channel region is trimmed.

To investigate the functionality of 6-T McFET SRAM cell array, SNM is evaluated. In case of poly-Si gate McFET, due to the low threshold voltage induced from thin body, static noise margin was not enough for SRAM working.(Figure 13) But in the case of TiN single gate McFET shown in Figures 14 and 15, having proper threshold voltage by adapting TiN gate to thin Si-body and large current drivability with channel width increase of McFET, TiN gate McFET SRAM cell shows 2 times larger SNM than poly-Si gate planar MOSFET. The SNM is 310mV at 0.8V. Due to the inherent stability of TiN gate McFET structure and process, all the test chips were operational with excellent SNM distribution in an 8 inch wafer.

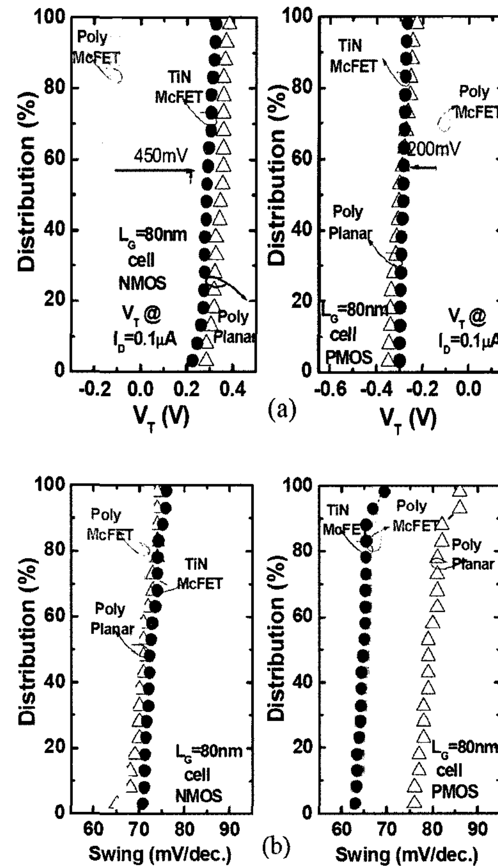


Fig. 11. Distribution of (a) threshold voltage (V_T) (b) sub-threshold swing of TiN gate McFET, poly-Si gate McFET and planar MOSFET. Thanks to intrinsic structural uniformity, McFET shows optimal uniform electrical characteristics for sub 1.0V operation.

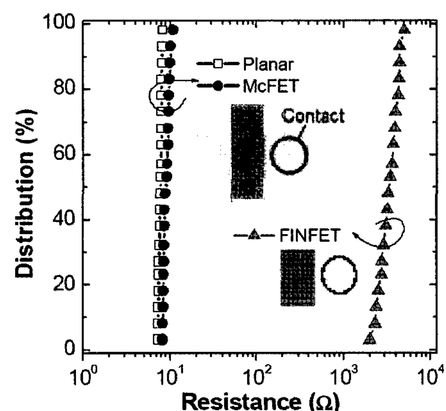


Fig. 12. Source/drain resistance of McFET is similar to planar MOSFET without any abnormal RSD increase of the other FinFET fabricated with active trimming method.

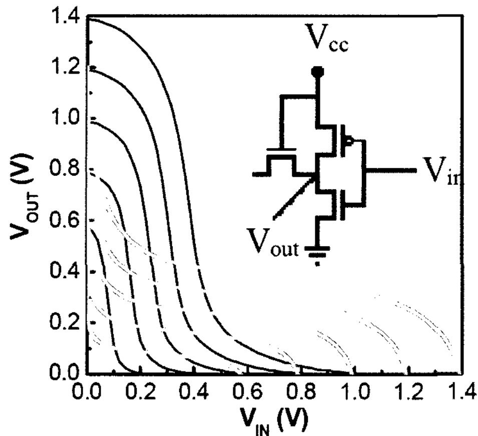


Fig. 13. 'Butterfly' curves for SRAM cell with poly-si gate McFET. Due to the low threshold voltages induced from thin body effect, static noise margin of poly-Si gate McFET was not enough for SRAM operation.

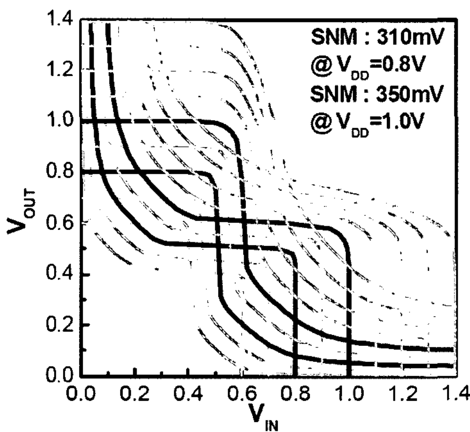


Fig. 14. TiN gate McFET 80nm 6-T SRAM cell shows large static noise margin due to the suitable threshold voltage and large driving current.

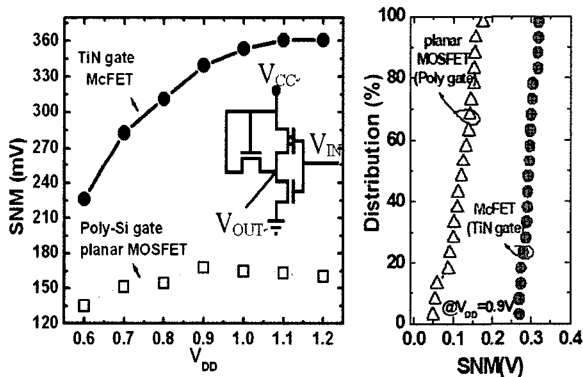


Fig. 15. The SNM of TiN gate McFET SRAM cell is more than 350mV at V_{CC} =1.0V and 310 mV at V_{CC} =0.8V with better distribution than poly-Si gate planar MOSFET in 8 inch wafer.

To examine the fine adjustment of V_T using ion implantation, local counter ion doping on top of fin channel was evaluated. The upper part of Si channel was partially doped using unique counter ion implantation process. Figure 16 shows threshold voltage shift of 70mV for n-channel McFET related to counter arsenic ion implantation of $2x10^{13}/cm^2$ with slight degradation of V_T uniformity. To examine the misalignment effect of the gate electrode to the hole on the active region, I_D-V_G characteristics were measured switching source and drain. As shown in Figure 17, 70nm poly-Si gate McFET misaligned by 20nm intentionally, did not induce any serious change in threshold voltage and I_{Dsat}.

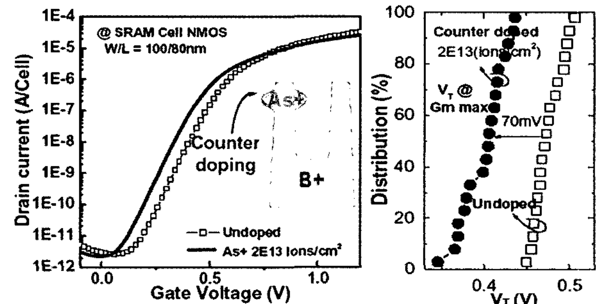


Fig. 16. For the fine tuning of threshold voltage (V_T), counter ion doping is applied. Threshold voltage shifts 70mV by $2x10^{13}$ (ion/cm^2) without off leakage current increase.

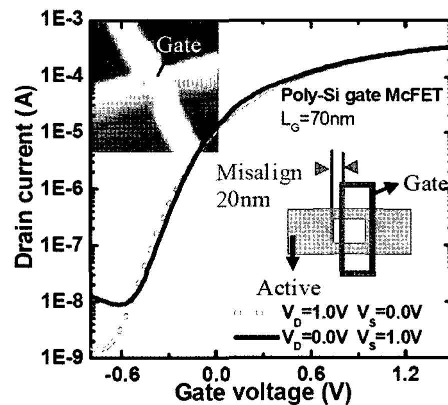


Fig. 17. Misalignment of 20nm between gate electrode and the hole on the active region does not induce any serious electrical characteristic change to 70nm McFET.

IV. Conclusions

A novel SRAM cell array McFET was successfully fabricated using highly manufacturable conventional CMOS process. It is realized that the McFET is highly effective to utilize the active area, overcoming the lithographical patterning limit. Using McFET structure,

drive current was increased 5~6 times with excellent short channel immunity. Optimal n-channel and p-channel threshold voltages for low voltage SRAM operation was achieved using the combination of midgap TiN metal gate and thin body double FinFET scheme of McFET. Single metal gate McFET was easily fabricated with simple replacement gate process. Excellent transistor performance and high SNM of 310 mV at 0.8 V was achieved.

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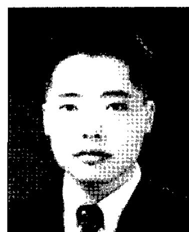

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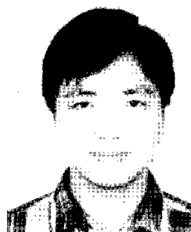

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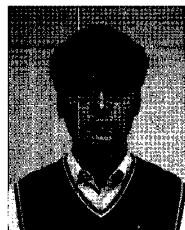

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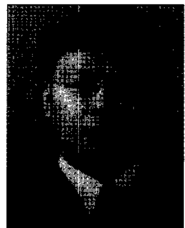

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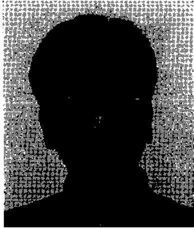

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