Fabrication of p-type FinFETs with a 20 nm Gate Length using Boron Solid Phase Diffusion Process

Won-Ju Cho

Abstract—**A simple doping method to fabricate a very thin channel body of the *p*-type FinFETs with a 20 nm gate length by solid-phase-diffusion (SPD) process was developed. Using the poly-boron-films (PBF) as a novel diffusion source of boron and the rapid thermal annealing (RTA), the *p*-type source-drain extensions of the FinFET devices with a three-dimensional structure were doped. The junction properties of boron doped regions were investigated by using the p^+-*n* junction diodes which showed excellent electrical characteristics. Single channel and multi-channel *p*-type FinFET devices with a gate length of 20-100 nm was fabricated by boron diffusion process using PBF and revealed superior device scalability.**

Index Terms—**FinFETs, 20 nm gate length, solid phase diffusion, ultra shallow junction**

I. Introduction

Metal-oxide-semiconductor field-effect-transistors (MOSFETs) is the most dominant electronic device in integrated circuit manufacturing. As the dimension of silicon MOSFETs shrinks to sub-100 nm regime, reducing the short channel effects becomes major efforts for the further scaling down of nano-scaled CMOS devices. One of the effects is a large subthreshold slope, which leads to a large leakage current. Another effect is a large drain-induced barrier lowering (DIBL), which causes an undesirable threshold shift as the drain voltage changes. To improve the short channel effects immunities, some modified MOSFET device structures have been proposed [1-3]. The double-gate MOSFETs is considered as the most promising device for CMOS scaling into deep sub-100 nm gate lengths [4-6].

This is because, for conventional bulk MOSFETs, the high concentration punch-through stopper ($>10^{18}$ cm^{-3}) is indispensable but results in severe drivability and leakage degradation. For the double-gate MOSFETs fabricated on the SOI substrate, the gate controls the energy barrier between the source and drain effectively. Therefore, the short channel effects can be suppressed without increasing the channel impurity concentration [7-9]. The FinFETs, a recently reported novel double-gate structure, consist of vertical Si fin controlled by self-aligned double-gate [10]. In spite of double-gate structure, the FinFETs are close to the conventional MOSFETs in layout and fabrication [11]. However, three-dimensional (3-D) device architecture of FinFETs leads to more complicate processing especially the doping of source/drain extension regions in comparison with the conventional planar CMOS transistors, which poses serious challenges to the device technology development in the sub-100 nm regime. Ion implantation with tilted-angle and the rotating implant process are indispensable for doping the long extension regions of FinFETs due to a high aspect ratio of fin extension regions [12,13]. The solid phase diffusion (SPD) process is an alternative doping method for 3-D device architecture and is also known as a defect-free process [14,15]. In SPD process, impurities diffuse into the silicon substrate from the doping source material by heat treatment. Therefore, shorter diffusion length and higher activation rates of diffused impurities are achieved compared to the conventional ion implantations.

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In this study, therefore, we investigated the fabrication of p-type FinFET devices by boron SPD process using a novel poly boron film (PBF) as a boron diffusion source. An extremely shallow (in depth direction) as well as a short (in lateral direction) p^+ junction was successfully formed. The p^+-n junction diodes with shallow junction depth and the FinFET devices with a 20 nm fin width were fabricated on the SOI substrate. The optimization of diffusion process using rapid thermal annealing (RTA) was carried out. The junction characteristics of p^+-n diodes and the electrical properties of FinEFT devices with a gate length of 20-100 nm fabricated by boron SPD were evaluated.

II. Experimental

The p-type SOI wafers with 200 nm buried oxide layer and 100 nm top silicon layer were used for p-type FinFET's fabrication. Hydrogen silsesquioxane (HSQ, Fox-12, Dow Corning) film with a 100nm thickness was coated on SOI wafers as negative tone inorganic electron beam resist with very high resolution. After the first electron-beam lithography (EBL) for formation of silicon fins, HSQ resists were developed in 2.38 % tetramethyl-hydroxyl-ammonium (TMAH) developers. Silicon fin channels with a width of 20 nm were obtained by EBL and Cl_2-based inductively coupled plasma reactive ion etch (ICP RIE) process. A gate oxide with a thickness of 4 nm was grown by dry oxidation and an in-situ phosphorus-doped polysilicon film with a 100 nm thickness was deposited as a gate electrode using the low-pressure chemical-vapor deposition (LPCVD). The secondary EBL was carried out to form the gate electrode patterns with 20-100 nm widths. After development of HSQ resist, the etching of the polysilicon gate electrode by Cl_2-based ICP RIE was followed. Then, the silicon nitride film with 20 nm thickness was deposited by LPCVD and was etched back by CHF_3-based RIE to form the sidewall spacer of gate electrode. A liquid-state dopant source containing boron (PBF, TOK, MMK-40) was used as a SPD source. A rapid thermal annealing (RTA) was carried out in N_2 ambient in order to diffuse the boron from the SPD source to the source-drain extensions of p-type FinFET devices. Secondary ion mass spectrometry (SIMS) was used to analyze the depth profiles of the boron atoms for various RTA process temperatures. The p^+-n junction diodes were also fabricated to investigate the junction properties formed by boron SPD.

III. Results and Discussions

Figure 1 shows the SIMS profiles of boron for various temperatures of RTA process. The boron atoms were gradually diffused from the doping source material (B_2O_3) layer to the silicon substrate by thermal energy and the diffusion length of the boron increased with increasing RTA temperature. In general, the substrate doping concentration of 4×10^{18} cm^{-3} is necessary to suppress the short-channel effect in the nano-scaled CMOS technologies. According to the International Technology Roadmap for Semiconductor (ITRS), the MOSFET devices with effective channel length (L_{eff}) below 100 nm require a junction depth X_j less than 47 nm [16]. From the results of this experiment, it is found that the formation of an ultra-shallow p^+ junction shallower than 20 nm is possible by low temperature RTA below 1000°C.

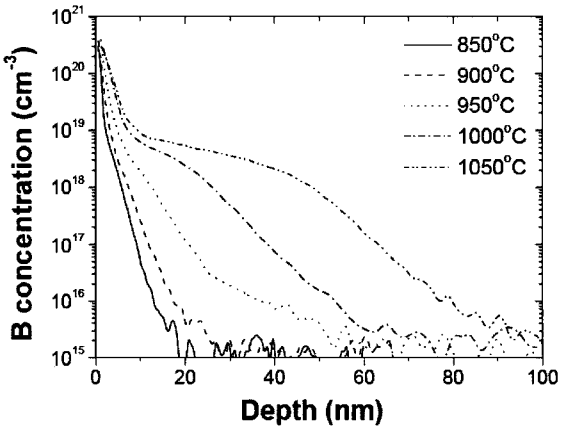

Fig. 1. SIMS profiles of boron for various RTA process temperatures using by using boron SPD.

Figure 2 shows the effect of RTA temperature on the sheet resistance (R_S) of boron diffused p^+-region. As the RTA temperature increased, the R_S decreased due to the diffusion of boron into the silicon substrate. When the RTA temperature was higher than 950°C, the R_S lower than 1000 Ω/cm^2 was achieved. Therefore, the relationships of R_S and X_j satisfy the demands for

source/drain extension (SDE) of p-MOSFET devices with a sub-100 nm gate length.

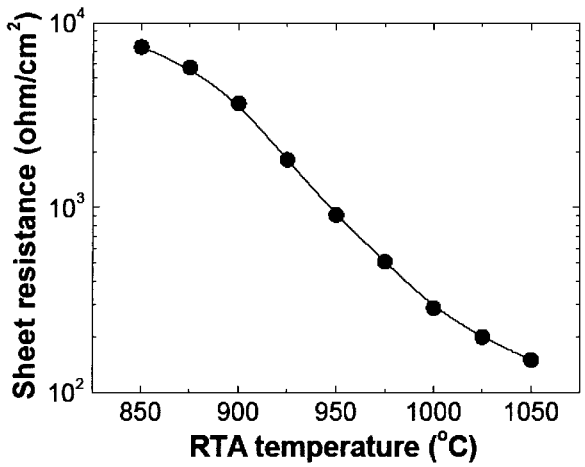

Fig. 2. Dependence of R_S on RTA temperature for a highly boron-doped region by SPD.

Figure 3 shows the current-voltage (I-V) characteristics of p^+-n diodes fabricated on the silicon substrate by SPD as a parameter of RTA temperature. The forward bias current increased with RTA temperature, which is attributed to the reduction of resistance at boron doped region. On the other hand, the reverse bias current was almost saturated at 950°C, because the solid phase diffusion (SPD) process is a defect-free doping method [14,15].

Figure 4 shows scanning electron microscope (SEM) images of fabricated multi-channel FinFET devices with a 20 nm silicon fin width. A 100-nm-thick HSQ layer

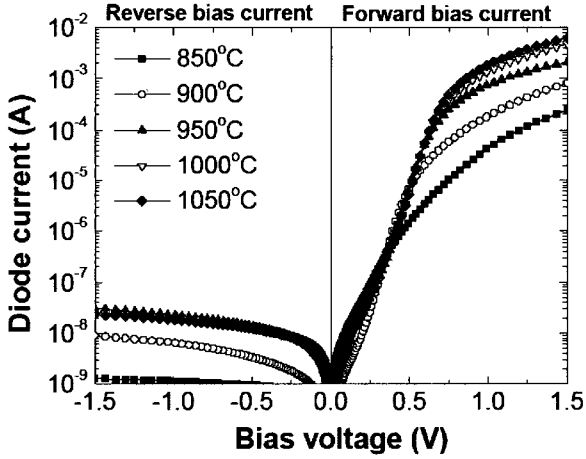

Fig. 3. Current-voltage(I-V) characteristics of p^+-n diode fabricated on silicon substrate by boron SPD methods with the parameter of RTA temperature.

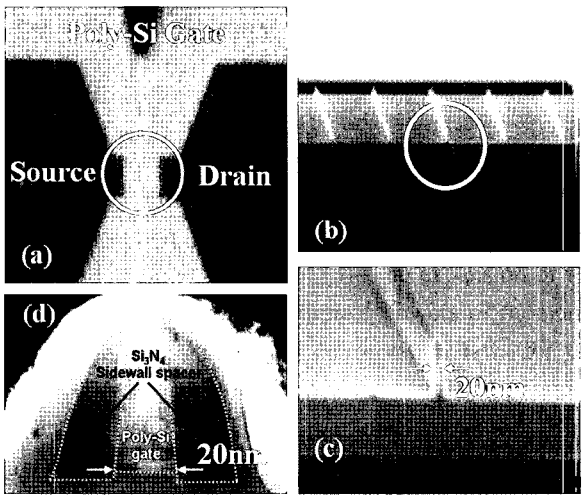

Fig. 4. SEM images of fabricated FinFET with a 20 nm silicon fin width.

was coated on the SOI layer for the generation of the ultra-fine fin-type single or multi-channel patterns, which also played a role as hard mask for the dry etching process. After definition of a fin pattern by using electron-beam lithography (EBL), the SOI layer was etched by the Cl_2-based RIE process. The 20 nm fin lines were successfully achieved with very good aspect ratio and sidewall smoothness as can be seen from Fig. 4(c). Also, the gate lines with 20-100 nm length were generated by similar method of fin pattern formation. Figure 4(d) shows the cross-sectional transmission electron microscopy (TEM) image of fabricated 20 nm gate line.

Figure 5 shows the subthreshold current characteristics (I_d-V_g) for the p-type FinFET devices as a parameter of gate length. The nitride sidewall spacer of gate electrode was 20 nm as shown in Fig. 4(d) and the SPD process was carried out by using the RTA at 950°C. The results obtained from the fabricated FinFETs with a 100 nm gate length showed good subthreshold characteristics. The threshold voltage (V_t) and subthreshold swing for this device were -0.96 V and 67 mV/dec, respectively. Because the large V_t is attributed to the n^+ polysilicon (phosphorus-doped) gate electrode, a lower threshold voltage can be obtained by using the p^+ polysilicon (boron-doped) gate electrode. However, the degradation of subthreshold swing, the roll-off of V_t and the increase of drain-induced barrier lowering (DIBL) were observed as the gate length decreases. In the case of 20 nm gate length, the threshold voltage, subthreshold swing and DIBL were -0.83 V, 97 mV/dec and 190 mV/V, respectively.

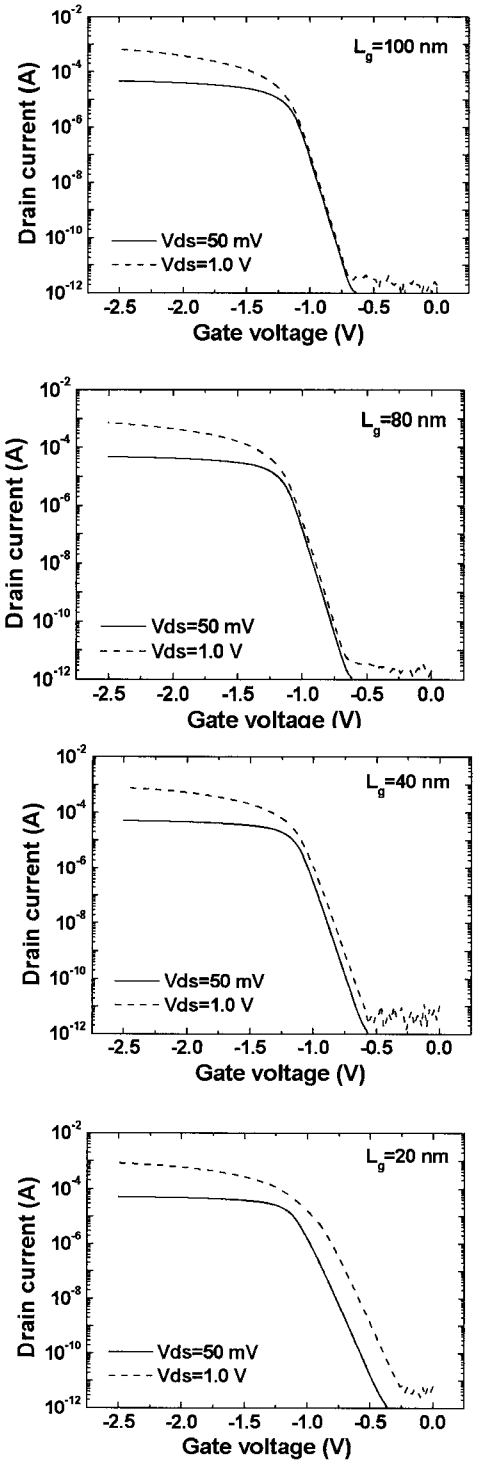

Fig. 5. I_d-V_g characteristics of p-type FinFETs fabricated by boron SPD.

Figure 6 shows the measured drain current (I_d-V_{ds}) as a parameter of gate length. The increase of drain current was observed as the gate length decreased due to the decrease of channel resistance. However, the short channel effect (SCE) was slightly observed in the 20 nm gate length FinFET devices. Nevertheless, it is considered that the boron SPD process PBF is excellent doping technique for the non-planar FinFET devices below a 50 nm gate length.

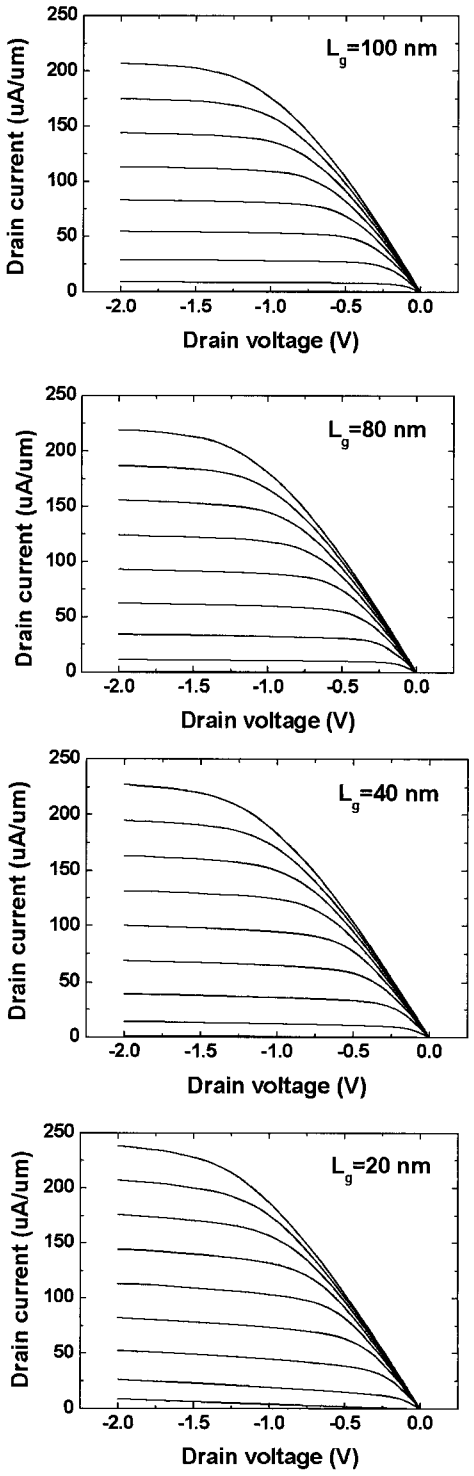

Fig. 6. I_d-V_{ds} characteristics of p-type FinFETs fabricated by boron SPD.

IV. Conclusions

A novel shallow-junction formation technique for the fabrication of *p*-type FinFET device with sub-100 nm gate length was reported. Using the boron SPD process with PBF diffusion source, the *p*-type FinFETs with gate length of 20-100 nm and the p^+-*n* junction diodes with extremely shallow junction depth were fabricated. Boron SPD was proved to be very effective process for sub-100 nm CMOS technology, because the p^+-*n* junction diodes with shallow junction depth and the *p*-type FinFET devices with a 20 nm gate length showed good electrical characteristics. Therefore, we concluded that the boron SPD process using the PBF is a promising doping technique for the further device scaling of nano-scale *p*-type FinFET devices.

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