Electrical Characteristics of Single-silicon TFT Structure with Symmetric Dual-gate for Kink Effect Suppression

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In this paper, a Symmetric Dual-gate Single-Si TFT, which includes three split floating n+ zones, is simulated. This structure drastically reduces the kink-effect and improves the on-current. This is due to the separated floating n+ zones, the transistor channel region is split into four zones with different lengths defined by a floating n+ region. This structure allows effective reduction in the kink-effect, depending on the length of the two sub-channels. The on-current of the proposed dual-gate structure is 0.9 mA, while that of the conventional dual-gate structure is 0.5 mA, at both 12 V drain and 7 V gate voltages. This result shows an 80 % enhancement in on-current. In addition, the reduction of electric field in the channel region compared to a conventional single-gate TFT and the reduction of the output conductance in the saturation region, is observed. In addition, the reduction in hole concentration, in the channel region, in order for effectively reducing the kink-effect, is also confirmed.

Keywords : Single silicon TFT, Kink effect, Dual gate

1. ITRODUCTION

In general TFTs, the output characteristics exhibit anomalous increases in the saturation current, often resulting in the kink effect. This added drain current makes the floating body harder, thereby causing regenerative action, leading to premature breakdown. This result also causes an increase in output conductance. Several undesirable effects in the electrical characteristics are created. The kink effect increases the power dissipation in the digital circuit and slightly degrades the switching characteristics, while the maximum attainable gain as well as the common mode rejection ratio in analog circuit applications are both reduced[1]. To overcome this kink-effect, several structures have been investigated, including drain offset, multiple gate, Lightly Doped Drain (LDD)[2], gate overlapped LDD (GOLDD)[3] and split LDD (SLDD). The conventional dual-gate structure has one floating n+ zone, therefore decreasing the leakage current exponentially increases with the drain field, while simultaneously reducing the on-current.

In order to suppress the kink-effect, the symmetric dual-gate structure with three split floating n+ zones is proposed, improving the on-current, compared to the conventional dual-gate TFT.

2. PROPOSED OF DUAL GATE AND CHARACTERISTICS

A SOG wafer was used for single-crystal silicon TFT. P-type wafer and pyrex 7740 wafer are bonded using an anodic bonding method. The device is fabricated using a 2-D numerical simulation program, ISE-TCAD. The simulation process is as follows; Single crystal silicon active layer 400 nm in thickness on 100 nm oxide was bonded by anodic bonding method at 380 °C, 700 V in a EBS-2000 A. The floating N+ regions are doped by im-planting Phosphorus at 100 keV with dose of 2×10^{15}, activated by annealing at 500 °C in nitrogen. The source and drain are doped by implanting P at 130 keV with dose of 4×10^{5}, activated by an anneal 550 °C in nitrogen. A 150 nm gate oxide is deposited by LPCVD. Molybdenum was

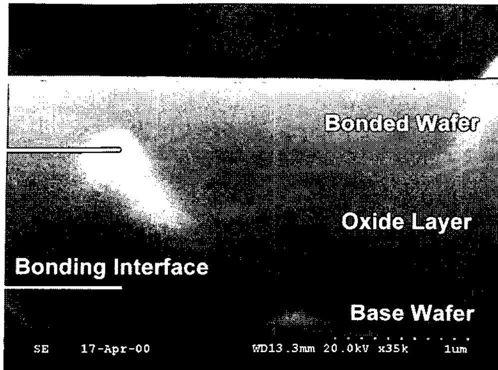


Fig. 1. A 100 nm oxidized SOG wafer.

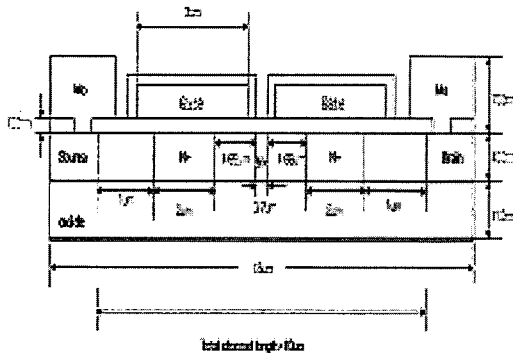


Fig. 2. Symmetric dual-gate TFT with three split floating n+ zones.

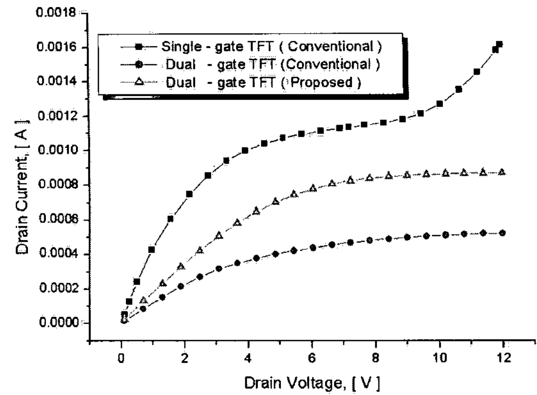


Fig. 3. The I-V characteristics for conventional single-gate dual-gate and the proposed dual-gate TFT (V_D=12 V, V_G=7 V).

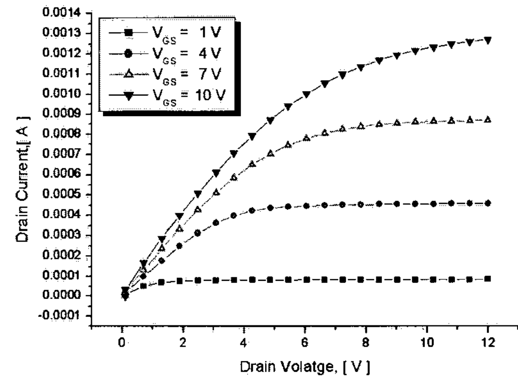


Fig. 4. Simulated I_D_V_D output characteristics of proposed dual-gate TFT (V_D=12 V, W/L=2).

subsequently deposited by sputtering, and patterned to form the gate as well as the metal contacts for 700 nm of the source and drain. Figure 1 presents a 100 nm oxidized SOG wafer, which has been fabricated. A cross section of the proposed dual-gate TFT structure is presented in Fig. 2.

3. RESULTS AND DISCUSSION

The electrical characteristics for the proposed TFT were observed. In addition, low hole concentration in the channel region with three split floating n+ processes was achieved. The low electric field at the edge of the drain region results in a drastic reduction in kink-effect. In addition, this structure improves the on-current, compared to conventional dual-gate TFTs.

3.1 The I-V output characteristics

Figure 3 presents the drain current - drain voltage output characteristics for the conventional single and dual gate TFT and the proposed dual gate TFT at V_G=7 V and V_D=12 V. The drain voltage range was from 0.1 V to 20 V and the gate voltage is fixed at 7 V. Both TFT channel lengths were 10 um, with a gate width of 20 um. The drain current of the conventional single gate TFT continuously increases in saturation. This effect is called the kink effect and the usual approach to reduce this effect is to limit the impact ionization contribution to decrease the electric field at the drain junction using a dual gate structure. Figure 3 demonstrates that the on-current of the conventional dual gate TFT is lower than that of the single gate TFT, because of the low electric field at the drain junction, this is the drawback of the dual gate structure.

The proposed dual gate TFT shows an improvement in the on-current, compared with the conventional dual gate TFT as presented Fig. 3. The on-current of the proposed dual-gate structure is 0.9 mA while that of the conventional dual-gate structure is 0.5 mA at both 12 V drain and 7 V gate voltages. This result shows an 80 % enhancement in on-current, due to the channel resistance reduction by two floating n+ zones. Figure 4 presents I-V output characteristics for the proposed dual-gate TFT at variable gate voltages.

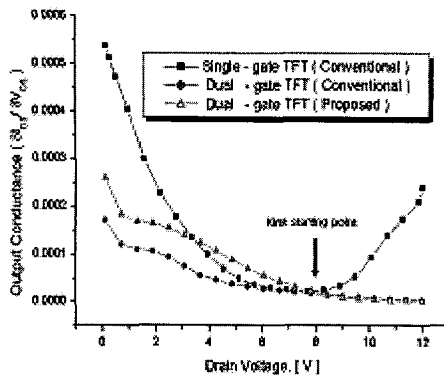


Fig. 5. The output conductance of proposed dual-gate TFT (V_D=12 V, V_G=7 V).

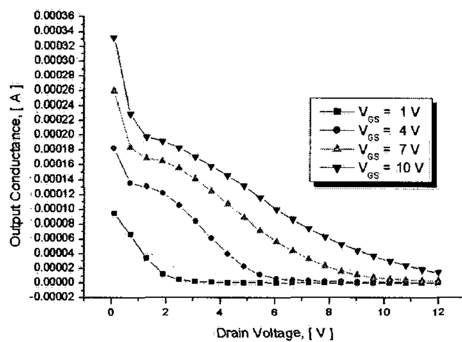
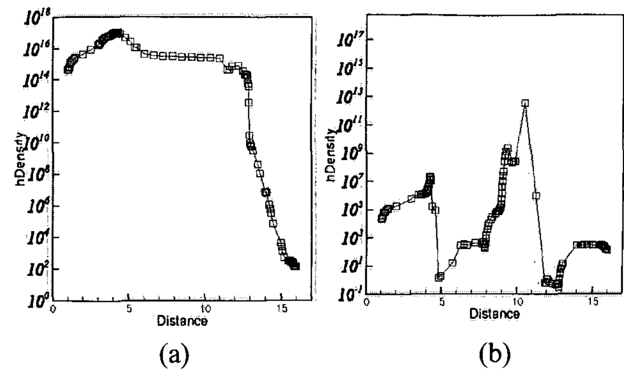


Fig. 6. The output conductance characteristics for different gate voltage of proposed dual-gate TFT (V_D=12 V).



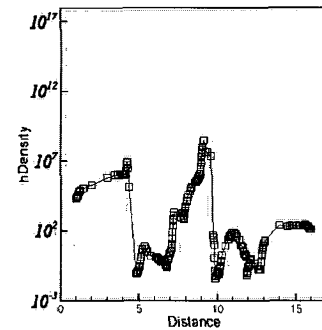


Fig. 7. Hole concentration in the channel region (cm^{-3}) (V_D=12 V, V_G=7 V): (a) The conventional single-gate TFT; (b) The conventional dual-gate TFT; and (c) The proposed dual-gate TFT.

3.2 The output conductance

Figure 5 presents the output conductance of the conventional single gate, the conventional dual gate TFT and the proposed dual gate TFT. The output conductance which continuously increases in the saturation region, means that the drain current is increasing. The kink effect of the proposed dual gate TFT is drastically reduced compared with the conventional single gate TFT, and an enhancement of the on-current rather than conventional dual gate TFT is observed, as shown in Fig. 3. Figure 6 shows the output conductance characteristics for a different gate voltage of the proposed dual gate TFT. The stable output conductance proves the prevention of the kink effect although the gate voltage increases.

3.3 The hole concentration characteristics

Figure 7 presents the hole concentration of the conventional single gate, the conventional dual gate TFT and the proposed dual gate TFT. The hole concentration is an important parameter in kink effect analysis. In conventional single gate TFTs, the holes generated by impact ionization at the drain junction can flow toward the source contact in the back-channel region and cause a potential barrier, lowering at the source junction (PBT action)[4]. The hole concentration of the proposed dual gate TFT at the source contact starting point (5 um) is very low because of the recombination between the floating n+ zones and holes. This result displays the prevention of the hole injection to the source contact to create a preclusion of the injection of the electron to the channel as shown in Fig. 7. The potential barrier is shown in Section 3.5 in detail.

3.4 The 2-dimensional electric field distribution

Figure 8 presents the electric field of the conventional single gate, the dual gate TFT and the proposed dual gate TFT. The electric field at a 13 um point in the proposed dual gate TFT is very low, compared with the conventional single gate TFT. In addition, the proposed dual gate is achieved at a lower electric field than that of the conventional dual gate TFT, making the reduction in kink effect significant. The low electric field in the proposed dual gate TFT is continuously kept at a low level, with the hole concentration and the reduction of the PBT action.

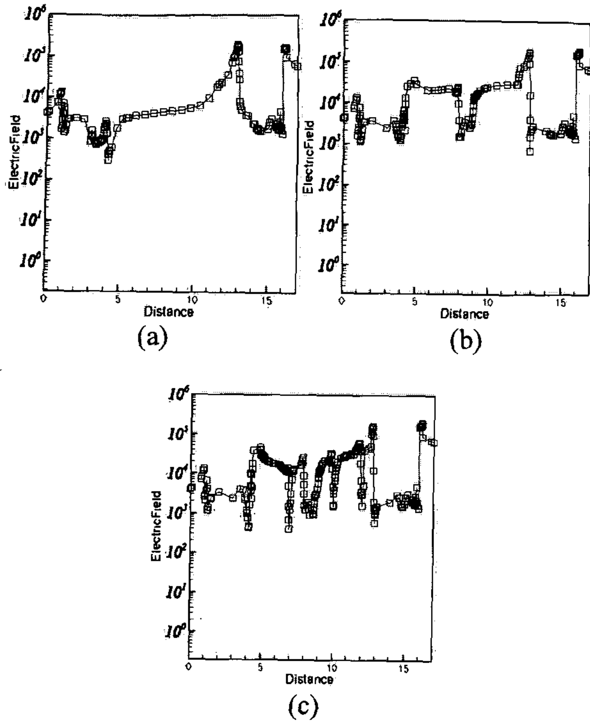


Fig. 8. The electric field in channel region (V) (V_D=12 V, V_G=7 V): (a) The conventional single-gate TFT; (b) The conventional dual-gate TFT; and (c) The proposed dual-gate TFT.

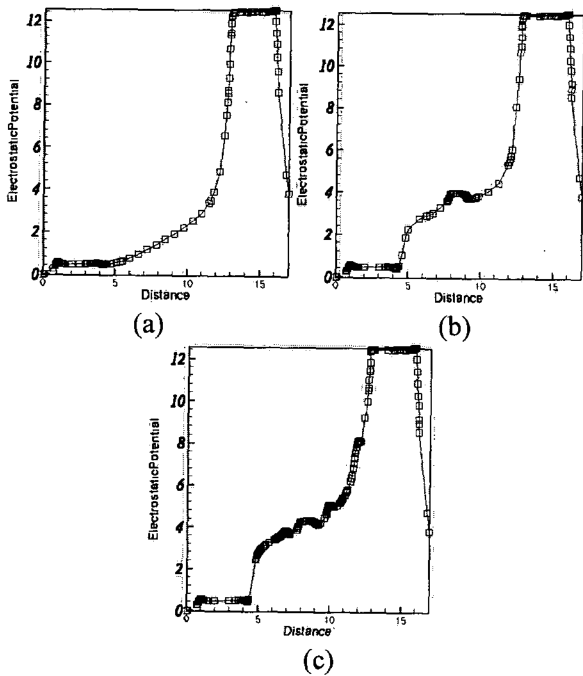


Fig. 9. The potential barrier distribution (V_D=12 V, V_G=7 V): (a) The conventional single-gate TFT; (b) The conventional dual-gate TFT; and (c) The proposed dual-gate TFT.

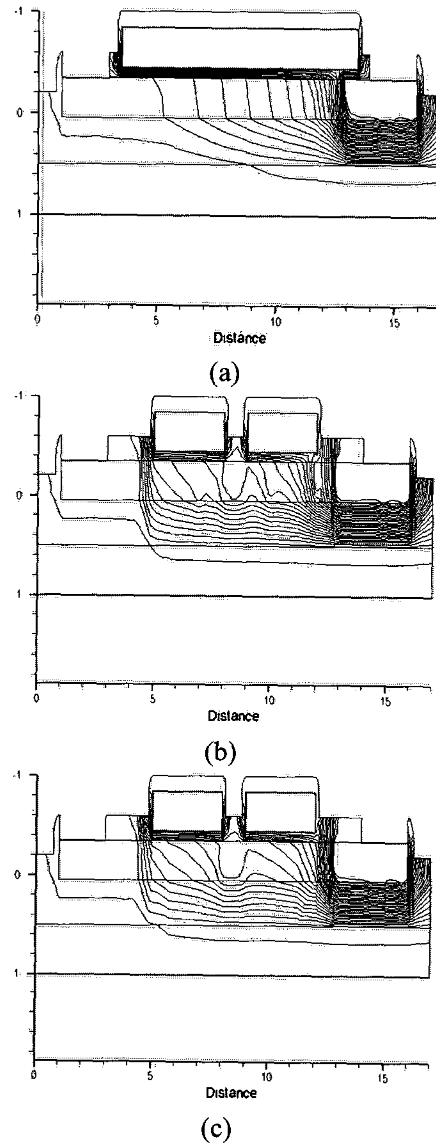


Fig. 10. The potential barrier distribution (V_D=12 V, V_G=7 V): (a) The conventional single-gate TFT; (b) The conventional dual-gate TFT; and (c) The proposed dual-gate TFT.

3.5 The 2-dimensional potential barrier distribution

As explained in the previous sections, the injection of electrons into the channel from the source contact lowers the potential barrier and consequently results in an increase in the drain current in the saturation region. Figure 9 presents the potential barrier of the conventional single gate, the dual gate TFT and the proposed dual gate TFT. The potential barrier of the proposed dual gate TFT is enhanced over that of conventional TFTs. This result increases the stability of output conductance because of the suppression of kink effect. Figure 10 shows the potential barrier of the cross section in the TFTs, with the length and height of the TFTs.

4. CONCLUSION

The new dual-gate TFT structure with three split floating n+ zones drastically reduces kink-effect. The stable output conductance is confirmed. It is observed that a reduction in hole concentration results in a reduction in kink-effect. In addition, the three split floating n+ zones causes a reduction of electric field at the drain/channel contact region, delaying premature breakdown. This structure demonstrated an improvement in on-current compared to conventional dual-gate TFTs. The on-current showed a 80 % enhancement, compared with the conventional dual gate TFT. Finally, the simulated single crystal silicon dual gate TFT structure appears very effective in limiting the kink-effect. In addition, if a doping element changes to As or An, instead of Phosphorus, a smaller channel length size of the TFT can be expected.

ACKNOWLOGYMENT

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