

Fabrication of Charge-pump Active-matrix OLED Display Panel with 64 × 64 Pixels

Se-Hwan Na[a], Jae Hoon Shim[b], Mi Young Kwak[*b], and Jong-Wook Seo[a]**

Abstract

Organic light-emitting diode (OLED) display panel using the charge-pump (CP) pixel addressing scheme was fabricated, and the results show that it is applicable for information display. A CP-OLED panel with 64 × 64 pixels consisting of thin-film capacitors and amorphous silicon Schottky diodes was fabricated using conventional thin-film processes. The pixel drive circuit passes electrical current into the OLED cell during most of the frame period as in the thin-film transistor (TFT)-based active-matrix (AM) OLED displays. In this study, the panel was operated at a voltage level of below 4 V, and this operation voltage can be reduced by eliminating the overlap capacitance between the column bus line and the common electrode.

Keywords : charge pump, active matrix, pixel addressing, OLED

1. Introduction

An OLED is one of the most promising technologies in flat-panel display area due to its benefits such as light-weight, wide viewing angle, self-emission, and rapid response [1]. Amongst these benefits, the potential of low manufacturing cost can be regarded as the most important one, and it is rooted in its simple structure compared to other competing technologies. However, a high information-density display requires not only the formation of OLEDs, but also the spatial separation and addressing of pixels [2]. Although a great effort has been put in to bring the TFT-based AM-OLED display into the market, the OLED still has a variety of problems that need to be solved such as threshold voltage shift of TFTs and the loss of aperture ratio due to the complexity of the circuitry [3,4].

A new easy-to-make charge-pump pixel circuit consisting of a storage capacitor and a rectifying diode has been proposed [5]. The new method provides a way to eliminate the need for the complex TFT-based pixel circuits. The basic operation of the circuit is to pump a fixed amount of charge into an OLED, and consequently drive an electrical current through the OLED during most of the frame period as in the TFT-based AM-OLED. Fig. 1 shows the schematic representation of the two-dimensional OLED cell array with charge-pump pixel circuits. In this paper, we investigate and discuss the fabrication of an OLED panel with 64 × 64 pixels by adopting the new addressing method and the analysis of the operation characteristics.

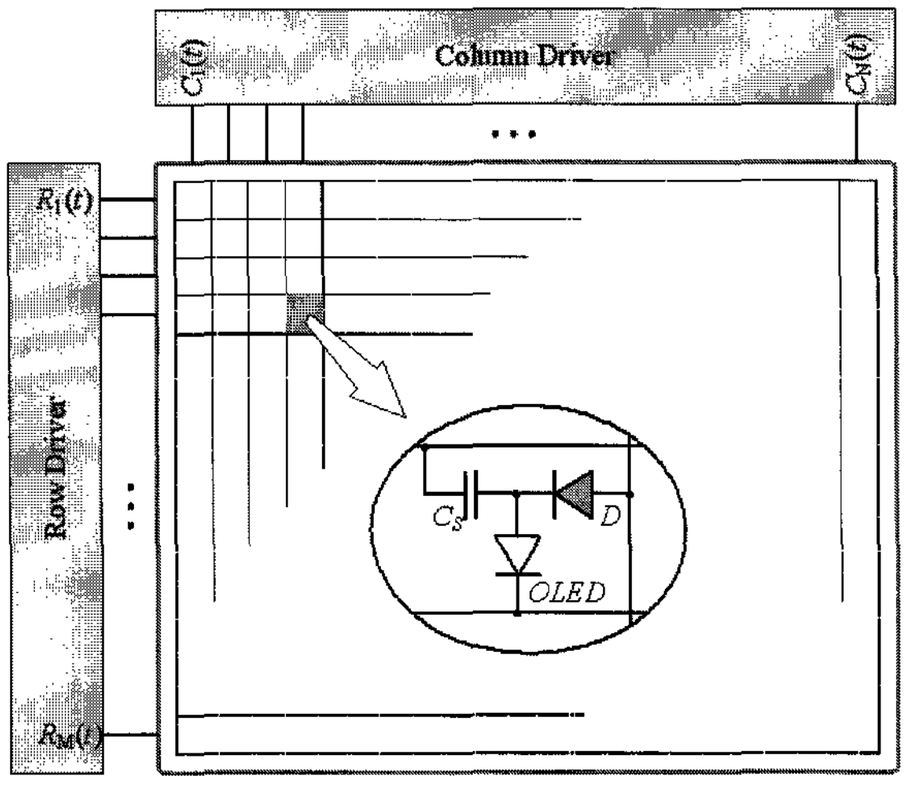

Fig. 1. Schematic representation of $M \times N$ OLED cell array with charge-pump pixel drivers.

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* Member, KIDS; ** Student Member, KIDS.

Corresponding Author : Jong-Wook, Seo

[a] School of Electronic and Electrical Engineering, Hongik University 72-1, Sangsu-dong, Mapo-gu, Seoul 121-791, Korea.

[b] Gracel Display Inc. 5F Samyangtechnotown, 284-25 Seongsu 2-ga, Seongdong-gu, Seoul 133-833, Korea.

E-mail : jwseo@wow.hongik.ac.kr **Tel** : +02 320-1663 **Fax** :+02-320-1119

2. Fabrication and Experiments

A CP-OLED panel with 64 × 64 pixels was fabricated by using conventional thin-film processes. The storage capacitors each of which covers the whole area of a pixel with an area of 490 × 490 μm^2 were formed by PECVD deposit of a 700 Å thick SiO_2 layer sandwiched between the row-bus lines (ITO) and the floating common electrodes (ITO). The rectifying Schottky diodes with an area of 100 × 50 μm^2 were formed by a 3000 Å thick hydrogenated amorphous silicon layer, which was deposited by PECVD. Fig. 2(a) shows the aerial and cross-sectional view of the pixel and the opening of the oxide (OLED window; 190 × 310 μm^2) down the ITO common electrode for the electrical contact of OLED. Fig. 2(b) shows the electrical connections between the layers showing that the floating ITO electrode acts as an electrode of the storage capacitor as well as the OLED anode and the Schottky diode cathode. Fig. 2(c) shows the fabricated CP-OLED panel finished with encapsulation and flexible printed circuit (FPC) cable bonding.

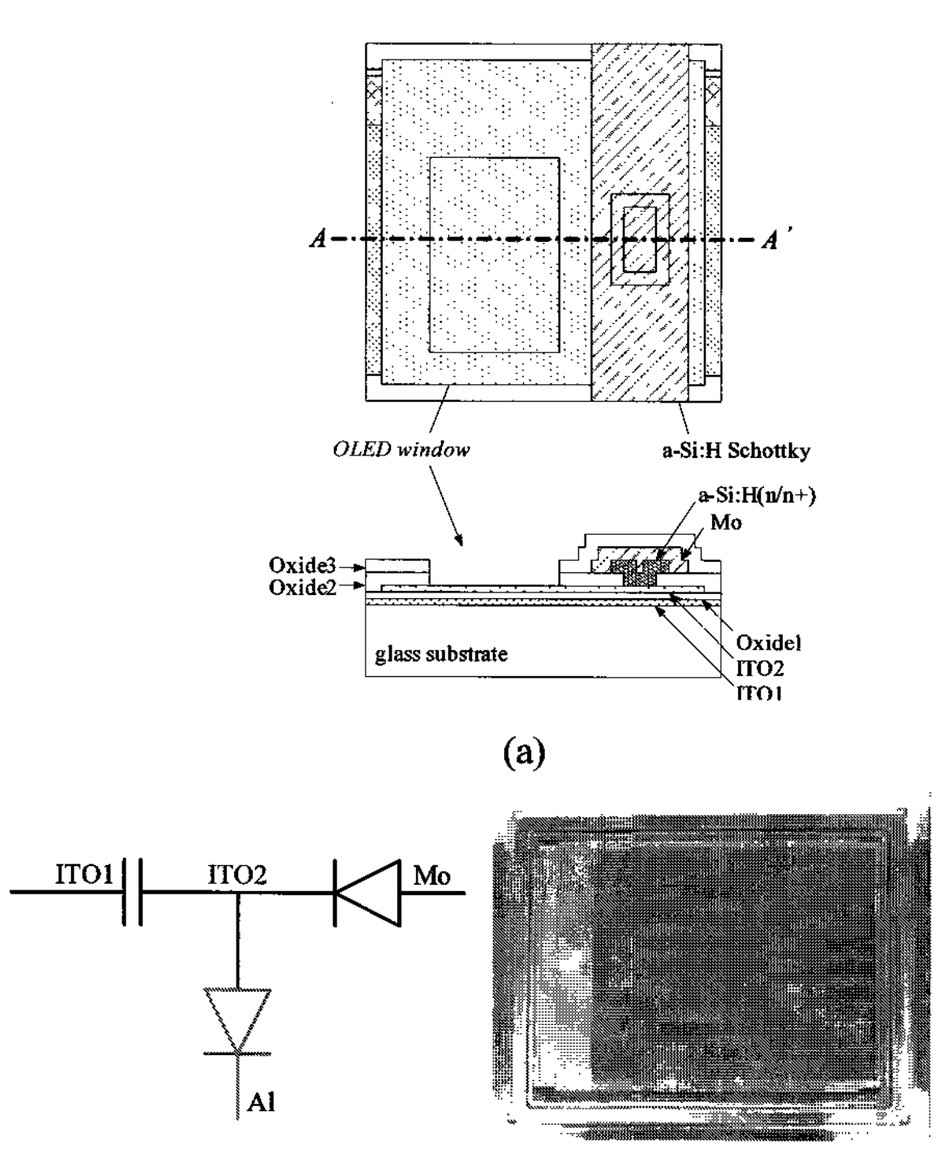


Fig. 2. (a) Aerial and cross-sectional view of the pixel. (b) Schematic representation of the cell structure. (c) Photograph of a panel completed with encapsulation and FPC (Flexible Printed Circuit) cable bonding.

The panel is controlled by a home-made digital electronics called the *Row Driver* and *Column Driver* (see Fig.1). Fig. 3 shows the typical waveforms of the display control signals from the row and column drivers. The basic operation of the circuit is to consecutively charge and discharge the storage capacitor through the rectifying diode (during the charging time) and the OLED (during the discharging time), respectively. The electrical current through the OLED is passed by the row-select signal $R_i(t)$ with a predetermined phase delay as shown in Fig. 3(a) where the two signals are those for adjacent rows. The light emission from an OLED cell during the discharging time can be turned on or off by making the column line voltage to be high or low rate, respectively, during the charging time by the action of column data signals $C_j(t)$ [5].

Since the control system used in the study is mounted with a field programmable gate array (FPGA) of insufficient number of gates to drive the whole 64 × 64 pixels independently, the panel was subdivided into common-circuited 2 × 2 array of 32 × 32 pixel arrays.

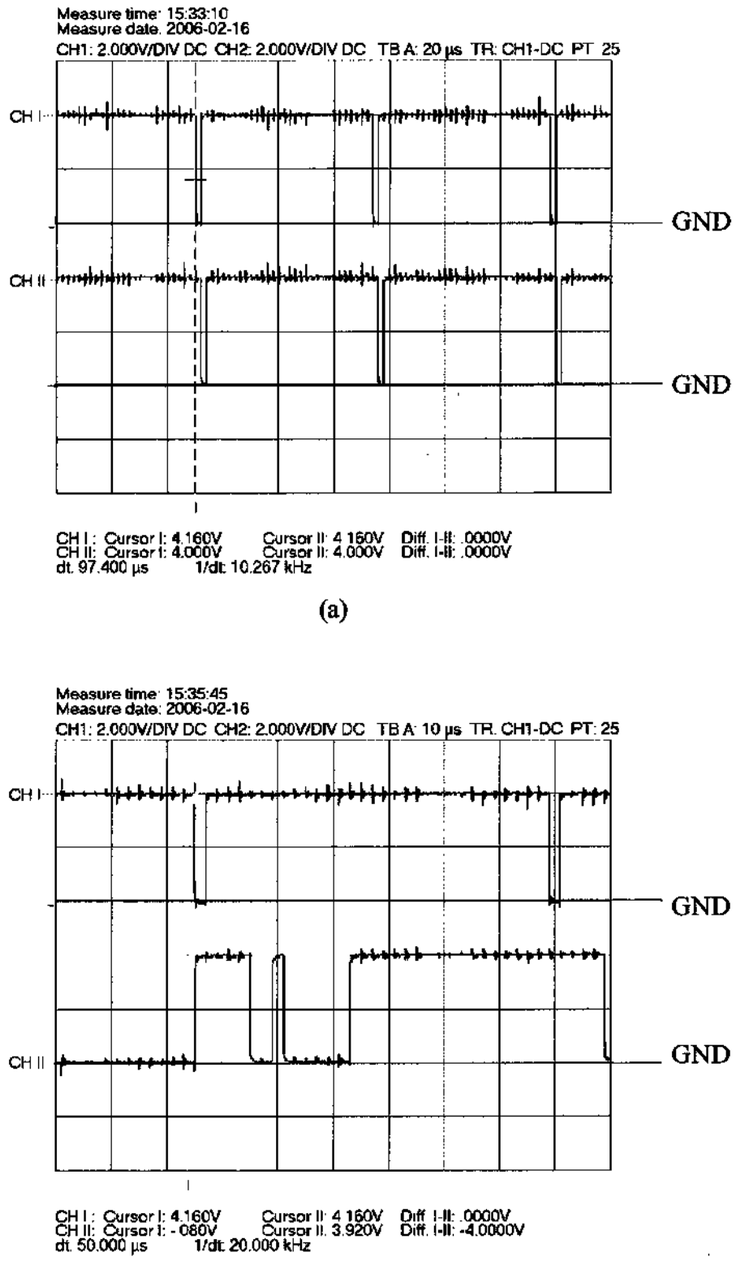


Fig. 3. (a) Row-select signal waveforms for 2 adjacent rows, and (b) a typical column data waveform with a corresponding row-select signal.

Control signals with a scan period of 65 μs $\left(=\frac{1}{60\text{ fps}\times 255}\right)$ and a charging time of 2 μs $\left(=\frac{65\,\mu s}{32}\right)$ were required to drive a 32 × 32 pixel array to perform an 8-bit gray scale with a frame rate of 60 fps. The gray scale control can be achieved using a method similar to the pulse width modulation (PWM) where the total number of charge-pumping during a frame period is controlled [6].

3. Results and Discussions

Fig. 4 shows the CP-OLED panel driven to display a test image. The Fig. on the left is the original bitmap image and the Fig. on the right is the photograph of the panel replicating the image. As can be seen from the Fig., the charge-pump pixel addressing method operates properly to display images. Considering that the pixel size scales down with the panel resolution, this method can be accepted as a suitable method for implementing high-information density OLED panels. The capacitive load for the drive circuit in a panel would not increase with the pixel density as smaller pixels are used. Meanwhile, it is noticeable from the figure that the relative brightness of the pixels is expressed differently from the original gray-scale data, and the deviation was found to be due to the crosstalk between pixels caused by the overlap capacitance between the column bus and the common electrode. The overlap capacitance, however, could be minimized through the optimization of the pixel layout design. The line defects on top of the image are due to the incomplete contact between the panel and the FPC connectors, and the areal defects on the top left corner are due to the accidental over-voltage burn out occurred while setting up the operating conditions. The point defects were found to be mostly due to the electrostatic discharge (ESD). The bad section with darker pixels around the low right corner of the panel is believed to be due to the process fault that is related specifically to the a-Si:H deposition. Despite the foregoing unskillful conditions of the panel, it can be seen that the CP-OLED panel can be implemented by using the conventional thin-film processes.

Since the operation of CP-OLED is dependent upon the device characteristics, it is worth studying the relation between the device characteristics and the performance of

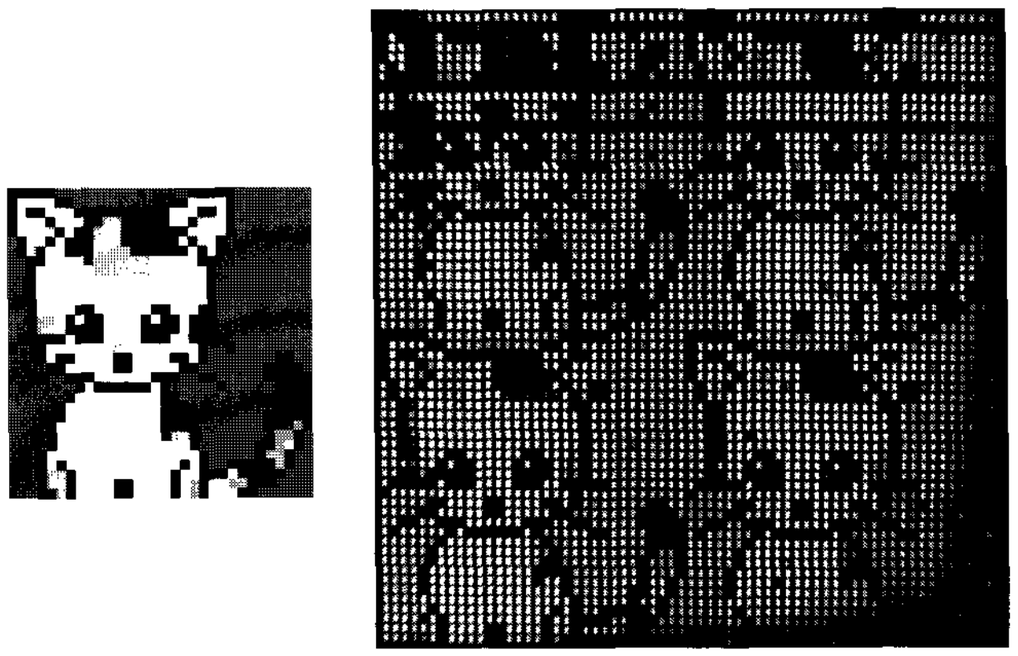
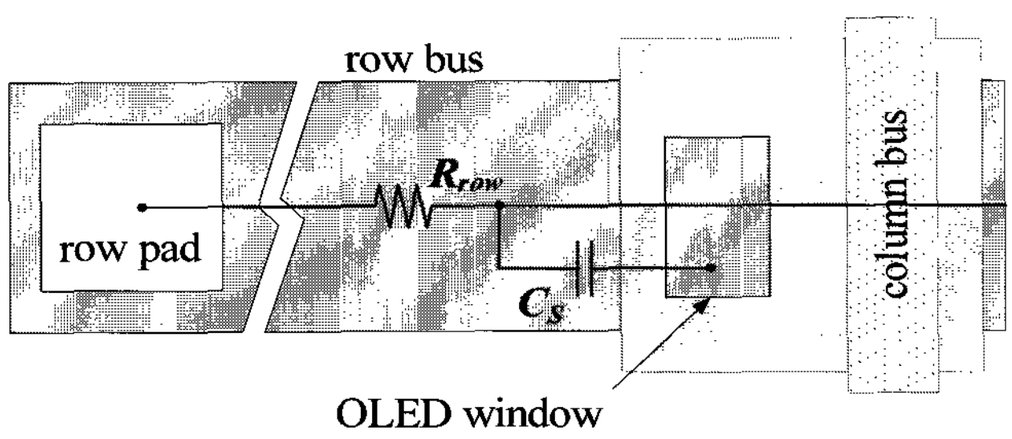
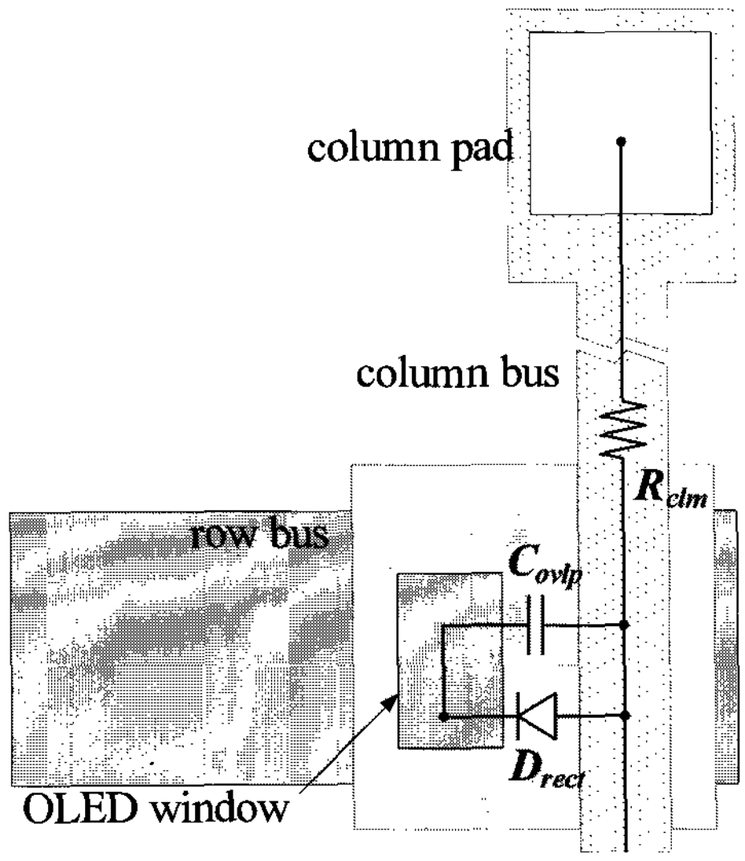


Fig. 4. Photograph of an OLED panel with 64 × 64 pixels displaying a test image. The panel was subdivided into common-circuited 2 × 2 array of 32 × 32 pixel arrays. The image on the left is the original test image.



(a)

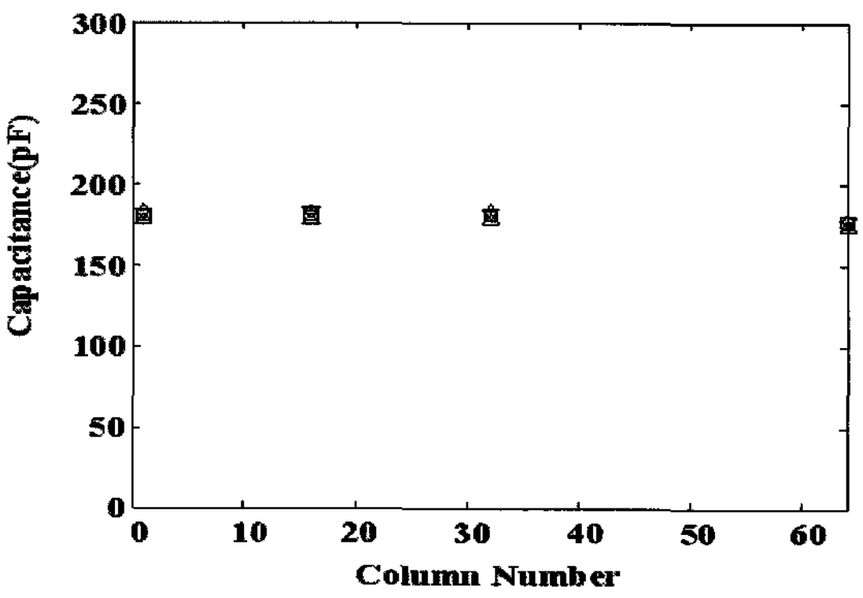


(b)

Fig. 5. Schematic representation between an FPC contact pad and an OLED window of a pixel for (a) row and (b) column bus line.

the display panel. Therefore, in this study the overlap capacitance between the column-bus and the floating common electrode, the storage capacitance, and the row- and column-bus line resistance were measured using an HP 4192A impedance analyzer. Since the row-bus line and the storage capacitance are connected in series as shown in Fig. 5(a), the row-bus line resistance R_{row} and the storage capacitance C_s can be obtained from the real and imaginary part of the measured impedance, respectively. Fig. 6(a) shows the measured storage capacitances for some pixels across the panel. From the Fig., it can be seen that the storage capacitance values distribute with a moderate uniformity at around 180 pF. In addition, the dielectric layer of the capacitors withstands the operating voltage of up to 10 V of operating voltage.

Since the column-bus line and the overlap capacitance are connected in series as shown in Fig. 5(b), the column-bus line resistance R_{clm} and the overlap capacitance C_{ovlp} can also be obtained in the similar way. Considering that the amplitude of the test signal for the impedance measurement is small enough to keep the diode from turning on and the diode junction capacitance is much smaller than the overlap capacitance, the effect of the a-Si:H diode can be ignored. The overlap capacitances were also found to have uniform values of about 130 pF. Fig. 6(b) shows the measured line resistances for the row- and column-bus. The abscissa is the column- and row-line number for the row- (□) and column-bus (○) resistance, respectively, and the slope is the bus line resistance per unit pixel. From the Fig., the bus resistance for row and column bus is 2.3 Ω/pixel and 5.9 Ω/pixel, respectively.



(a)

(b)

Fig. 6. (a) Measured storage capacitances of a CP-OLED backplane with 64 × 64 pixels along the 1st(□), 16th(◇), 32nd(△), and 64th(▽) row. Measurement was made at a frequency of 100 kHz. (b) Measured line resistances of row (□) and column (○) bus.

The *I-V* characteristics of the a-Si:H Schottky diodes were measured using the configuration shown in Fig. 5(b), and the diode turn-on voltages were found to have a large inhomogeneity across the panel as can be seen from Fig. 7. The saturation currents of the diodes were extracted from the data and were found to be uniform with a value of *IS*=5 pA, whereas the ideality factor *N* and the series resistance *RS* were found to vary drastically from 5.5 to 11.7 and from 170 Ω to 150 kΩ, respectively, across the panel. It means that the uniformity of the diode characteristics depends mainly on the electrical properties of the lightly-doped amorphous silicon and the junction formed with the metal (Mo) on it.

The performance of the panel was characterized by analyzing the display pattern of an image with a uniform

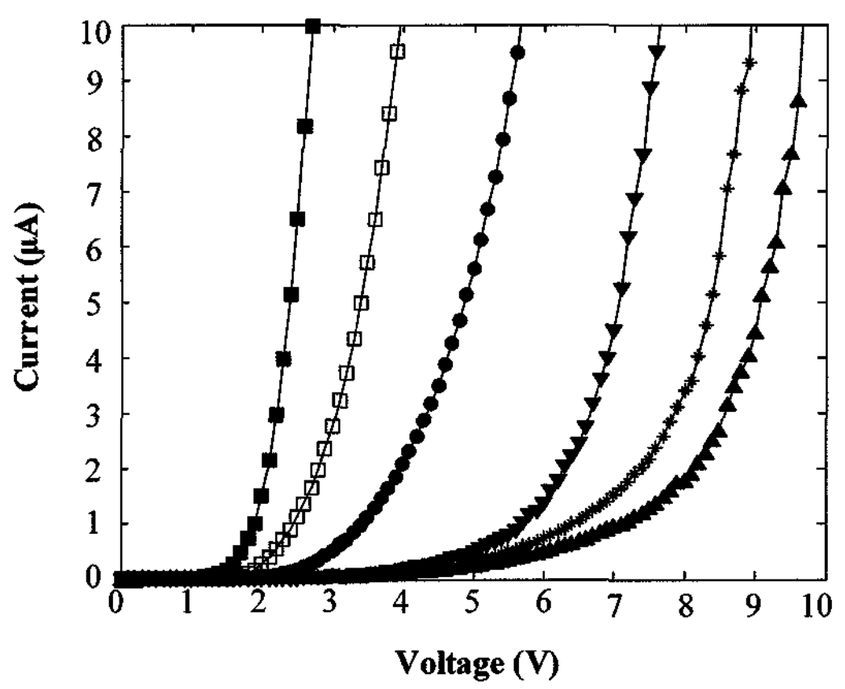


Fig. 7. Measured *I-V* characteristics of a-Si:H Schottky diodes at the 9th(■), 21st(●), 33rd(▼), 45th(*), and 57th(▲) row along the 9th column line. Also shown (□) is that of a diode at the 57th column of the 9th row.

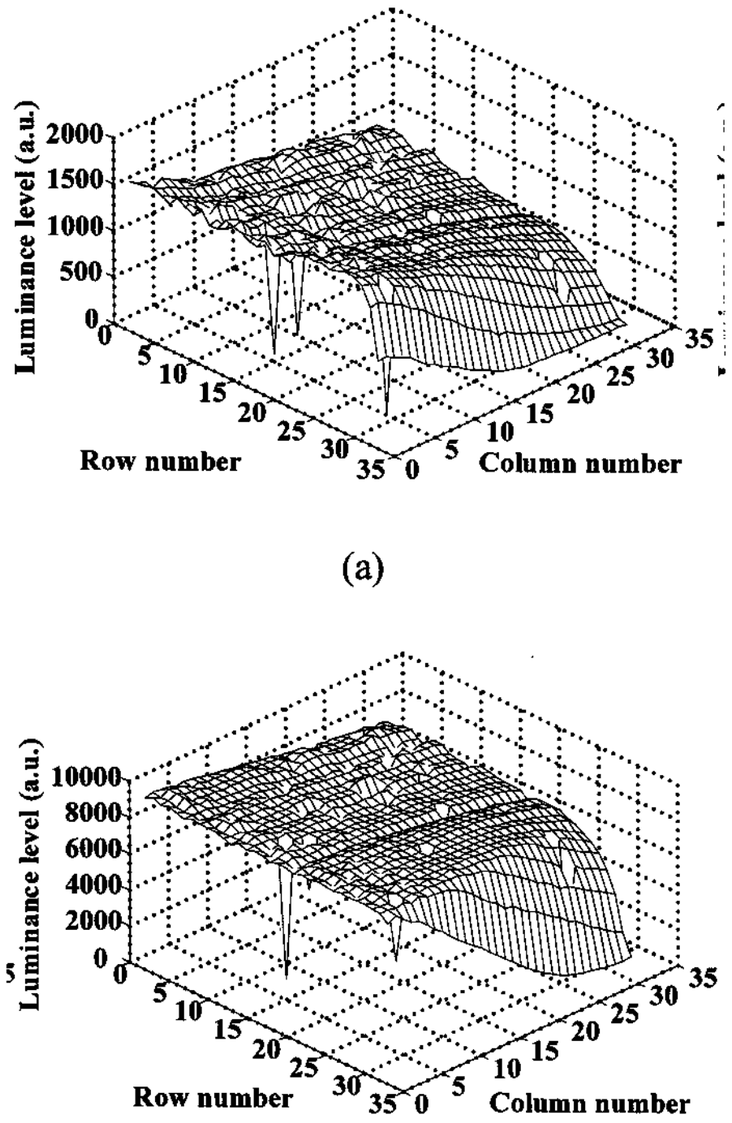


Fig. 8. Luminance variation for an "all white" image when driven by control signals with voltage amplitudes of (a) 3.0 V and (b) 3.8 V. The luminance variations along column lines at the 33 rd(□), 45 th(◇), and 57 th(*) row are translated into line graphs for driving voltages of (c) 3.0 V and (b) 3.8 V.

luminance as shown in Fig. 8. The display pattern from one of the subsections (32 × 32 pixels) was captured by a CCD camera *DTA Chroma-C*3, and the luminance data was obtained by subtracting the background luminance component from the captured data. The figure shows that the luminance variation is far more moderate than that of the a-Si:H Schottky diode turn-on voltage shown in Fig. 7. The charge pump action by the storage capacitance lessens the dependence of the cell luminance on the device characteristics. It can also be seen that the display performance becomes less sensitive to the device characteristics when driven by control signals with larger amplitudes. It can also be seen that the panel luminance is highly dependent on the amplitudes of the control signals. That is, as the amplitude is increased from 3.0 V to 3.8 V, the panel luminance increases up to more than 6 times.

Meanwhile, the non-ideal behavior observed in gray scale representation such as non-linear dependence of the luminance on gray-level data and crosstalk between pixels are mainly related to the overlap capacitance that exists between the column-bus and the common electrode (ITO). Since the charge-pump circuit is activated by switching on the rectifying diode, the overlap capacitance connected in shunt with the diode need to be minimized to maximize the voltage applied to the junction. It was found that the presence of the overlap capacitance results in loss of pixel luminance. The overlap capacitance also jeopardizes the electrical isolation between the column-bus and the common electrode resulting in crosstalk and loss of contrast ratio.

4. Conclusions

Through this study, it was confirmed that the charge-pump pixel addressing can be applied to high information density OLED display panels. A CP-OLED panel with 64 × 64 pixels with an area of 490 × 490 μm^2 was fabricated and driven to display images. A CP-OLED pixel consists of a storage capacitor and an a-Si:H Schottky diode, and the gray scale is controlled in a full digital way similar to the pulse width modulation. Although the performance of the panel is largely limited by the unripe processes, the devices fabricated using conventional thin-film processes have been verified to be suitable for implementation of CP-OLED panel. The panel was driven by control signals with voltage

amplitude below 4 V. Considering that the panel brightness is sacrificed by the presence of the overlap capacitance, it is expected that the operating voltage can be reduced further for power efficient operation.

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