

Threshold Voltage Control of Pentacene Thin-Film Transistor with Dual-Gate Structure

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Abstract

This paper presents a comprehensive study on threshold voltage (V_{th}) control of organic thin-film transistors (OTFTs) with dual-gate structure. The fabrication of dual-gate pentacene OTFTs using plasma-enhanced atomic layer deposited (PEALD) 150 nm thick Al_2O_3 as a bottom gate dielectric and 300 nm thick parylene or PEALD 200 nm thick Al_2O_3 as both a top gate dielectric and a passivation layer was investigated. The V_{th} of OTFT with 300 nm thick parylene as a top gate dielectric was changed from 4.7 V to 1.3 V and that with PEALD 200 nm thick Al_2O_3 as a top gate dielectric was changed from 1.95 V to -9.8 V when the voltage bias of top gate electrode was changed from -10 V to 10 V. The change of V_{th} of OTFT with dual-gate structure was successfully investigated by an analysis of electrostatic potential.

Keywords : Pentacene, Threshold voltage, Dual-Gate, Organic Thin Film Transister(OTFT)

1. Introduction

Organic electronics have recently become a promising technology for applications requiring low-cost, large area coverage, mechanical flexibility, and low temperature processing. Among them, organic thin film transistors (OTFTs) have been proposed for various applications of electronic circuits, including radio-frequency identification (RFID) tag, digital paper displays, back planes for flexible active-matrix liquid crystal displays (AMLCDs) and organic light-emitting diodes (AMOLEDs)[1,2]. Over the decades the device performances of OTFTs have improved dramatically. The carrier mobilities of OTFTs are similar to or even higher than those typically obtained with hydrogenated amorphous silicon TFTs, which have found widespread use in AMLCDs [1]. In particular, the OTFTs based on pentacene have received considerable attention in recent years due to their superior performances that include high field-effect mobility and large on/off current ratio [1]. Other issues that remain to be investigated with respect to the development and the mass-production of practical OTFTs are the improvement of passivation performance and the control of electrical parameters such as threshold voltage (V_{th}) and on-current. These problems can be simultaneously solved using dual-gate (DG) OTFT. Furthermore, the dual-gate geometry adapts to different bias configurations and offers higher flexibility of operation with respect to single-gate devices. Recently, the results on the control of V_{th} of pentacene and polymer OTFT with DG structure have been reported [3-5]. In this work, the control of electrical parameters and the long-term stability of DG OTFTs were investigated and discussed.

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2. Experimental Details

Si wafers with thermally grown 300 nm SiO_2 were used as substrates for these experiments. A 50 nm Ti was deposited by e-beam evaporator through a shadow mask for the patterned bottom gate electrode (G1). A PEALD 150 nm thick Al_2O_3 film was deposited at 150 °C to form bottom gate dielectric using trimethylaluminum (TMA) precursors and O_2 gas mixed with N_2 gas. The breakdown field of 9 MV/ cm and the capacitance (C_{ox}) of 41 nF/cm^2 were obtained in our PEALD Al_2O_3 [6]. Source (S) and

drain (D) consisting of 3 nm thick Ti and 80 nm thick Au layers was deposited on top of Al_2O_3. The bottom gate dielectric surface was treated with hexamethyldisilane (HMDS) as the self-organizing materials, which improved the quality of the organic/dielectric interface [7], Then, a 100 nm thick pentacene layer was deposited. The substrate with bottom gate OTFT was then coated with a 300 nm thick parylene layer (C_{par}=7.15 nF/cm^2) or a 200 nm thick PEALD Al_2O_3 layer deposited at 100 °C (C_{Al2O3}=26.9 nF/cm^2). Parylene is a material commonly used as a passivation layer on top of pentacene layer [8] and the PEALD Al_2O_3 deposited at 100 °C is a recently developed new passivation material that does not damage the pentacene layer [9]. Finally, a 50 nm thick Ti layer was deposited to form the top gate electrode (G2). The cross-sectional structure and bias configuration of OTFT are schematically shown in Fig. 1. We evaluated the transfer characteristics of OTFTs using Keithley 4200 semi-conductor parameter analyzer in the dark at room temperature.

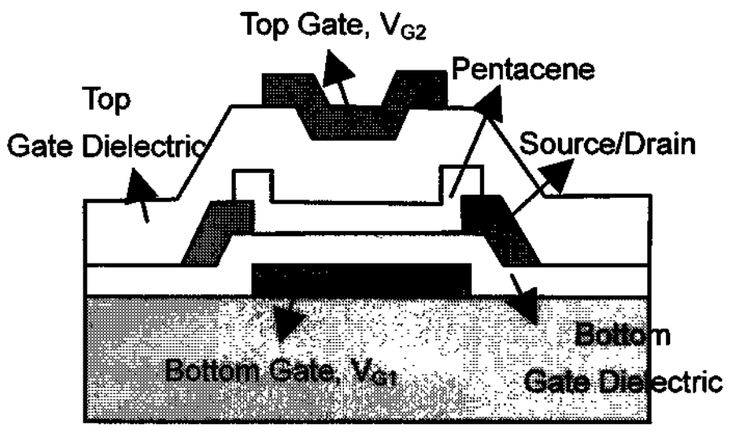

Fig. 1. Schematic structure and bias configuration of the bottom contact DG OTFT device.

3. Results and Discussion

The drain current (I_D)-gate voltage (V_G) curves in Fig. 2 show the transfer characteristics of the DG OTFT with PEALD 150 nm Al_2O_3 as a bottom gate dielectric and with 300 nm parylene as a top gate dielectric. The bottom OTFT of this DG structure had a saturation mobility of 0.01 cm^2/Vs, V_{th} of 4.7 V, subthreshold swing (SS) of 1.12 V/decade, and on/off current ratio of 6.3×10^5. Mobility and V_{th} were obtained from the linear fit of the plot, $I_D^{1/2}$ vs. V_G. In case of the OTFT with a top contact S/D structure using PEALD Al_2O_3, we obtained a saturation mobility of 0.1~0.5 cm^2/Vs. Even though the properties of top contact device was much better than those of bottom contact device, especially with respect to mobility, we adopted the bottom contact configuration in our consideration of the development and mass production of practical OTFTs and integration of inverter.

When V_{G2} was 0 V, the transfer curves of first and second scan were exactly identical. Based on this successive scan, we concluded that there is no bias stress effect in our devices which consists of a progressive shift of the V_{th} towards negative voltage as the gate electrode is biased and the stability of our device is enough for testing the control of V_{th} using the top gate bias. When V_{G2}, top gate bias was varied from -10 V to 10 V in steps of 5 V, the V_{th} of bottom OTFT was systematically shifted from 4.7 V to 1.3 V as shown in Fig. 2 (a). The top OTFT of the DG structure had a saturation mobility of 0.005 cm^2/Vs, V_{th} of -4.8 V, SS of 4.26 V/decade, and on/off current ratio of 1.2×10^5. When V_{G1}, bottom gate bias was varied from -10 V to 10 V in intervals of 5 V, the V_{th} of top OTFT was intensely shifted from 15.2 V to -20 V as shown in Fig. 2 (b).

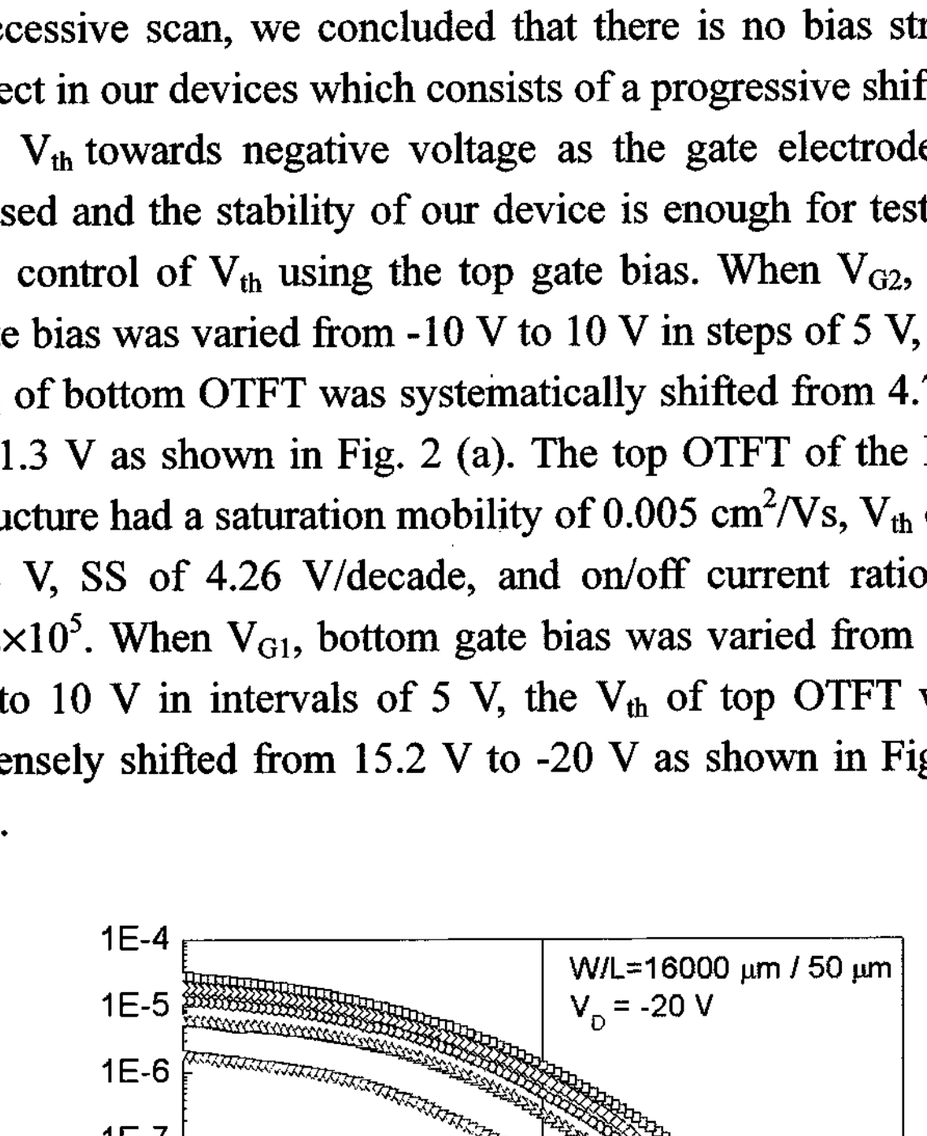

Fig. 2. (a) The change of transfer characteristics of the bottom OTFT of DG structure with the change of top gate bias, V_{G2} and (b) that of the top OTFT with the change of bottom gate bias, V_{G1}.

The shift in the transfer curve can be explained by the body effect in a Si transistor [10]. In a bulk device, the body effect is defined as the dependence of the V_{th} of the bottom gate OTFT on the top gate bias. The V_{th} as a function of top gate bias can be predicted from Eq. 1

$$\frac{dV_{th}}{dV_{G2}} = -\frac{C_{pen}C_{top}}{C_{bottom}(C_{pen}+C_{top})} \cong -\frac{C_{top}}{C_{bottom}} \quad (1)$$

where C_{bottom}, C_{pen}, and C_{top} are the capacitance of bottom gate dielectric, pentacene semiconductor, and top gate dielectric, respectively [11]. Fig. 3 shows the transfer characteristics of DG OTFT with PEALD 150 nm Al_2O_3 as a bottom gate dielectric and with 1000 nm parylene as a top gate dielectric. When V_{G2}, top gate bias was varied from 0 V to 100 V in steps of 10 V, the V_{th} was only shifted from 6.6 V to 1.3 V. In the case of low C_{top}/C_{bottom}, the large top gate voltage was needed to shift V_{th} value as shown in Fig. 3. From the DG OTFT with 300 nm thick parylene, as shown in Fig. 2 (a), the measured slope of dV_{th}/dV_{G2} was -0.16 and that from the DG OTFT with 1000 nm thick parylene was -0.05, which were in agreement with C_{top}/C_{bottom} of -0.17 and -0.052, respectively. In the case of DG OTFT with PEALD 200 nm Al_2O_3 deposited at 100 °C as a top gate dielectric, the measured dV_{th}/dV_{G2} was -0.6, which was also in agreement with C_{top}/C_{bottom} of -0.66.

The relationship between V_{G2} and V_{th} of DG OTFT with different combinations of bottom and top gate dielectrics was shown in Fig. 4. In silicon metal-oxide-semiconductor field effect transistors (MOSFETs), which are widely used as electronic devices, V_{th} can be controlled by changing the doping level of semiconductor. However, in case of OTFT, V_{th} control by doping is not possible yet. The DG OTFT used in this work is an alternative for artificially controlling V_{th} and on-current. Furthermore, the top gate dielectric layer plays an additional role of passivation for OTFT devices. As mentioned above, parylene is a commonly used passivation material and the PEALD Al_2O_3 deposited at a low temperature is a newly developed passivation layer by the authors. Fig.5 shows the transfer characteristics of DG OTFT with PEALD 150 nm Al_2O_3 deposited at 100 °C as a top gate dielectric after the shelf storage of 6 months at room temperature in air. The initial V_{th} of this device was about -3.9 V and that after the shelf storage it was slightly shifted to the positive to -3.5 V. Other electrical parameters such as mobility, off current, and subthreshold slope were almost identical, compared with the initial values. The relationship between V_{G2} and V_{th} was still clearly observed meaning the pentacene OTFT was not seriously degraded even after 6 months storage as shown in Fig. 5. We also checked the passivation performances of DG OTFT with parylene as a top gate dielectric after the storage of 6 months. Some degradation of pentacene active layer happened and that caused the decrease of mobility and on-current and the increase of subthreshold slope and off-current. It is believed that the passivation performance of PEALD Al_2O_3 is superior to that of parylene.

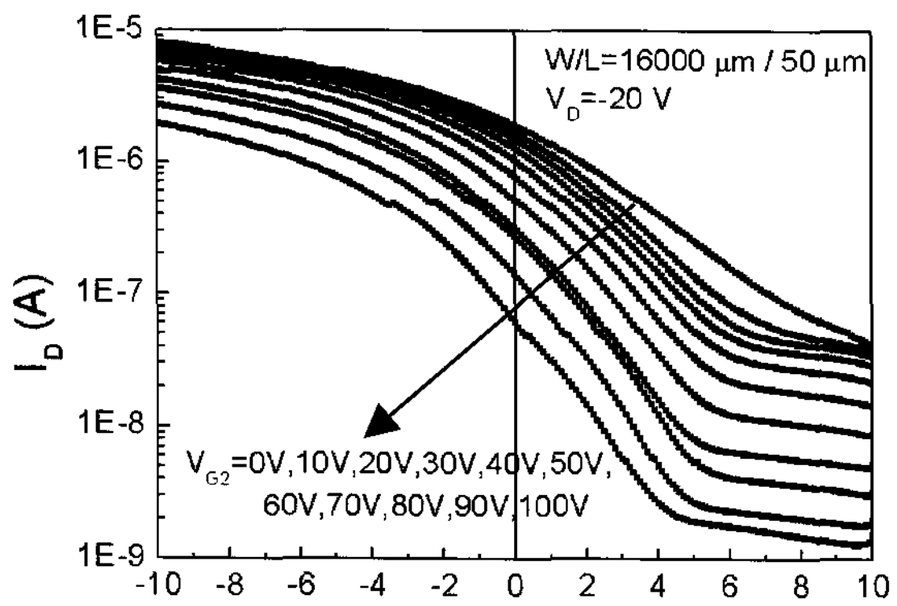

Fig. 3. The change of transfer characteristics of OTFT with PEALD 150 nm Al_2O_3 as a bottom gate dielectric and with 1000 nm parylene as a top gate dielectric when V_{G2} was varied from 0 V to 100 V in intervals of 10 V.

Although V_{th} of OTFT can be controlled by modifying the surface of gate dielectric layer with self-assemble monolayer (SAM) [12,13], such approaches are still far from practical use due to the reliability of manufacturing process and the instability in moisture on SAM coating. The present work shows that DG OTFT can be applied and in fact, be a useful method for the fabrication of practical OTFTs.

4. Conclusion

We reported on the fabrication of DG pentacene OTFT using parylene and PEALD Al_2O_3 as top gate dielectrics. The V_{th} shift of DG OTFT was elucidated by an analysis of the electrostatic potential. The control of electrical parameters of OTFT such as V_{th} and on-current and the

improvement of passivation performance could be simultaneously solved using a DG OTFT. The present work suggests that the PEALD Al_2O_3, which is possible of low temperature deposition onto plastic substrate, is a good candidate for both gate dielectric and passivation layer of DG OTFT.

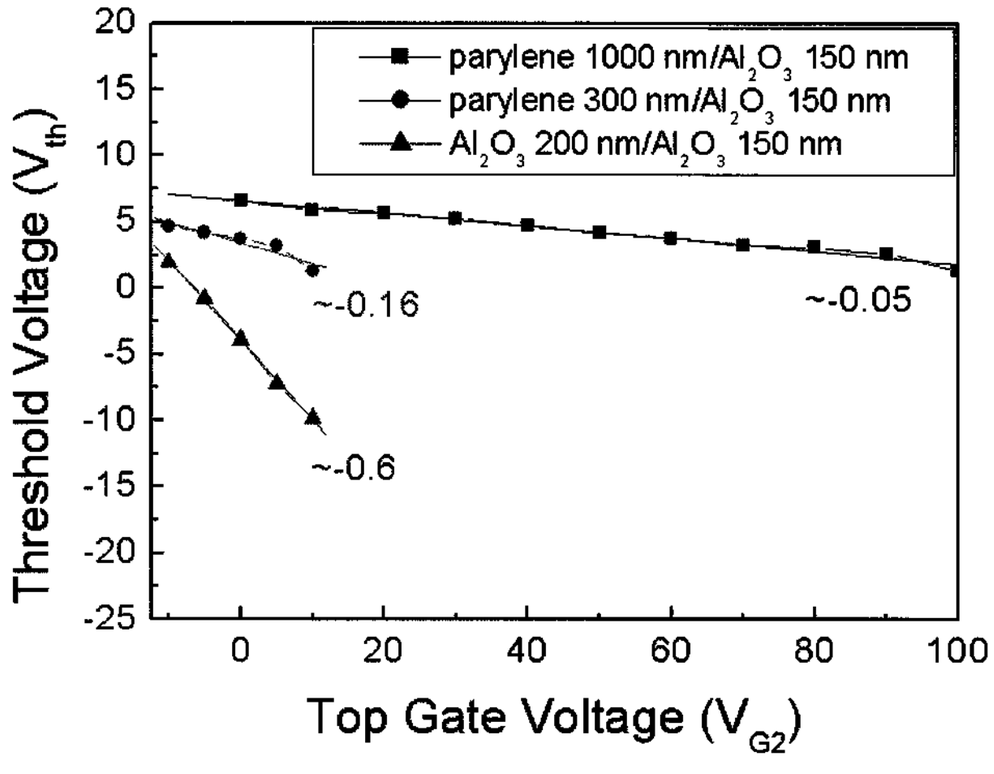

Fig. 4. The dependence of V_{th} on V_{G2} for DG OTFTs with different combinations of bottom and top gate dielectric.

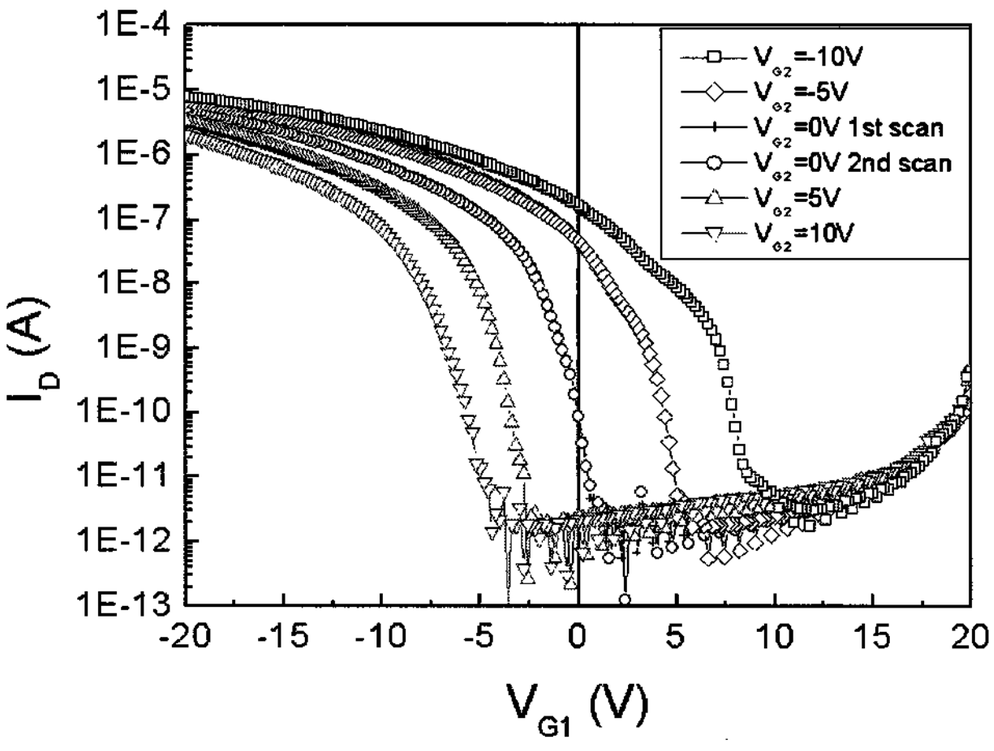

Fig. 5. The change of transfer characteristics of the DG OTFT with 150 nm thick PEALD Al_2O_3 as a bottom gate dielectric and with 200 nm thick PEALD Al_2O_3 as a top gate dielectric when V_{G2} was varied from -10 V to 10 V in steps of 5 V. The DG OTFT was measured after the shelf storage of 6 months at room temperature in air.

6. References

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