Optimized Phase Noise of LC VCO Using an Asymmetrical Inductance Tank

Jae-Ho Yoon · Bhanu Shrestha · Ah-Rah Koh · Gary P. Kennedy · Nam-Young Kim

Abstract

This paper describes fully integrated low phase noise MMIC voltage controlled oscillators(VCOs). The Asymmetrical Inductance Tank VCO(AIT-VCO), which optimize the shortcoming of the previous tank's inductance optimization approach, has lower phase noise performance due to achieving higher equivalent parallel resistance and Q value of the tank. This VCO features an output power signal in the range of −11.53 dBm and a tuning range of 261 MHz or 15.2 % of its operating frequency. This VCO exhibits a phase noise of −117.3 dBc/Hz at a frequency offset of 100 kHz from carrier. A phase noise reduction of 15 dB was achieved relative to only one spiral inductor. The AIT-VCO achieved low very low figure of merit of −184.6 dBc/Hz. The die area, including buffers and bond pads, is 0.9×0.9 mm^2.

Key words : Symmetrical and Asymmetrical Inductance Tank Structures, Monolithic Microwave Integrated Circuit (MMIC), Heterodyne Bipolar Transistor(HBT), Differential LC VCO, Phase Noise, Cross Coupled Configuratio.

Ⅰ. Introduction

Integrated VCOs are important blocks in any communication or test and measurement system. They are used in virtually all up-conversion, down-conversion, frequency modulation and high frequency generation systems. While most VCOs are designed to generate a sinusoidal voltage waveform, their uses and required performance varies widely.

A desired characteristic of VCOs is low phase noise. Generally, efforts to improve the phase noise performance of integrated LC VCOs have resulted in a differential topology. An advantage of this architecture is its high loop gain making it popular for differential VCO designs in MMIC and RFICs. Furthermore, an integrated circuit reduces the size of devices such as on-chip inductors and capacitors thereby improving the spectral purity of VCOs[1],[2]. Also, the varactor diode which is used for frequency tuning is realized on the same chip. A further advantage is that 1/f noise is reduced by using differential topology with capacitive coupling feedback because balanced differential design helps to minimize jitter due to power supply coupling, which is a major source of jitter in high-frequency oscillators[3],[4]. On the other hand, hybrid VCO circuits are usually used in the more traditional Colpitts design which avoids the added complexity of the differential VCO configuration. Only limited differential VCO design and modeling information has been made available here because of its primary usage in proprietary MMICs and RFICs. Therefore this design methodology forms the basis of the fully differential LC VCOs for L-band applications.

In this paper, a comparative analysis of differential LC VCOs with asymmetrical and symmetrical inductance tank structures is presented. In section II, a description of the design methodology of the VCO is presented. Section III presents measured data from the VCOs.

Ⅱ. InGaP/GaAs HBT Technology

The technology used in this work is an InGaP/GaAs HBT technology based on a high linearity(HL) process from Knowledge* on Semiconductor Inc. The VCO core devices reported in this letter have two emitter fingers of width 2-μm, and an emitter length of 20-μm(2×2×20 μm^2). The epitaxial layer structure features a metal organic chemical vapor deposition(MOCVD) grown C-doped base, an InGaAs emitter contact layer, mesa etch stops, and a base ledge layer. Two metal layers are provided for interconnection. The backside process features 50-μm-diameter standard through via holes, gold plating, and a street etch.

The measured HBT DC current gain is approximately 112 at a current density of Jc=25 kA/cm^2. Breakdown

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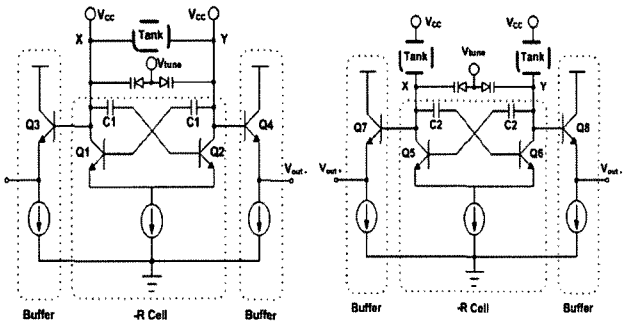
voltages BV_{CEO} and BV_{CBO} are 12 V and 23 V, respectively; these are suitable for most IC applications. The 2×20 μm^2 single emitter HBTs produced a peak f_T and f_{max} of 48 GHz and 80 GHz, respectively, at a current density of Jc=50 kA/cm^2 and a collector emitter voltage (V_{CE}) of 1.5 V.

The next section describes the design methodology that was used in order to ensure the VCOs have low phase noise behavior; asymmetrical and symmetrical tank structures were compared.

Ⅲ. Circuit Design Considerations

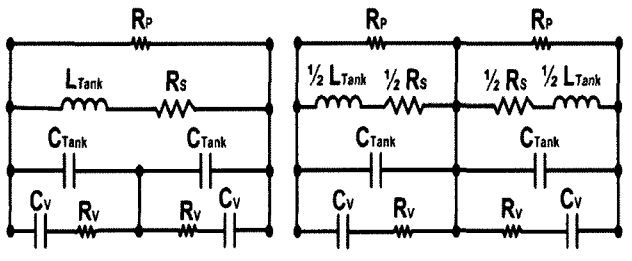
The VCOs implemented in this work consist of an Asymmetrical or a Symmetrical LC tank, a pair of emitter follower buffers and a negative resistance. The core circuits of the VCOs are shown in Fig. 1. To reduce the $1/f$ noise, a cross-coupled differential topology with capacitive coupling feedback is used to realize the VCO. The cross-coupled transistors($Q1$ and $Q2$, $Q5$ and $Q6$) form a positive feedback loop providing a negative resistance which cancels the loss in the LC-resonator[4]. This loop increases the loop gain through the capacitors and thereby acts to suppress the up and down-conversion noise as well as to block the dc bias cross-coupling the transistors.

The VCO core is isolated from the load impedance(50 Ω) by means of two buffer circuits($Q3$ and $Q4$, $Q7$ and Q8). The source of the current mirror provides constant current to the differential VCO core as well as the output buffer circuits thereby improving the VCO pulling figure. Also, low current consumption in the core circuit is maintained by optimizing the fingers of the core transistors. Thus, it is possible to get the required VCO pulling figure and output swing with this transistor arrangement. Furthermore, to obtain low phase noise performance, the high Q resonator is optimized; this is one of the most important aspects of oscillator design.



(a) AIT-VCO (b) SIT-VCO

Fig. 1. Differential LC VCOs circuit schematics.



(a) AIT-VCO (b) SIT-VCO

Fig. 2. Simple equivalent circuits of the LC tank.

The AIT-VCO design concern was related to the optimization of the quality factor of the tank using only one asymmetrical spiral inductor. To acquire a high Q tank, large parallel resistance of tank(R_P) has to be achieved because Q value of the tank decides phase noise performance in the oscillator. From Leeson's equation[5], we have

$$\left|\frac{Y}{X}(j\omega)\right|^2 = \frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{1}$$

Equation (1) forms the noise shaping function for the oscillator. This expression reveals the dependence of the output noise upon the Q factor of the tank, the center frequency, and the offset frequency. As the Q factor of the tank increases, the performance improves in two ways: (a) the noise shaping function, equation (1), becomes sharper; (b) the noise injected by active devices decreases[6],[7]. The asymmetrical inductance tank structure used large tank parallel resistance(R_P) when comparing the symmetrical inductance tank structure shown in Fig. 2. If the asymmetrical inductor is used in tank, the parallel resistance of the tank(R_P) will be two times better than the symmetrical tank as shown in Fig. 2. The equivalent parallel resistance of the tank can be expressed as

$$R_P = \frac{(L_{eq}\omega_{res})^2}{R_S} \tag{2}$$

where R_S models the loss of the inductor as a series resistance. In typical inductor, L_{eq} is proportional to the R_s; that is, if L_{eq} increases by a factor m, then so does R_P. Since the impedance of the tank at resonance is equal to R_P, the voltage swing for a given bias current also increases by the same factor[6]. Since the Q factor of the inductor is constant(the inductor is the only source of loss in the tank), then the Q of the tank will also be constant. Therefore, the parallel resistance of the resonator can be written as

$$R_P = Q_{ind}\omega_{res}L \tag{3}$$

For low values of inductor, R_P will be small[7]. It can assume that the oscillation amplitude is proportional to

$$V_{\tan k} \propto R_P \tag{4}$$

And then, the power in the tank is given by

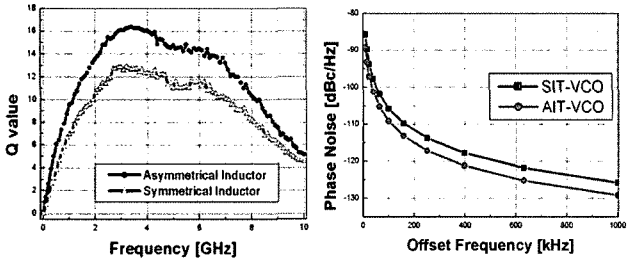
$$P_S \propto \frac{V^2_{\tan k}}{R_P} = \frac{(R_P)^2}{R_P} = R_P \tag{5}$$

The criterion for achieving low phase noise is given by Leeson's[5] formula for phase noise, as follows:

$$L(\Delta\omega) = 10 \cdot \log\left[\frac{2FkT}{P_{sig}}\left\{\left(1+\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{6}$$

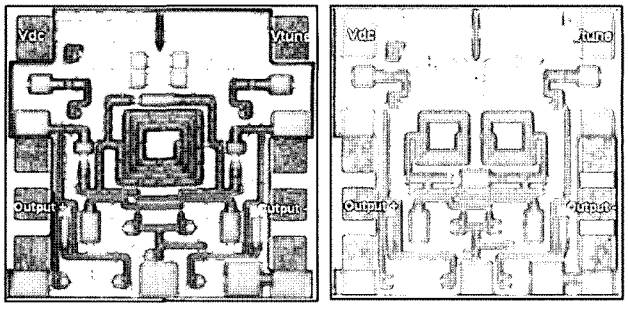
where F represents the noise figure of the transistor, k is Boltzmann's constant, T is the temperature, P_{sig} is the signal power, ω_0 is the oscillation frequency, $\Delta\omega$ is the offset from the oscillation frequency, Q is the loaded Q value of the tank, and $\Delta\omega_{1/f^3}$ is the corner frequency of $1/f$ noise. This equation is phenomenological and is useful for understanding how phase noise can be minimized[8]. Generally, the Q value of the tank and the oscillation amplitude in the tank should be maximized, and the noise generated by the transistor should be as small as possible. In addition, the tank energy should be maximized, leading to a minimization of the tank inductance. All these criteria were taken into account when designing the VCOs. As a result, the asymmetrical inductance tank structure with only one spiral inductor can be optimized with high R_P, voltage swing, and Q factor. If conventional symmetrical inductors are used in tank, the Q value of the tank decrease because of low parallel resistance of tank(R_P).

Fig. 3 shows a comparison of the Q value and phase noise simulation as a function of offset frequency for the asymmetrical and symmetrical inductance tank structures. The most important point to note here is that the phase noise of the AIT-VCO is greater than 3.5 dB at 100 kHz offset. The reason for this is the higher Q factor of the asymmetrical tank circuit. Thus, an asymmetrical inductance tank combined with a VCO can be optimized to produce better phase noise performance than that of symmetrical inductance tank combined with a VCO[9]. Microphotographs of the fabricated differential



(a) Q value of the inductors (b) phase noise

Fig. 3. Simulation results.



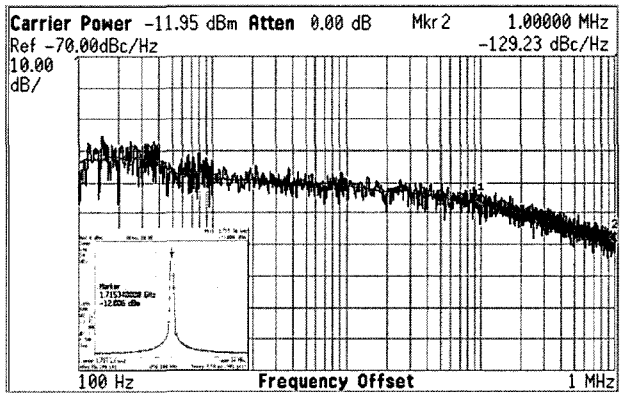
(a) AIT-VCO(0.9×0.9 mm^2) (b) SIT-VCO(0.9×0.9 mm^2)

Fig. 4. Microphotographs of the differential LC VCOs.

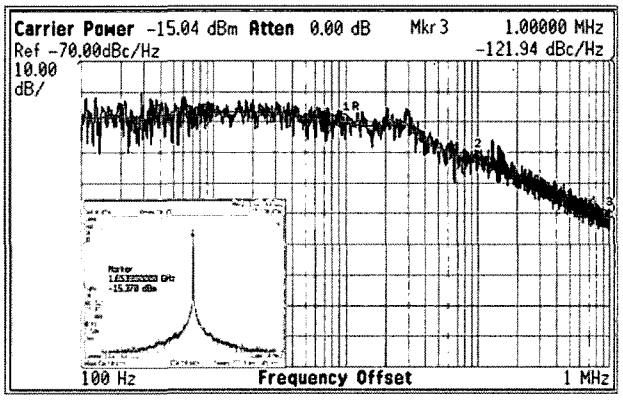
LC VCOs are shown in Fig. 4 and both chip areas are 0.9×0.9 mm^2.

Ⅳ. Measurement Results

Free running oscillation frequencies of 1.715 GHz with an output power of −11.53 dBm and 1.664 GHz with an output power of −15 dBm were obtained from the AIT-VCO and the SIT-VCO, respectively, with a 5 V supply voltage.



(a) AIT-VCO



(b) SIT-VCO

Fig. 5. Output spectrum and phase noise of the VCOs.

The measured output spectrum and phase noise of the VCOs shown in Fig. 5 is −117.3 dBc/Hz(AIT-VCO) and −102.4 dBc/Hz(SIT-VCO) at 100 kHz offset and −129.3 dBc/Hz(AIT-VCO) and −121.9 dBc/Hz(SIT-VCO) at an offset frequency of 1 MHz, respectively. Using an asymmetrical inductor produces low phase noise as a result of optimization of the parallel resistance of tank(R_P), and Q factor of the inductance tank. In order to compare the VCO performance with other VCOs in terms of different frequencies and power dissipations, a widely used figure-of-merit(FOM) is defined[7] as

$$FOM = L(\Delta f_m) - 20\log\left(\frac{f_0}{f_m}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \quad (7)$$

where L is the measured phase noise, f_0 is the oscillation frequency, f_m is the frequency offset, and P_{diss} is the dissipation power of the VCO. In this work we achieve a FOM of −184.6 dBc/Hz(AIT-VCO) which is quite comparable to the previously published results.

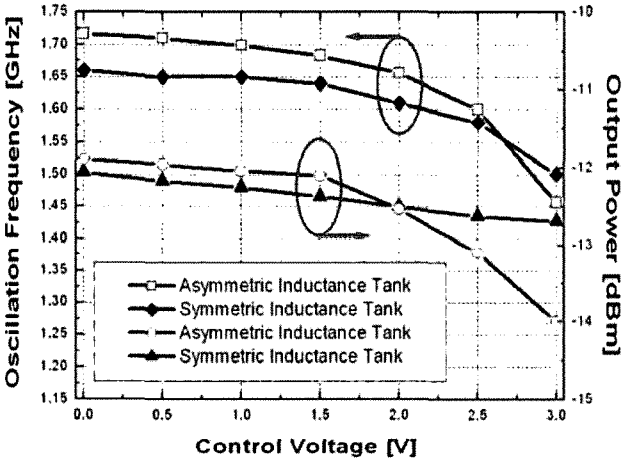


Fig. 6. Variation of oscillation frequency and output power as a function of control voltage sweep.

Table 1. Summary of the measurement results from the LC VCOs.

Items	Unit	Measurement Results	
		AIT-VCO	SIT-VCO
Oscillation Frequency	GHz	1.715	1.664
Output Power	dBm	−11.53	−15
Tuning Range (0~3 V)	MHz	261	160
Supply Voltage	V	5	5
Current Consumption	mA	11	13
PhaseNoise @100 kHz	dBc/Hz	−117.3	−102.4
Figure of Merit		−184.6	−169.8
Chip size	mm^2	0.9×0.9	0.9×0.9

Table 2. A summary of the VCO performance from published literature.

Ref.	Type	Freq. [GHz]	Tuning Range [MHz]	PhaseNoise [dBc/Hz] @100 kHz	Figure of Merit
[3]	0.5 um bipolar	1.9	100	−103	−172.5
[4]	CMOS	2.6	-	−99	−177.7
[10]	SiGe HBT	2.02	470	−86	−157.3
[11]	SiGe HBT	2.5	120	−107	−168.7
[12]	SiGe HBT	1.476	150	−100	−166.8
[13]	CMOS	1.9	160	−98	−171.8
AIT-VCO	InGaP -HBT	1.715	261	−117.3	−184.6

The oscillation frequency and output power variation as a function of control voltage sweep are depicted in Fig. 6. The oscillation frequency is varied from 1.454 GHz to 1.715 GHz in the asymmetrical VCO and from 1.504 GHz to 1.664 GHz in the symmetrical VCO, respectively. Table 1 summarizes the measurement results of the designed LC VCOs and Table 2 presents a comparison of VCO performance from recent literature with this work.

V. Conclusions

InGaP/GaAs HBT-based VCOs based on a cross-coupled topology with different tank structures including an optimized inductance tank are simulated, fabricated, and characterized. This paper has presented the phase noise optimization method using asymmetric inductance tank structure and compared with the two types of oscillators using asymmetrical and symmetrical tanks. Low phase noise performance was obtained by using inductance optimization with a high quality factor and parallel resistance of the tank(R_P) in the LC tank. The measurement result shows that the minimum phase noise performance with an optimal asymmetric inductance tank structure is −117.3 dBc/Hz at 100 kHz offset which shows the best performance, as compared with the previous HBT VCOs; this is improving the phase noise of the 15 dBc better than symmetrical inductance tank structure. Furthermore, it has a wider frequency tuning range than the symmetric tank structure.

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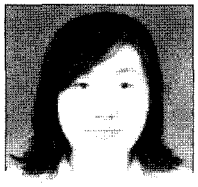

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