An MMIC Broadband Image Rejection Downconverter Using an InGaP/GaAs HBT Process for X-band Application

Jeiyoung Lee · Young-Ho Lee · Gary P. Kennedy · Nam-Young Kim

Abstract

In this paper, we demonstrate a fully integrated X-band image rejection downconverter, which was developed using InGaP/GaAs HBT MMIC technology, consists of two single-balanced mixers, a differential buffer amplifier, a differential VCO, an LO quadratue generator, a three-stage polyphase filter, and a differential intermediate frequency(IF) amplifier. The X-band image rejection downconverter yields an image rejection ratio of over 25 dB, a conversion gain of over 2.5 dB, and an output-referred 1-dB compression power($P_{1dB,OUT}$) of − 10 dBm. This downconverter achieves broadband image rejection characteristics over a frequency range of 1.1 GHz with a current consumption of 60 mA from a 3-V supply.

Key words : X-band Image Rejection Downconverter, Single-Balanced Mixer, Voltage Controlled Oscillator, LO Quadrature Generator, Polyphase Filter.

I . Introduction

The downconverter in a heterodyne receiver translates signals from the RF frequency range to the down-converted intermediate frequency. However, the input signal consists of not only the wanted RF signal but also the unwanted image signal, which is symmetrically located around the LO frequency. Hence, both signals share the same IF frequency; both the image and RF bands are downconverted to the same intermediate frequency(IF). The unwanted image signal may have some serious problems. Therefore, the image power is restricted by the image rejection ratio according to its system specification [1],[2].

An image rejection filter is commonly used in the signal path ahead of the mixer in order to eliminate the possibility of interference from the image band[3]. The image rejection filter is designed to have a relatively small loss in the RF band and a large attenuation in the image band. Thus, the image rejection filter has good image rejection performance. However, in a highly integrated receiver module, the image rejection filter causes insertion loss of the RF signal path, increased cost, and packaging complexity.

Another way to remove the unwanted image signal utilizes image rejection architecture, such as Hartley or Weaver architecture, which is used for high-level circuit integration[4],[5]. Accurate and symmetrical design is very important in order to minimize the amplitude and phase error, thereby providing better image rejection characteristics. In this paper, an X-band MMIC image rejection downconverter is proposed for broadband image rejection characteristics. The designed fully differential image rejection downconverter consists of two single-balanced mixers, a differential buffer amplifier, a differential VCO, an LO quadrature generator, a three-stage IF poly phase filter, and a differential IF amplifier as shown in Fig. 1.

II . Image Rejection Architecture

A block diagram of the image rejection architecture is illustrated in Fig. 2. The configuration contains two mixers, a differential VCO, a 90 phase shifter, a low pass filter and an adder. This Hartley architecture is employed for its low power characteristics, since it uses half mixers, by comparison with the weaver architecture[1].

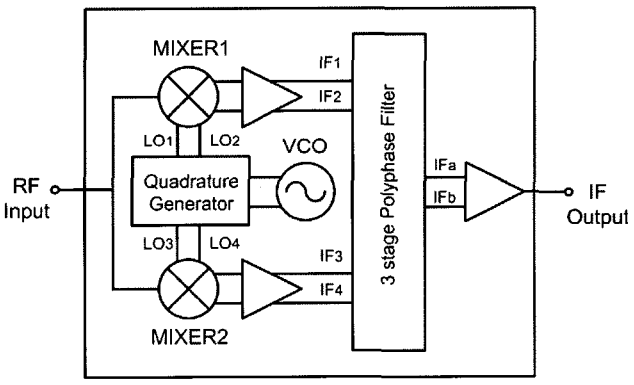

Fig. 1. Block diagram of the image rejection downconverter.

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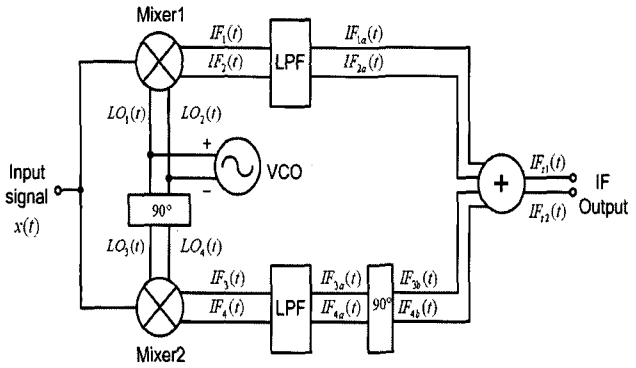

Fig. 2. Designed double balanced mixer.

Without the image rejection filter, the input signal includes both the RF signal and the image signal. Therefore, $A_{RF}\cos\omega_{RF}t$ and $A_{IM}\cos\omega_{IM}t$ represent the RF signal and the image signal, respectively. Then, the input signal $x(t)$ becomes

$$x(t)=A_{RF}\cos\omega_{RF}t+A_{IM}\cos\omega_{IM}t \quad (1)$$

Quadrature LO signals are generated by a differential VCO and a 90 phase shifter. In the case of low-side LO injection, the input signal($x(t)$) is multiplied by quadrature LO signals($LO_1(t)$ to $LO_4(t)$) producing IF signals($IF_{1a}(t)$ to $IF_{4a}(t)$) after low pass filtering.

$$IF_{1a}(t)=\frac{A_{RF}}{2}\cos(\omega_{RF}-\omega_{LO})t+\frac{A_{IM}}{2}\cos(\omega_{LO}-\omega_{IM})t \quad (2)$$

$$IF_{2a}(t)=-\frac{A_{RF}}{2}\cos(\omega_{RF}-\omega_{LO})t-\frac{A_{IM}}{2}\cos(\omega_{LO}-\omega_{IM})t \quad (3)$$

$$IF_{3a}(t)=\frac{A_{RF}}{2}\sin(\omega_{RF}-\omega_{LO})t-\frac{A_{IF}}{2}\sin(\omega_{LO}-\omega_{IM})t \quad (4)$$

$$IF_{4a}(t)=-\frac{A_{RF}}{2}\sin(\omega_{RF}-\omega_{LO})t+\frac{A_{IM}}{2}\sin(\omega_{LO}-\omega_{IM})t \quad (5)$$

Then, $IF_{3a}(t)$ and $IF_{4a}(t)$ are phase-shifted by 90, resulting in $IF_{3b}(t)$ and $IF_{4b}(t)$.

$$IF_{3b}(t)=\frac{A_{RF}}{2}\cos(\omega_{RF}-\omega_{LO})t-\frac{A_{IF}}{2}\cos(\omega_{LO}-\omega_{IM})t \quad (6)$$

$$IF_{4b}(t)=-\frac{A_{RF}}{2}\cos(\omega_{RF}-\omega_{LO})t+\frac{A_{IM}}{2}\cos(\omega_{LO}-\omega_{IM})t \quad (7)$$

Finally, the IF signals are combined, which results in the cancellation of the image signals, producing:

$$IF_{t1}(t)=A_{RF}\cos(\omega_{RF}-\omega_{LO})t \quad (8)$$

$$IF_{t2}(t)=-A_{RF}\cos(\omega_{RF}-\omega_{LO})t \quad (9)$$

III. Circuit Design

The X-band image rejection downconverter consists of two single-balanced mixers, a differential VCO, an LO quadrature generator, a three-stage polyphase filter and a differential IF amplifier. The RF input signal between 10.5 and 11.6 GHz is down-converted to an L-band IF frequency between 0.9 to 2 GHz with a 9.6 GHz local oscillator signal from the integrated differential VCO. Also, the unwanted image signal between 7.6 and 8.7 GHz is suppressed by this image rejection downconverter.

A single-balanced mixer is designed in the downconverter, which has the advantage of low power dissipation. This is because only half the number of transistors are required in the mixer core by comparison with those of the double-balanced Gilbert-cell mixer. In the single-balanced mixer, the port isolations of LO-IF and RF-IF show worse characteristics than those produced by the double-balanced Gilbert-cell mixer. However, the frequency separation between the IF frequency and the LO frequency(RF frequency) is sufficient enough to be filtered out by the low pass filter. A strict symmetry is maintained in the layout of the balanced structure for the RF and LO input ports in order to minimize the amplitude and phase error at each port. The mixer simulation shows a conversion gain of 4.4 to 6.5 dB at a bias of 3 V and current consumption of 12 mA[6].

The Quadrature signal generator and the three-stage IF polyphase filter use an RC poly phase network, which provides wideband characteristics in terms of phase and amplitude. The quadrature generator is designed using a single-stage polyphase filter as shown in Fig. 4. When the differential LO signals drive the input, the circuit generates four quadrature signals at its outputs. The resistor and capacitor values are determined from $\omega=1/RC$.

The polyphase filter is designed as shown in Fig. 5. The IF frequency band is between 0.9 and 2 GHz, however, the effective bandwidth is narrow to cover the whole IF band with just a single-stage polyphase filter. Thus, the three-stage polyphase filter is used to produce sufficient broad-

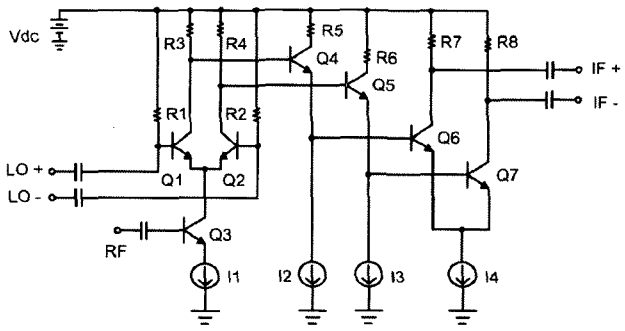

Fig. 3. Circuit schematic of the single-balanced mixer core.

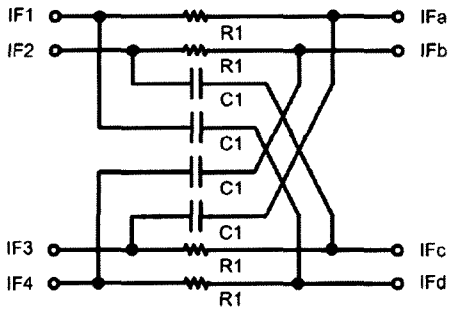

Fig. 4. Circuit schematic of the quadrature generator.

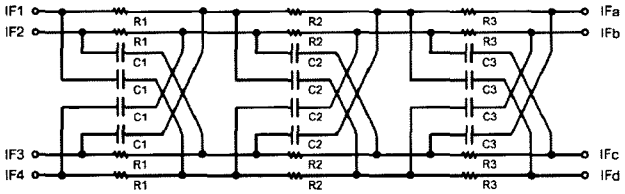

Fig. 5. Circuit schematic of the 3-stage poly phase filter.

band characteristics for this image rejection downconver ter design. In each stage, the resistor and capacitor values are determined by 1, 2, and 3 with resonance frequencies of 1.1, 1.5, and 1.9 GHz. A simulation of the polyphase filter design predicts an insertion loss of 9 dB in the desired RF signal input, and an attenuation of over 50 dB in the undesired image signal input.

The VCO comprises a VCO core, a voltage controlled resonator, an output buffer, and an LC resonator. Cross-coupled feedback is used for negative trans-conductance topology($-Gm$) as shown in Fig. 6 and the varactor diodes are used for voltage tuning. When a reverse bias is applied to them, the resonance frequency can be varied. Thus, they provide oscillation frequency tuning capability. The output buffer employs the common collector configuration. This is used to compensate the output swing and to transform the output impedance. The VCO simulation(for the case of

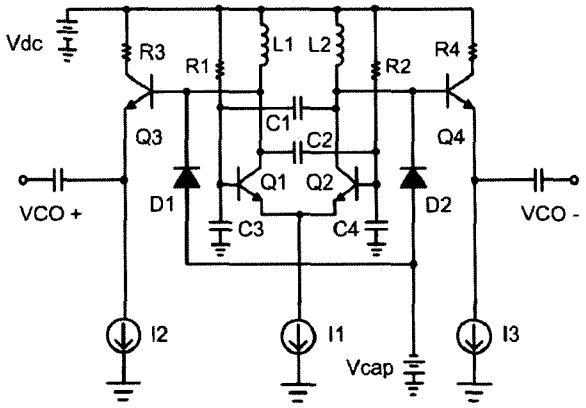

Fig. 6. Circuit schematic of the differential VCO.

a single-ended output) resulted in an output power between -5 and -3 dBm, an oscillation frequency between 9.8 and 10.2 GHz. Also, phase noises of -80 dBc/Hz and -100 dBc/Hz were also predicted at 100 kHz and 1 MHz offset, respectively.

Ⅳ. Fabrication and Measurement

As shown in Fig. 7, the image rejection downconverter IC was fabricated in a commercially available InGaP/GaAs HBT MMIC technology. The chip was measured using RF on-wafer probes. The conversion gain and image rejection ratio were measured to be 2.5 to 7 dB and over 25 dB, respectively(Fig. 8 and Fig. 9). Also, the $P1dB,OUT$ was -10 dBm in the IF frequency range 0.9 to 2 GHz with a 9.6 GHz LO frequency. Furthermore, with a two tone RF input of -35 dBm and a 4-MHz frequency spacing, the IF output power was found to be -31 dBm with a third-order intermodulation distortion($IMD3$) product of over 44 dBc. Therefore, a third-order output intercept point($OIP3$) of -9 dBm and a third-order input intercept point($IIP3$) of -13 dBm were produced.

Table 1 compares the results with previous work. The

Table 1. Summary of previously published image rejection downconverter MMICs.

Works	RF(GHz)	IF(Hz)	Conversion Gain(dB)	IRR(dB)	Supply voltage(V)	Current Diss.(mA)	Process
[3]	11.7~12.3	1 G~1.6 G	46	30	5	43	GaAs MESFET
[4]	17.3~18.35	11.7 G~12.75 G	3	23	-	-	GaAs MESFET
[7]	5.1~5.8	75 M	14	36	0.9	21.6	SiGe HBT
[8]	5.1~5.8	75 M	17	45	2.2	22.7	Si BJT
[9]	1.9	10 M	16	34	3.3	7.1	CMOS
[10]	2	4 M	4	40.8	3.3	27.7	CMOS
[5]	2.45	2 M	46	45	3	10.4	CMOS
This work	**10.5~11.6**	**0.9 G~2 G**	**2.5**	**25**	**3**	**60**	**InGaP HBT**

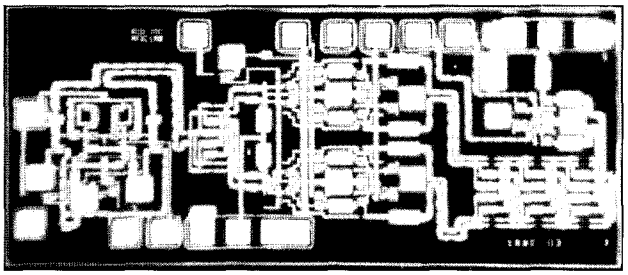

Fig. 7. Photographic image of the image rejection downconverter chip(The chip area is 2.6×1.1 mm^2).

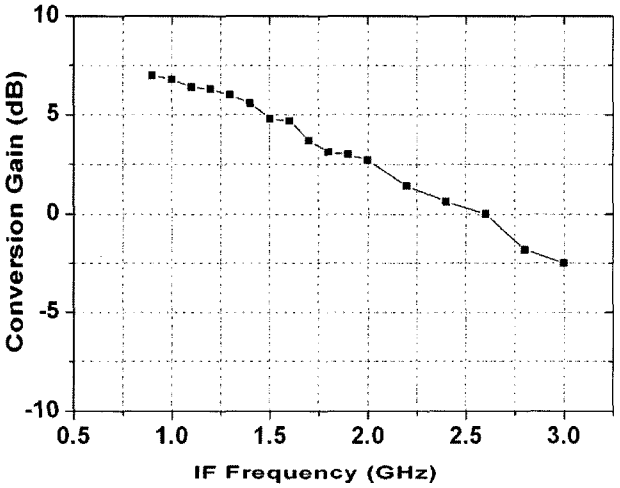

Fig. 8. Measured conversion gain of downconverter.

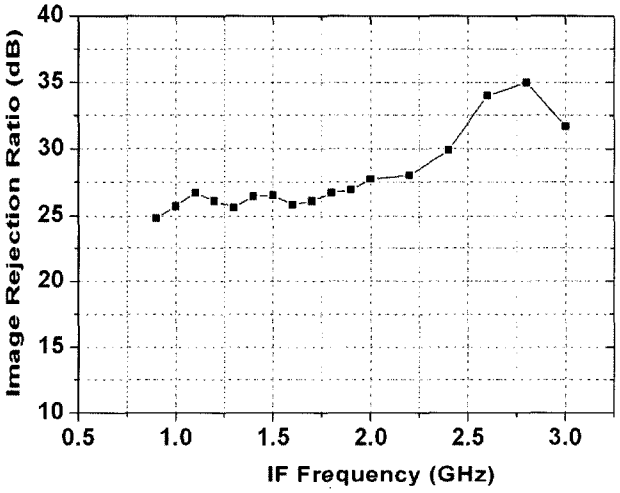

Fig. 9. Measured image rejection ratio of downconverter.

chip in reference[4] used passive-type balanced mixers, a 90 phase splitter, and a power combiner, based on the Hartly architecture in a single-ended configuration. From the work of J.R. Long[7] and J.P. Maligeorgos et al.[8], low voltage image rejection downconverter ICs used an IF frequency of 5 GHz. Also, their ICs were fabricated using SiGe HBT and Si-BJT processes. However, additional off-chip elements, such as 180 and 90 hybrid couplers are required to configure a Hartly architecture. The image rejection downconverter ICs used by Azevedo et al.[9], Song et al.[10], and Khannur et al.[5] were developed for bluetooth applications using the Weaver architecture in CMOS technology. In this case, the oscillators are not included in the ICs, thus, they need an additional LO signal from outside of the chip. In spite of high current consumption, it shows lower conversion gain than others. Due to mismatching of gain and phase at quardrature generator, the performance of conversion gain and image rejection ratio are degenerated. Table 2 shows a comparison with simulation and measurement data.

Table 2. Comparison with simulation and measurement data.

Parameter		Units	Simulation	Measurement
Input Freq.		GHz	10.5~11.6	10.5~11.6
Image Freq.		GHz	7.6~8.7	7.6~8.7
Output Freq.		GHz	0.9~2	0.9~2
Conversion Gain		dB	6~10	2.5~7
Image Rejection Ratio		dBc	36~50	25~27.5
$P_{1dB,IN}$		dBm	-14	-13
$P_{1dB,OUT}$		dBm	-6.5	-10
IIP3		dBm	-6.5	-10.5
OIP3		dBm	1	-6.5
Oscillation Freq.		GHz	9.8~10.2	9.6~9.8
VCO Output Power		dBm	-5	-5
Phase Noise	@100 kHz	dBc/Hz	-80	-54
	@1 MHz		-100	-110
Total Current Consumption		mA	60	60
Supply Voltage		V	3	3

The X-band image rejection downconverter comprises two mixers, a differential buffer amplifier, a VCO, an LO quadrature generator, a polyphase filter, and an IF amplifier. The supply voltage is 3 V with a total current consumption of 60 mA; 12 mA for the single-balanced mixers, 8 mA for the differential buffer amplifiers, 10 mA for the IF amplifier, and 10 mA for the differential VCO. This IC achieves broadband image rejection characteristics over a frequency range of 1.1 GHz by comparison with previously reported downconverters.

V. Conclusion

We developed a fully differential X-band MMIC image rejection downconverter using an InGaP/GaAs HBT pro-

cess with a total chip area of 2.6×1.1 mm^2. The downconverter gives broadband image rejection characteristics over a frequency range of 1.1 GHz from a 3-V supply. Hence, no additional image rejection filter is necessary when using this downconverter in a X-band heterodyne receiver application.

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References

[1] B. Razavi, *RF Microelectronics*, Prentice Hall, 1998.

[2] Jeiyoung Lee, Hyunchol Shin, C. H. Park, and N. Y. Kim, "A low-power Ku-band downconverter in InGaP-GaAs HBT technology", *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 4, pp. 193-195, Apr. 2005.

[3] T. Yoshimasu, T. Tomita, "A low current GaAs monolithic image rejection downconverter for X-band broadcast satellite applications", *IEEE Trans. Microwave Theory & Tech.*, vol. 40, no. 12, pp. 2433-2438, Dec. 1999.

[4] A. H. Baree, I. D. Robertson, "MMIC SSB frequency translators with image-rejection for satellite trans-ponder applications", *IEEE MTT-S Microwave Symp. Dig.*, vol. 2, pp. 869-872, May 1995.

[5] P. B. Khannur, Soo Ling Koh, "A 2.45 GHz fully-differential CMOS image-reject mixer for Bluetooth application", *IEEE MTT-S Microwave Symp. Dig.*, vol. 1, pp. 549-552, Jun. 2002.

[6] Shang-Shin Choi, Eun Namking, S. H. Lee, J. Y. Lee, S. J. Kim, J. C. Lee, B. J. Lee, J. H. Kim, S. H. Jeon, and N. Y. Kim, "InGaP/GaAs HBT MMIC SBM with low pass filter type output matching circuit for LNB application", *Asia Pacific Microwave Conference 2004 Abstracts*, p. 556, Dec. 2004.

[7] J. R. Long, "A low-voltage 5.1~5.8-GHz image-reject downconverter RF IC", *IEEE Trans. Solid-State Circuits*, vol. 35, no. 9, pp. 1320-1328, Sep. 2000.

[8] J. P. Maligeorgos, J. R. Long, "A low-voltage 5.1~5.8-GHz image-reject receiver with wide dynamic range", *IEEE Trans. Solid-State Circuits*, vol. 35, no. 12, pp. 1917-1926, Dec. 2000.

[9] F. Azevedo, J. C. Freire, "CMOS monolithic wideband image rejection mixer with polyphase filters", *SBMO/IEEE MTT-S int. Microwave and Optoelectronics Conference*, vol. 2, pp. 815-818, Sep. 2003.

[10] Eunseok Song, Wonchan Kim, "A 2 GHz CMOS double conversion downconverter with robust image rejection performance against the process and temperature variations", *VLSI Circuits Symp. Dig.*, pp. 38-41, Jun. 2000.

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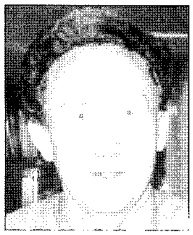

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