JPE 6-1-10

A New High Efficiency and Low Profile On-Board DC/DC Converter for Digital Car Audio Amplifiers

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ABSTRACT

A new high efficiency and low profile on-board DC/DC converter for digital car audio amplifiers is proposed. The proposed converter shows low conduction loss due to the low voltage stress of the secondary diodes, a lack of DC magnetizing current for the transformer, and a lack of stored energy in the transformer. Moreover, since the primary MOSFETs are turned-on under zero-voltage-switching (ZVS) conditions and the secondary diodes are turned-off under zero-current-switching (ZCS) conditions, the proposed converter has minimized switching losses. In addition, the input filter can be minimized due to a continuous input current, and an output inductor is absent in the proposed converter. Therefore, the proposed converter has the desired features, high efficiency and low profile, for a viable power supply for digital car audio amplifiers. A 60W industrial sample of the proposed converter has been implemented for digital car audio amplifiers with a measured efficiency of 88.3% at nominal input voltage.

Keywords: digital car audio amplifier, DC/DC converter, zero-voltage-switching, zero-current-switching

1. Introduction

Generally, analog audio amplifiers have excellent distortion characteristics, but show considerably low efficiency and require bulky heat sinks for cooling. On the other hand, digital audio amplifiers have high efficiency and a compact size, but relatively poor fidelity. Nowadays, since new technologies for digital audio amplifiers have been developed and their fidelity characteristics have been improved, as reported in [1-3], they are being applied to compact car audio systems. Therefore, a high efficiency and low profile on-board DC/DC converter is required for digital car audio amplifiers. Among previously proposed DC/DC converters, the boost integrated half bridge (BHB) converter shown in Fig. 1 is suitable for low voltage battery input applications, because the converter has a continuous input current, I_{LIN}, and a boosted link voltage, V_L. In addition, the primary MOSFETs are turned-on under zero-voltage-switching (ZVS) conditions[4-5]. However, the main disadvantages of the BHB converter are the high DC magnetizing current of the transformer, high voltage stress and large turn-off voltage oscillation of the secondary rectifier diodes, increased magnetic components count, and considerable freewheeling energy in the transformer.

In this paper, to overcome these disadvantages of the BHB converter, a new high efficiency and low profile

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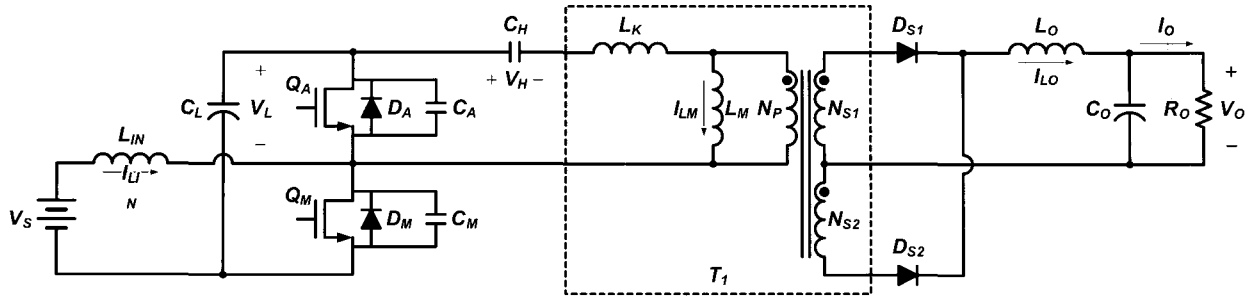


Fig. 1 Conventional BHB converter

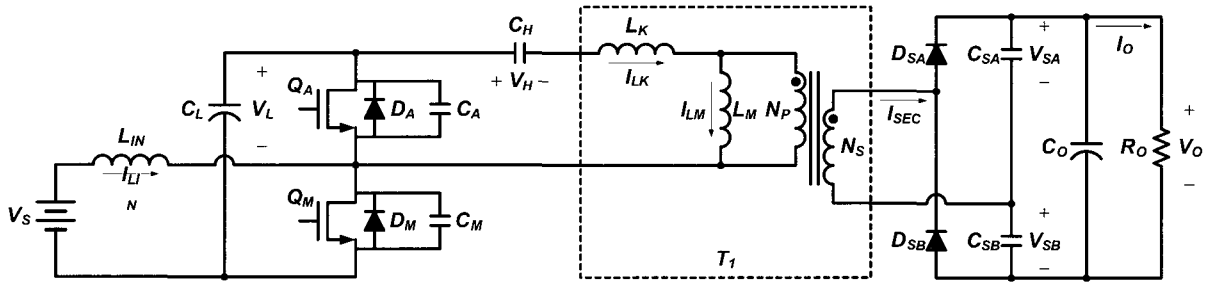


Fig. 2 Circuit diagram of the proposed converter

on-board DC/DC converter is proposed. The operational principles of the proposed converter are analyzed and the advantages are described. A 60W industrial sample for digital car audio amplifier has been implemented to verify the operational principles and the advantages of the proposed converter.

2. Principles of Operation

As shown in Fig. 2, the proposed converter is an asymmetrically controlled half bridge converter integrated with a boost converter in the output stage and a voltage doubling rectifier in the output stage. To simplify the analysis of the proposed converter, the following statements are assumed.

- All components are ideal except the primary MOSFETs which include the anti-parallel body diode and the parasitic output capacitor. The transformer is composed of an ideal transformer, a leakage inductor, and a magnetizing inductor.
- The proposed converter is operating in steady-state.
- The capacitances of C_L, C_H, C_{SA}, and C_{SB} are large enough to be considered as constant voltage sources.

2.1 Modal Analysis

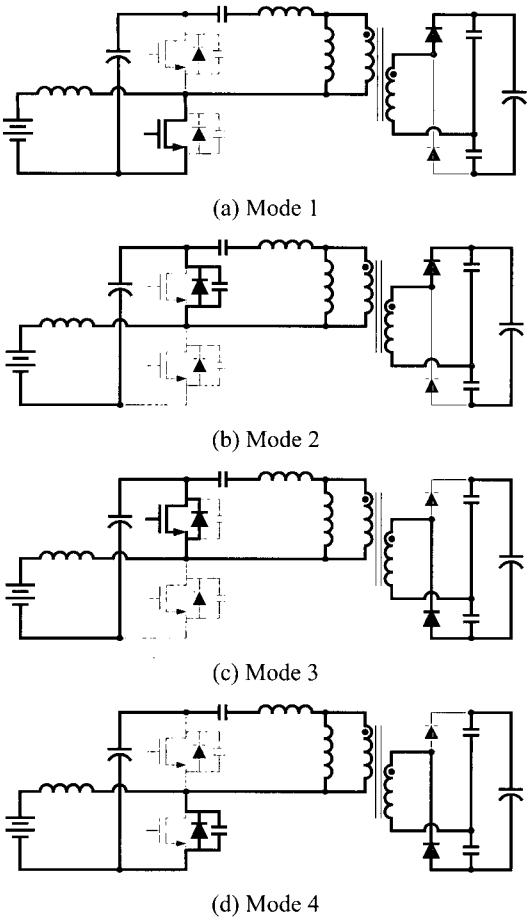
The proposed converter operates in four modes according to the switching states of the primary MOSFETs and the secondary diodes. The operational modes and the key waveforms are presented in Fig. 3 and Fig. 4, respectively. Before t_0, I_{LIN} flows through Q_M, and I_{LK} flows through D_M. In addition, I_{SEC} flows through D_{SB} and abruptly increases toward zero.

Mode 1 (M_1, t_0~t_1) : When I_{SEC} is increased to zero and D_{SB} is turned-off at t_0, Mode 1 begins and D_{SA} is turned-on as shown in Fig. 3(a). The boost inductor current, I_{LIN} and the transformer primary current, I_{LK} flows through Q_M, and linearly increases. The slopes of these currents are given by

$$\frac{d}{dt} I_{L_{IN}} = \frac{V_S}{L_{IN}} \tag{1}$$

$$\frac{d}{dt} I_{L_K} = \frac{1}{L_K}\left[(V_L - V_H) - \frac{N_P}{N_S} V_{SA} \right] \tag{2}$$

The transformer's secondary current, I_{SEC} flows through D_{SA}, and linearly increases, while C_{SA} is charged and C_{SB} is discharged.



(a) Mode 1

(b) Mode 2

(c) Mode 3

(d) Mode 4

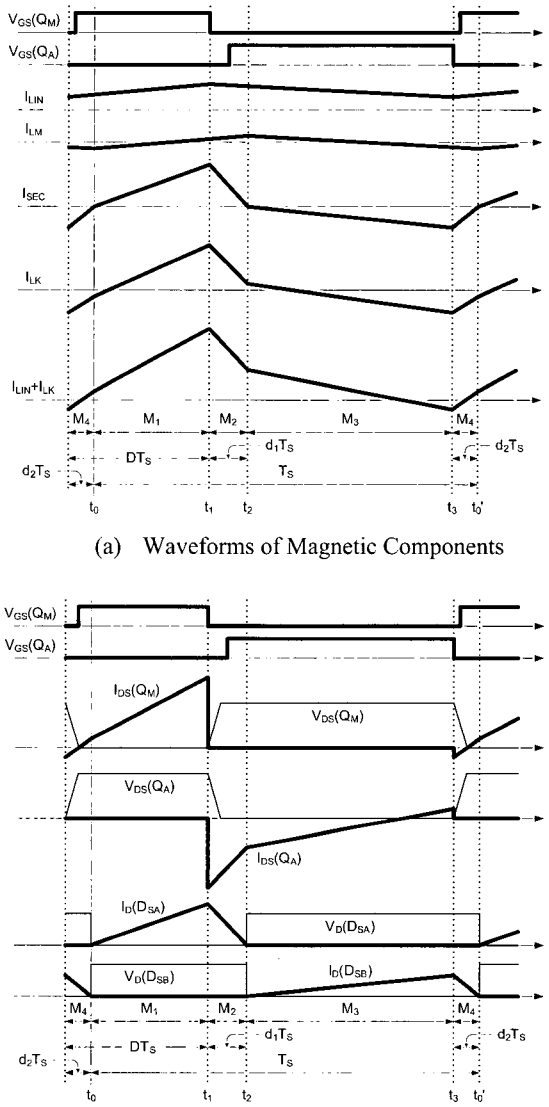
Fig. 3 Operational modes of the proposed converter

Mode 2 (M_2, t_1~t_2) : When Q_M is turned-off at t_1, Mode 2 begins, as shown in Fig. 3 (b). I_{LIN} and I_{LK} flow through the parasitic output capacitors, C_M and C_A. Provided that the gating signal of Q_A, $V_{GS}(Q_A)$ becomes actively high when C_M is charged to V_L and C_A is discharged to zero, ZVS turn-on of Q_A is obtained. After, I_{LIN} and I_{LK} flow through the anti-parallel body diode, D_A, and decrease linearly with the current slopes of the following equations.

$$\frac{d}{dt} I_{L_{IN}} = \frac{V_S - V_L}{L_{IN}} \tag{3}$$

$$\frac{d}{dt} I_{L_K} = \frac{1}{L_K}\left[(-V_H) - \frac{N_P}{N_S} V_{SA}\right] \tag{4}$$

I_{SEC} flows through D_{SA} and abruptly decreases, while C_{SA} is charged and C_{SB} is discharged.



(a) Waveforms of Magnetic Components

(b) Waveforms of Switching Components

Fig. 4 Key waveforms of the proposed converter

Mode 3 (M_3, t_2~t_3) : When I_{SEC} is decreased to zero and D_{SA} is turned-off at t_2, Mode 3 begins and D_{SB} is turned-on as shown in Fig. 3 (c). I_{LIN} flows through D_A, charging C_L, and decreases linearly with the slope of the equation (3). I_{LK} flows through Q_A and decreases linearly with the following slope.

$$\frac{d}{dt} I_{L_K} = \frac{1}{L_K}\left[(-V_H) + \frac{N_P}{N_S} V_{SB}\right] \tag{5}$$

I_{SEC} flows through D_{SB} and linearly decreases, while C_{SA} is discharged and C_{SB} is charged.

Mode 4 (M_4, t_3~t_0') : When Q_A is turned-off at t_3, Mode 4 begins, as shown in Fig. 3 (d). I_{LIN} and I_{LK} flow through the parasitic capacitors, discharging C_M and charging C_A. By firing Q_M after the full discharge of C_M, we can achieve ZVS turn-on of Q_M. And then I_{LIN} flows through Q_M, increasing with the slope of the equation (1), and I_{LK} flows through D_M, increasing with the slope given by

$$\frac{d}{dt}I_{L_K}=\frac{1}{L_K}\left[(V_L-V_H)+\frac{N_P}{N_S}V_{SB}\right] \tag{6}$$

I_{SEC} flows through D_{SB} and abruptly decreases, while C_{SA} is discharged and C_{SB} is charged.

2.2 Input-Output Voltage Conversion Ratio

In order to derive the output voltage equation, it is assumed that V_L, V_H, V_{SA}, V_{SB}, and V_O are constant during the switching period and the current of L_M is zero. By applying the voltage•second product equations on L_{IN}, L_K, and L_M during one switching period, the following equations can be easily obtained.

$$V_L=\frac{1}{1-D}V_S \tag{7}$$

$$V_H=DV_L \tag{8}$$

$$V_{SA}=(1-D-d_1+d_2)V_O=(1-D)V_O-\alpha \tag{9}$$

$$V_{SB}=(D+d_1-d_2)V_O=DV_O+\alpha \tag{10}$$

where D is the duty ratio of Q_M, and α is the correction factor. From the above equations, the peak currents of the secondary diodes are derived as follows:

$$I_{D,peak}(D_{SA})=\frac{N_P}{N_S}\frac{DT_S}{L_K}\left[(1-D)\left(V_L-\frac{N_P}{N_S}V_O\right)+\frac{N_P}{N_S}\alpha\right] \tag{11}$$

$$I_{D,peak}(D_{SB})=\frac{N_P}{N_S}\frac{(1-D)T_S}{L_K}\left[D\left(V_L-\frac{N_P}{N_S}V_O\right)-\frac{N_P}{N_S}\alpha\right] \tag{12}$$

By applying the current•second product equations on C_{SA} and C_{SB} during one switching period, the equation of α can be obtained as

$$\alpha=\frac{D(1-D)(1-2D)}{D^2+(1-D)^2}\frac{N_S}{N_P}\left(V_L-\frac{N_P}{N_S}V_O\right) \tag{13}$$

Therefore, the peak currents of the secondary diodes are arranged by substituting equation (13) into (11) and (12) as the following equations.

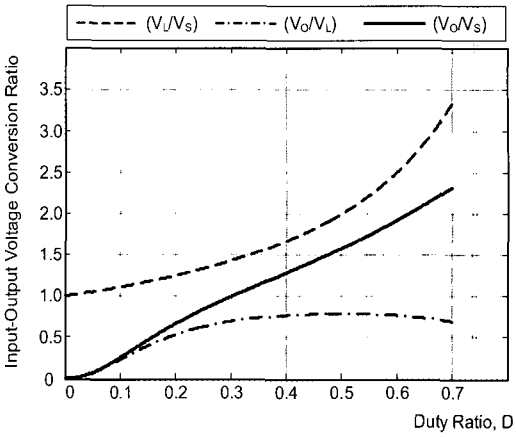


Fig. 5 Input-output voltage conversion ratio

$$I_{D,peak}(D_{SA})=\frac{N_P}{N_S}\frac{DT_S}{L_K}\frac{(1-D)^2}{D^2+(1-D)^2}\left(V_L-\frac{N_P}{N_S}V_O\right) \tag{14}$$

$$I_{D,peak}(D_{SB})=\frac{N_P}{N_S}\frac{(1-D)T_S}{L_K}\frac{D^2}{D^2+(1-D)^2}\left(V_L-\frac{N_P}{N_S}V_O\right) \tag{15}$$

Since the output load current equals the average current of D_{SA} or D_{SB}, it is given by

$$\begin{aligned}I_O&=\frac{V_O}{R_O}=\frac{1}{2}\times DT_S\times I_{D,peak}(D_{SA})\times\frac{1}{T_S}\\&=\frac{1}{2}\times(1-D)T_S\times I_{D,peak}(D_{SB})\times\frac{1}{T_S}\end{aligned} \tag{16}$$

Therefore, by substituting equations (14) or (15) into (16), the ratio of V_O to V_L is derived as

$$\frac{V_O}{V_L}=\frac{\frac{N_S}{N_P}D^2(1-D)^2}{D^2(1-D)^2+\left(\frac{N_S}{N_P}\right)^2\frac{2L_KF_S}{R_O}\left[D^2+(1-D)^2\right]} \tag{17}$$

where F_S is the switching frequency and it equals $1/T_S$. Finally, by substituting equation (7) into (17), we can obtain the input-output voltage conversion ratio of the proposed converter as the following equation.

$$M=\frac{V_O}{V_S}=\frac{\frac{N_S}{N_P}D^2(1-D)}{D^2(1-D)^2+\left(\frac{N_S}{N_P}\right)^2\frac{2L_KF_S}{R_O}\left[D^2+(1-D)^2\right]} \tag{18}$$

The input-output voltage conversion ratio is plotted as a function of duty ratio D in Fig. 5 under the conditions of $N_P/N_S = 1$, $L_K = 2\mu H$, $F_S = 100kHz$, and $R_O = 12\Omega$.

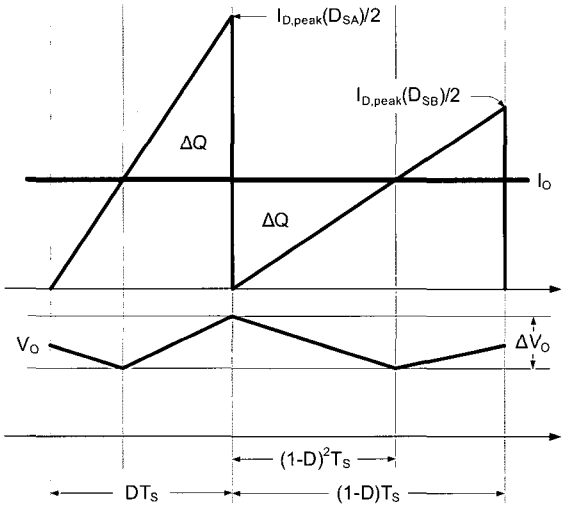


Fig. 6 Simplified output voltage and current waveforms

2.3 Output Voltage Ripple Ratio

In order to derive the output voltage ripple ratio of the proposed converter with the condition of D < 0.5, an increased charge or a decreased charge of the output capacitor is needed, as shown in Fig. 6. Moreover, the decreased charge can be obtained more easily as follows.

$$\Delta Q = C_O \Delta V_O = \frac{1}{2} \times I_O \times (1-D)^2 T_S \tag{19}$$

Therefore, by arranging the equation (19), the output voltage ripple ratio of the proposed converter can be obtained as

$$\frac{\Delta V_O}{V_O} = \frac{(1-D)^2}{2C_O R_O F_S}, \quad D < 0.5 \tag{20}$$

In addition, the output voltage ripple ratio with the condition of D > 0.5 can be derived similarly and it is given by

$$\frac{\Delta V_O}{V_O} = \frac{D^2}{2C_O R_O F_S}, \quad D > 0.5 \tag{21}$$

On the other hand, the output voltage ripple ratio of the conventional BHB converter is given by these equations.

$$\frac{\Delta V_O}{V_O} = \frac{|1-2D|}{16 L_O C_O F_S^2} \tag{22}$$

As can be seen in equations (20) and (21), the proposed converter shows relatively larger output voltage ripples than the conventional BHB converter. Since there is no need for an output inductor in the proposed converter, the properly sized output capacitor can be available without an increase in size.

2.4 ZVS Characteristics of Primary MOSFETs

ZVS of the primary MOSFETs is related to input current I_{LIN} and the transformer primary current I_{LK} at the switching instant. The current to achieve ZVS turn-on of Q_A at t_1 can be expressed by the sum of $I_{LK}(t_1)$ and $I_{LIN}(t_1)$ as follows.

$$I_{ZVS,Q_A} = I_{L_K}(t_1) + I_{L_{IN}}(t_1) \tag{23}$$

where

$$I_{L_K}(t_1) = \frac{1}{L_K F_S} \frac{D(1-D)^2}{D^2 + (1-D)^2} \left(\frac{1}{1-D} V_S - \frac{N_P}{N_S} V_O \right) \tag{24}$$

$$I_{L_{IN}}(t_1) = \frac{1}{\eta} \frac{V_O^2}{V_S R_O} + \frac{V_S}{2 L_{IN} F_S} D \tag{25}$$

and η is the efficiency of the proposed converter. Therefore, ZVS condition of Q_A is obtained as

$$\frac{1}{2} L_K I_{ZVS,Q_A}^2 \geq \frac{1}{2(1-D)^2} (C_M + C_A) V_S^2 \tag{26}$$

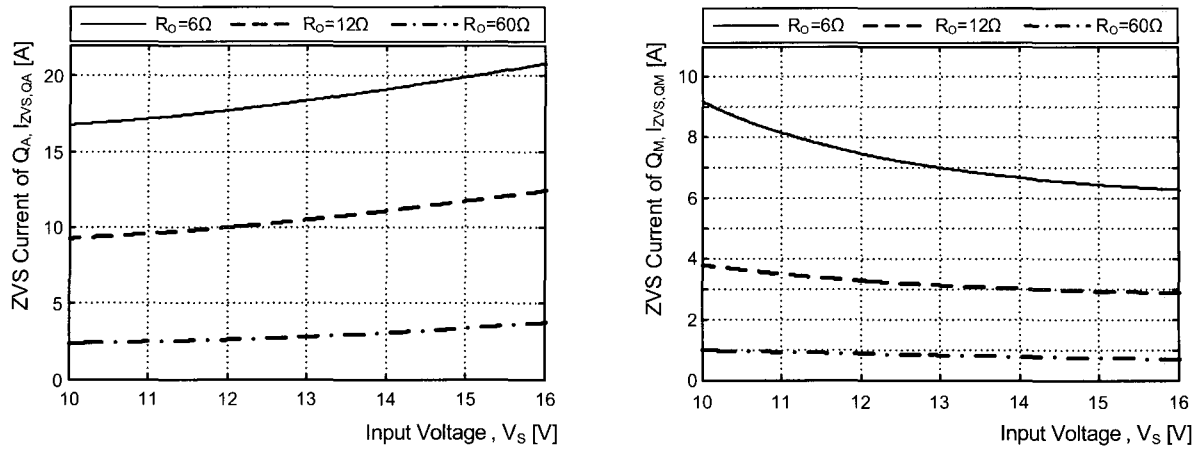
where C_M and C_A are the output capacitances of Q_M and Q_A, respectively. On the other hand, the current to obtain ZVS turn-on of Q_M at t_3 can be expressed by the difference of $|I_{LK}(t_3)|$ and $I_{LIN}(t_3)$ as follows.

$$I_{ZVS,Q_M} = |I_{L_K}(t_3)| - I_{L_{IN}}(t_3) \tag{27}$$

where

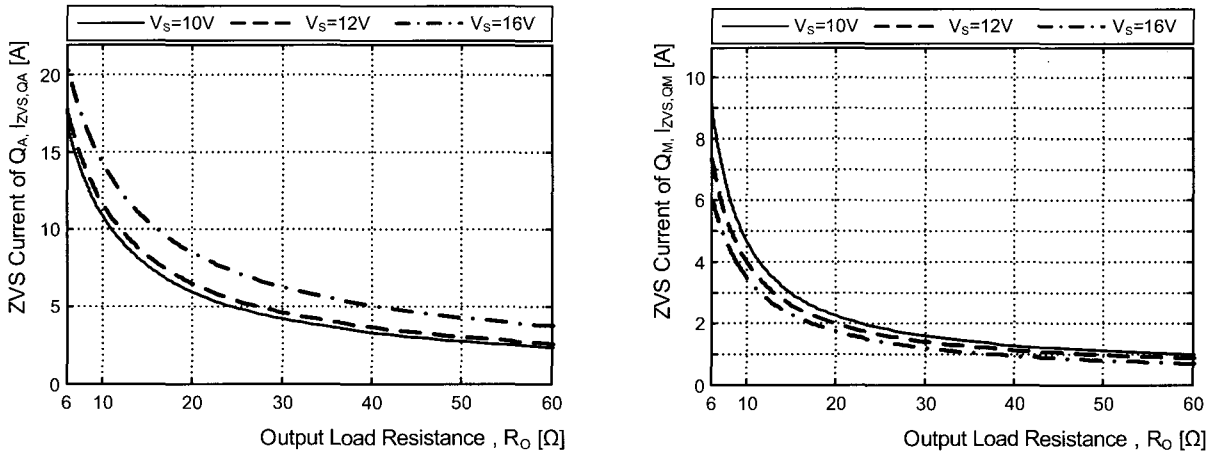
$$|I_{L_K}(t_3)| = \frac{1}{L_K F_S} \frac{D^2(1-D)}{D^2 + (1-D)^2} \left(\frac{1}{1-D} V_S - \frac{N_P}{N_S} V_O \right) \tag{28}$$

$$I_{L_{IN}}(t_3) = \frac{1}{\eta} \frac{V_O^2}{V_S R_O} - \frac{V_S}{2 L_{IN} F_S} D \tag{29}$$



(a) ZVS Current of Q_A (b) ZVS Current of Q_M

Fig. 7 ZVS current of primary MOSFETs as the function of the input voltage



(a) ZVS Current of Q_A (b) ZVS Current of Q_M

Fig. 8 ZVS current of primary MOSFETs as the function of the load resistance

Thus, the ZVS condition of Q_M is obtained as

$$\frac{1}{2}L_K I_{ZVS,Q_M}{}^2 \geq \frac{1}{2(1-D)^2}(C_M + C_A)V_S^2 \tag{30}$$

With the condition of N_P:N_S = 1:1, L_{IN} = 50μH, L_K = 2μH, and F_S =100kHz, ZVS currents of the primary MOSFETs are plotted as functions of the input voltage and the load resistance in Fig. 7 and Fig. 8, respectively. In this case, ZVS turn-on of Q_M, as well as Q_A, can be obtained from 10% to 100% output load in the overall input voltage range, provided that the primary MOSFETs are selected to satisfy the following equation.

$$C_M + C_A \leq 1.862\text{nF} \tag{31}$$

2.5 Advantages of Proposed Converter

The advantages of the proposed converter are as follows:

i) The BHB converter has a DC offset of the transformer magnetizing current given by

$$DC\ Magnetizing\ Current = I_{L_M,DC} = \frac{N_S}{N_P}(1-2D)\frac{V_O}{R_O} \tag{32}$$

where $N_S = N_{S1} = N_{S2}$. On the other hand, the proposed converter has no DC offset of the transformer's

magnetizing current due to the series-connected DC blocking capacitors, C_H, C_{SA}, and C_{SB}. That is, since the average currents of both the primary and the secondary sides of the transformer are zero, the average current of the magnetizing inductor is also zero. As a result, since optimal design of the transformer is possible, the size of the transformer can be minimized and the radiated heat of the transformer can be greatly reduced.

ii) The voltage stress of secondary diodes, D_{S1} and D_{S2} in the BHB converter is given by

$$Voltage\ Stress\ of\ D_{S1} = V_{D_{S1}} = 2\frac{N_S}{N_P}V_H = V_O/(1-D) \quad (33)$$

$$Voltage\ Stress\ of\ D_{S2} = V_{D_{S2}} = 2\frac{N_S}{N_P}(V_L - V_H) = V_O/D \quad (34)$$

where $N_S = N_{S1} = N_{S2}$. Therefore, the voltage stress of D_{S2} increases at high input voltage and light load conditions. However, in the proposed converter, the voltage stresses of the secondary rectifier diodes, D_{SA} and D_{SB} are always clamped to the output voltage V_O regardless of the duty ratio D as follows.

$$Voltage\ Stress\ of\ D_{SA} = V_{D_{SA}} = V_O \quad (35)$$

$$Voltage\ Stress\ of\ D_{SB} = V_{D_{SB}} = V_O \quad (36)$$

The voltage stresses, normalized by V_O, of the secondary diodes in both converters as the functions of the duty ratio, D are shown in Fig. 9.

iii) In the conventional BHB converter, a serious voltage ringing exists in the secondary diodes. Thus, an RC snubber or transient-voltage-suppressor (TVS) has to be used, which deteriorates efficiency. Conversely, since the secondary diodes of the proposed converter are turned-off under ZCS condition, the turn-off voltage oscillation is very small. Therefore, since the use of the snubbers is not necessary, the proposed converter can achieve high efficiency.

iv) Since the proposed converter has no output inductor, conduction loss can be greatly reduced, and this is desirable for a low profile and lower cost.

v) In the BHB converter, the non-power-transfer time interval exits due to the commutation of D_{S1} and D_{S2}. Thus, the effective duty ratio, D_{eff}, is decreased in the BHB converter as in the following equation.

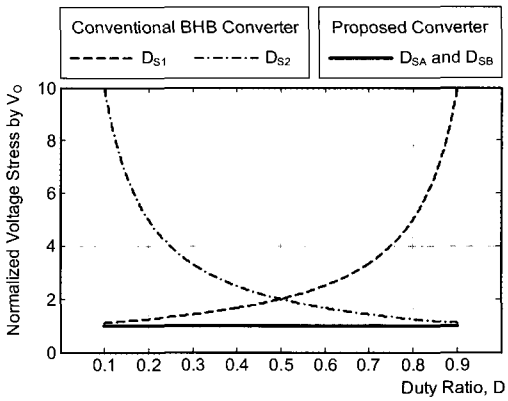


Fig. 9 Normalized voltage stress of the secondary diodes

$$D_{eff} = D - 2L_K I_{L_O} F_S \frac{N_S}{N_P}\left(\frac{1}{V_H} + \frac{1}{V_L - V_H}\right) \quad (37)$$

On the other hand, the proposed converter always transfers the power of the primary stage to the secondary stage in the overall switching period and has no freewheeling energy. Thus, high efficiency can be obtained without large circulating energy loss in the proposed converter.

vi) Since the primary MOSFETs, Q_M and Q_A, of the proposed converter are turned-on under the ZVS condition, switching loss can be minimized.

vii) Since the input current is continuous, the proposed converter has a the minimized input filter.

Although the current stresses of the secondary diodes in the proposed converter are rather large compared with those in the conventional BHB converter, the proposed converter has high efficiency due to minimized conduction and switching losses. Furthermore, the proposed converter shows desirable features such as high power density and low profile due to the reduced count and size of magnetic components. In addition, the proposed converter is expected to have a low EMI due to the wide ZVS range of the primary MOSFETs, and ZCS turn-off of the secondary diodes.

3. Experimental Results

To verify the operational principles and the feasibility of the proposed converter, the 60W industrial sample of the proposed converter is implemented by employing the metal printed-circuit-board (PCB) for digital car audio

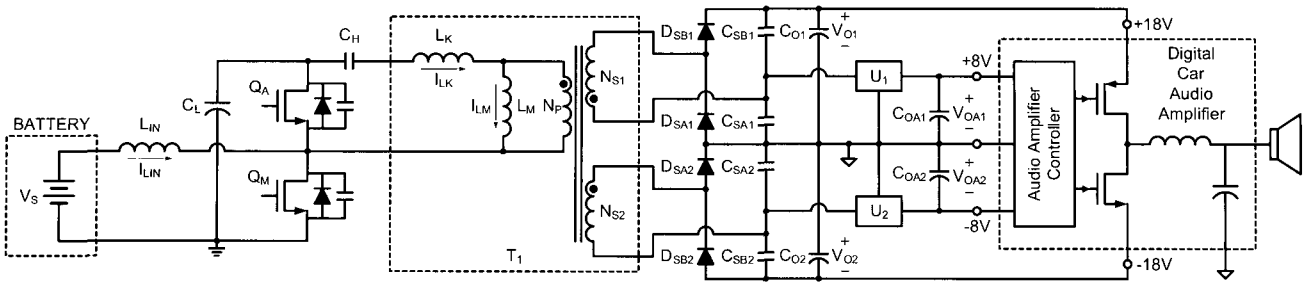


Fig. 10 Circuit diagram of 60W sample for digital car audio amplifiers

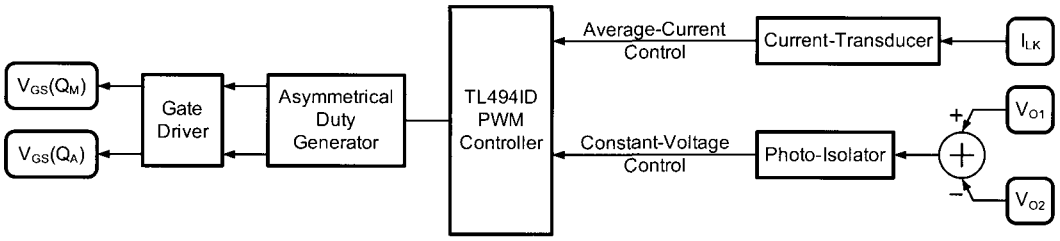


Fig. 11 Control scheme of 60W sample for digital car audio amplifiers

amplifiers. The circuit diagram and the control scheme of the proposed system are shown in Fig. 10 and Fig. 11, respectively. As can be seen in Fig. 10, the proposed converter produces ± 18V and ± 8V as a power supply for the power stage and the controller stage of digital car audio amplifiers, respectively. The dimension of the industrial sample is 129(L)×48(W)×13(H) [mm] and its photograph is presented in Fig. 12.

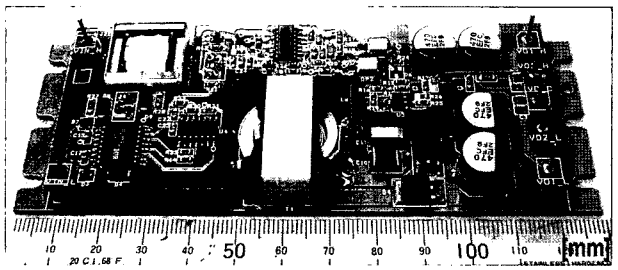


Fig. 12 Photograph of 60W industrial sample for digital car audio amplifiers

Table 1 Design Specification for Digital Audio Amplifiers

Input Voltage, V_S	10V ~ 16V, 12V Nominal
Output Voltage, V_O	+18V(1.5A) and –18V(1.5A)
Auxiliary Output Voltage, V_{OA}	+8V(0.4A) and –8V(0.4A)
Maximum Output Power, $P_{O,max}$	60W
Switching Frequency, F_S	100kHz

Table 2 Circuit Parameters for Digital Audio Amplifiers

L_{IN}	50μH, EPC17 (TDK)
C_L	100μF, 35V, Electrolytic, 2EA
C_H	22μF, 25V, MLCC, 2EA
C_{SA1}, C_{SB1}, C_{SA2}, C_{SB2}	22uF, 25V, MLCC
	22uF, 25V, Tantal
C_{O1}, C_{O2}	470uF, 35V, Electrolytic, 2EA
T_1	PQ2610 (Magnetics)
	L_M = 100μH, L_K = 2μH
	N_P = 3, N_{S1} = 3, N_{S2} = 3
Q_M	IRF1104S, D2-Pak (C_{OSS} = 1.10nF)
Q_A	IRFR3504, D-Pak (C_{OSS} = 0.58nF)
D_{SA1}, D_{SB1}, D_{SA2}, D_{SB2}	12CWQ03FN, D-Pak
U_1	UA78M08C, D-Pak
U_2	UA79M08C, D-Pak

The design specifications of the sample are shown in Table 1. While the circuit parameters and the selected components are shown in Table 2. Moreover, the primary MOSFETs are chosen by the ZVS condition of Q_M, as presented in the equation (31). The input current, I_{LIN} and the transformer primary current, I_{LK}, at the nominal input voltage, is presented in Fig. 13. The input current is continuous and it has the small current ripple of 1.3A. The

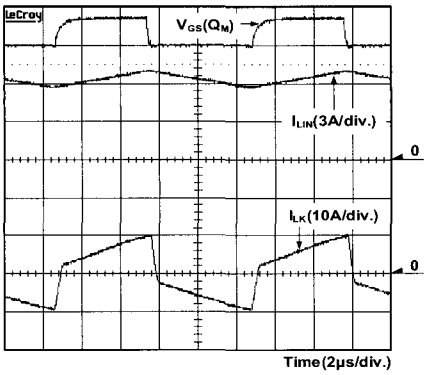


Fig. 13 Experimental waveform of I_{LIN} and I_{LK} at V_S = 12V

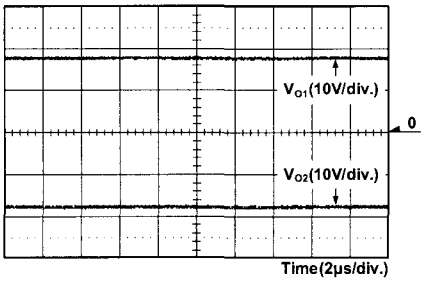
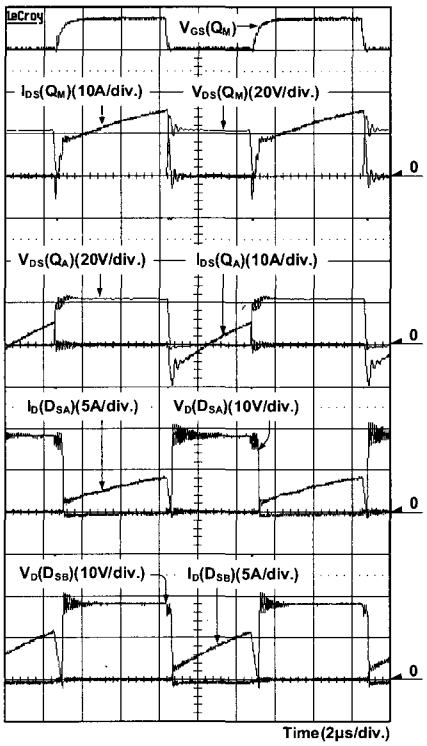
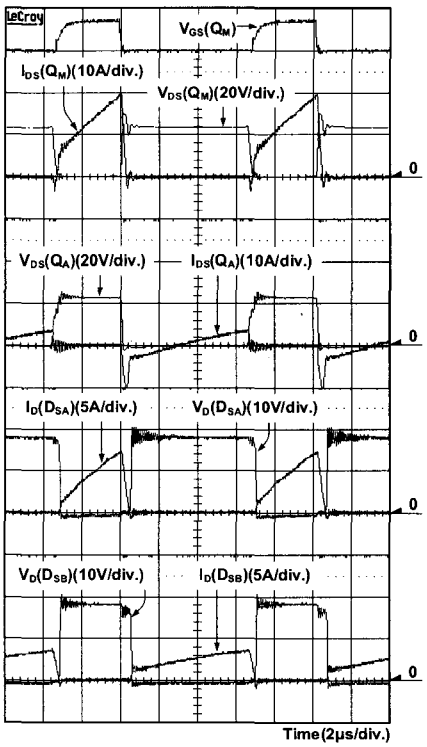


Fig. 14 Experimental waveforms of output voltages at V_S = 12V

waveform of I_{LK} agrees well with the theoretical waveform, as shown in Fig. 4, and it is balanced around zero for maximum efficiency at the nominal input voltage. Fig. 14 shows the output voltages of +18V and −18V with greatly reduced output voltage ripples and switching noises. The switching waveforms of the proposed converter at both the minimum and the maximum input voltages are presented in Fig. 15. As can be seen in this figure, the primary MOSFETs, Q_M and Q_A are turned-on under the ZVS condition and the secondary rectifier diodes are turned-off under ZCS condition at both the input voltages. In addition, the voltage stress of the secondary rectifier diodes is clamped to the output voltage, 18V, and the voltage oscillation is considerably small without the snubbers. The measured efficiencies of the proposed converter and the BHB converter are compared in Fig. 16. At nominal input voltage, the efficiency of the proposed converter is 88.3% and that of the BHB converter 84.8%. As can be seen in Fig. 16, the proposed converter shows higher efficiency than the conventional BHB converter in the overall input voltage range.



(a) V_S = 10V



(b) V_S = 16V

Fig. 15 Experimental waveforms of switching components

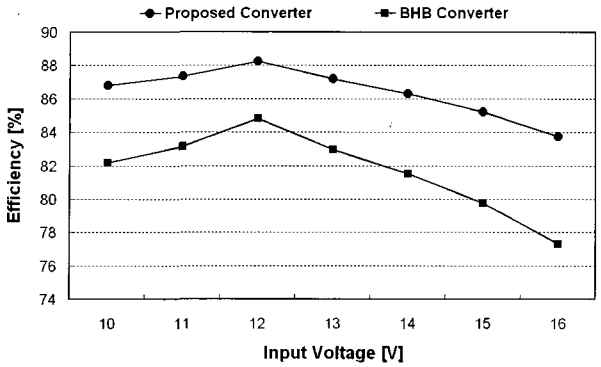


Fig. 16 Measured efficiencies

4. Conclusions

In this paper, a new high efficiency and low profile on-board DC/DC converter for digital car audio amplifiers is proposed. The proposed converter shows a lack of DC magnetizing current for the transformer, low voltage stress of the overall active components, ZCS turn-off of the secondary diodes and no output inductor. Furthermore, the proposed converter has a wide ZVS range for the primary MOSFETs and a continuous input current.

The operational principles of the proposed converter were analyzed and the advantages were described. A 60W industrial sample of the proposed converter was implemented for digital car audio amplifiers to confirm the advantages of the proposed converter. The measured efficiency of the proposed converter was 88.3% at the nominal input voltage which is higher than that of the BHB converter at the overall input voltage range. The proposed converter demonstrates suitability for high efficiency and low profile on-board DC/DC converters for digital car audio amplifiers and other low input voltage applications.

Acknowledgment

This work was supported through research funds by NGVtek, Hyundai Motor Company, and Hyundai Autonet, Korea.

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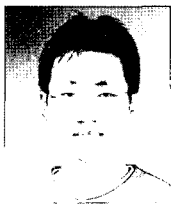

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