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A New High Efficiency Phase Shifted Full Bridge Converter for a Power Sustaining Module of Plasma Display Panel

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ABSTRACT

A new high efficiency phase shifted full bridge (PSFB) converter for the power sustaining module of a plasma display panel (PDP) is proposed in this paper. The proposed converter employs a voltage doubler rectifier without an output inductor. Since it has no output inductor, the voltage stresses of the secondary rectifier diodes can be clamped at the output voltage level. No dissipative resistor-capacitor (RC) snubber for rectifier diodes is needed. Therefore, high efficiency, as well as, a low noise output voltage can be realized. Due to the elimination of the large output inductor, it features a simple structure, lower cost, smaller mass and lighter weight. Furthermore, the proposed converter has wide zero voltage switching (ZVS) ranges with low current stresses of the primary switches. Also the resonance between the leakage inductor of the transformer and the capacitor of the voltage doubler cell reduces the current stresses of the rectifier diodes. In this paper, operational principles, an analysis of the proposed converter and experimental results are presented.

Keywords: phase shifted full bridge converter, voltage doubler rectifier, PDP

1. Introduction

Plasma display panels (PDPs) are gaining popularity for its use in large area wall-hanging color TVs, because it has various advantages over conventional display devices. Such advantages include a large screen, a wide viewing angle, light weight, thin, a long life time and a high contrast [1-3]. The operation of a PDP can be divided into three periods: resetting, addressing and sustaining periods. During the sustaining period, a high voltage sustaining pulse makes the PDP emit light by inducing gas discharge [1-3]. Since most of the power driving of the PDP is consumed during this period, the sustaining power module is especially responsible for overall system efficiency. Recent wall hanging PDP color TVs tend to be smaller, lighter and contain a fan-less system for lower acoustic noise and vibration. These TVs also have high power density, high performance and high efficiency which make it a hot issue in PDP power modules[1-3]. Therefore, among various DC/DC converters developed, the conventional

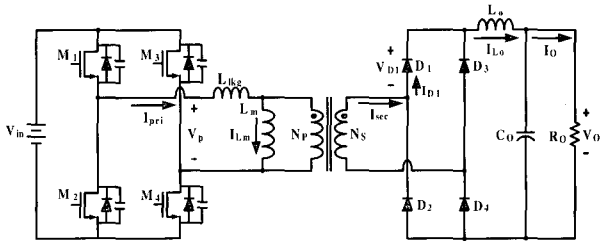

Fig. 1 Circuit diagram of the conventional PSFB converter

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phase shifted full bridge converter (as shown in Fig. 1), which is widely used in mid/high power applications like PDP power modules, has been proposed to reduce component current/voltage stress and to provide the ZVS operation of all power switches [4]. However, it has several serious problems such as a narrow ZVS range with lagging leg switches, serious voltage ringing in the secondary rectifier, considerable heat, a bulky cooling system and noisy output voltage [5-6]. During the transition of the lagging leg, only the energy stored in the leakage inductor is related to the charge and discharge of the output capacitors (C_{oss}) of the lagging leg switches. Since the energy available for providing ZVS operation of these switches is dependent on load condition, it is inevitable that hard switching is necessary for operations at light loads. Additionally, the voltage ringing problem of the rectifier diodes is more serious in cases of high voltage applications like the PDP power sustaining module. Thus, for the resistor-capacitor (RC) snubber to absorb the serious voltage ringing a secondary rectifier is needed. This results in poor overall system efficiency, since the energy stored in the snubber capacitor is not only very large, but also all dissipated through the snubber resistor [5-7]. To resolve these problems, the proposed converter employs the voltage doubler rectifier which has no output inductor. Due to the output inductor, the voltage stresses of the secondary rectifier diodes can be clamped at the output voltage and the structure is simplified. Therefore, no dissipative RC snubber for a rectifier diode is needed and a high efficiency, as well as, a low noise output voltage can be realized. Moreover, a zero current switching (ZCS) turn off of the rectifier diode can be achieved. The ZVS turn on of the primary switches also can be easily achieved by using the magnetizing current regardless of the load condition. Although the current stresses of the rectifier diodes D1 and D2 are rather large compared with those of conventional PSFB converters, because of the half bridge configuration, the resonance between the leakage inductor of the transformer and the capacitor of the voltage doubler cell can reduce the current stresses of the secondary rectifiers. Thus, the proposed converter, which is suitable for high voltages and low current applications, can effectively overcome the above problems and realize high power density, high performance and high efficiency.

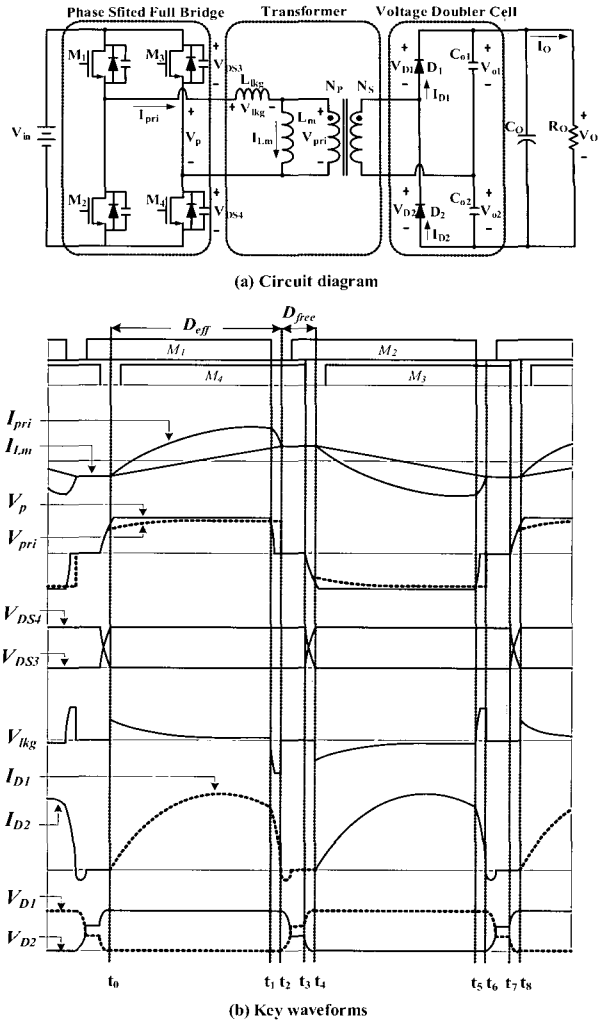


Fig. 2 The proposed PSFB converter

2. Operational Principles

Fig. 2 shows the circuit diagram and operational waveforms of the proposed converter, respectively. As shown in Fig. 2(a), the proposed converter is a phase shifted full bridge converter with the voltage doubler type rectifier stage. The operation of the proposed converter can be divided into eight modes. One switching cycle of the proposed circuit is divided into two half cycles, t_0~t_4 and t_4~t_8. Since the operation principles of the two half cycles are symmetric, only the first half cycle is explained. A half cycle can be divided into 4 modes and its equivalent circuits are shown in Fig. 3. The switches of the leading leg (M_1 and M_2) and the lagging leg (M_3 and M_4) are turned on and off alternately with the constant

duty ratio. The phase difference between both legs determines the operational duty cycle of the converter, where $D_{eff}T_s$ is the operational conduction time and $D_{freq}T_s$ is the phase shifted time. To illustrate a steady state operation, it is assumed that the power switches (M_1~M_4) are ideal except for their internal diodes and output capacitors (=C_{oss}). The output voltage V_o is constant.

Mode 1 (t_0~t_1) : After the ZVS condition of M_4 is achieved (V_{DS4} = 0V), the primary current I_{pri}, which rises with resonance between the leakage inductor and rectifier capacitor and the magnetizing current I_{Lm}, rises linearly given by

$$I_{pri}(t) = I_{Lm}(t_0)\cos\omega_r(t-t_0) + \left(\frac{(V_{in}-nV_{o1})}{Z_o}\right)\sin\omega_r(t-t_0) \quad (1)$$

$$I_{Lm}(t) = I_{Lm}(t_0) + \frac{nV_{o1}}{L_m}(t-t_0) \quad (2)$$

where, $\omega_r = n\sqrt{\frac{1}{L_{lkg}C_r}}$, $Z_o = n\sqrt{\frac{L_{lkg}}{C_r}}$, $n = \frac{N_p}{N_s}$, $C_r = C_{o1} // C_{o2}$

Before M_4 is turned on, I_{pri} flows through the internal diode of M_4. Thus, the ZVS of M_4 is guaranteed. After M_4 is turned on, I_{pri} flows through the channel of M_4 and then the direction of I_{pri} is changed. The current of rectifier diode D_1 is I_{D1}, flowing through C_{o1}. Therefore the rectifier capacitor C_{o1} is charged, while C_{o2} is discharged.

Mode 2 (t_1~t_2) : When M_1 is turned off at t_1, Mode 2 begins. The primary current at t_1 occurs when $I_{pri}(t_1)$ starts to charge and discharge the output capacitors of M_1 and M_2. Therefore the voltage across the transformer primary side V_p, is decreased to 0V and concurrently the voltage across L_{lkg}. V_{lkg} is also decreased. After V_{lkg} is the same as $-nV_{o1}$(=V_{pri}), the primary current is decreased with a slope of $-nV_{o1}/L_{lkg}$. At the same time, the secondary side of the transformer operates similarly to Mode 1.

Mode 3 (t_2~t_3) : When the primary current I_{pri} becomes equal to the magnetizing current I_{Lm}, Mode 3 begins. Since the primary current I_{pri} becomes smaller than the magnetizing current I_{Lm}, the direction of the secondary current I_{sec} is reversed and the commutation between D_1 and D_2 begins. After M_2 is turned on, the voltage across the primary of transformer V_p is maintained to 0V. Primary current I_{pri} is still equal to $I_{Lm}(t_2)$.

Mode 4 (t_3~t_4) : After M_4 is turned off, the voltage across the primary of transformer V_p is decreased to $-V_{in}$. At t_4, the commutation between D_1 and D_2 is completed.

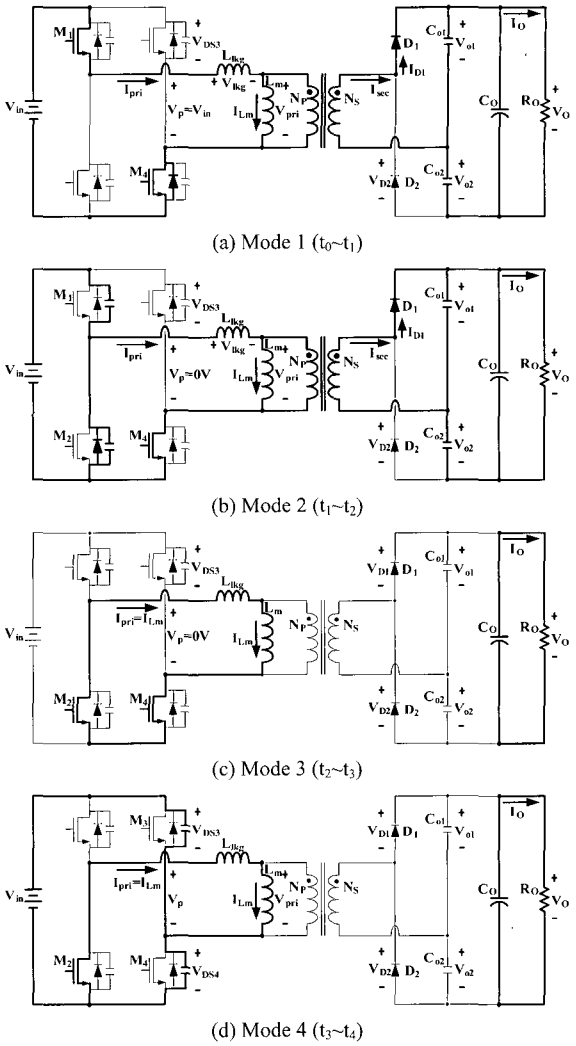


Fig. 3 Equivalent circuit of the proposed converter

3. Analysis of the Proposed Converter

3.1 DC conversion ratio

In order to derive the DC conversion ratio, several assumptions are made as follows:

- The capacitor C_{o1}, C_{o2} and output capacitor C_o are large enough to be considered as a constant voltage source V_{o1}, V_{o2}, and V_o respectively.
- The magnetizing inductor L_m is so large that I_{Lm}=0.
- The primary current I_{pri} is increased and decreased linearly.

- Since time intervals t_1~t_2 and t_5~t_6 are much smaller than switching period T_s, they can be discarded for simplicity of analysis.
- Dead time is discarded. Hence, only the phase shifted time $D_{free}T_s$ is considered. During this period, the energy can not be transferred to the output stage.

By imposing the volt-second balance rule on the magnetizing inductor L_m for one switching cycle, the steady state equation can be obtained as

$$nV_{o1}\frac{D_{eff}T_s}{2} = nV_{o2}\frac{D_{eff}T_s}{2} \tag{3}$$

$$V_{o1} = V_{o2} \tag{4}$$

Since the sum of V_{o1} and V_{o2} is always the same as output voltage V_o, (by KVL) the relation between V_{o1}, V_{o2} and V_o can be expressed as follows

$$V_{o1} = V_{o2} = \frac{V_o}{2} \tag{5}$$

The operation of the proposed converter is symmetric during one switching cycle. Only a half cycle is considered. By averaging the current of the secondary rectifier, the input-output voltage gain is expressed by

$$I_o = \frac{V_o}{R_o} = avg(I_{D1}) = \frac{2n}{T_s}\left[\frac{1}{2}\frac{V_{in}-nV_{o1}}{L_{lkg}}D_{eff}^2\frac{T_s^2}{2}\right] \tag{6}$$

where, avg<•> means the average value of '•'.

From equations (5) and (6), the steady state voltage conversion ratio of the overall system can be derived as follows

$$\frac{V_o}{V_{in}} = \frac{1}{\frac{4L_{lkg}}{nR_oT_sD_{eff}^2}+\frac{n}{2}} \tag{7}$$

3.2 Zero –voltage switching

Fig. 5 shows the different ZVS operations of the conventional PSFB and proposed PSFB converters. For a convenient description of the ZVS operation, it is assumed that the output capacitors (C_{oss}) of all switches have the same capacitance and magnetizing current is constant during t_2~t_4. In the conventional PSFB converter, the ZVS operation of the leading leg switches can be easily achieved due to the large reflected load current.

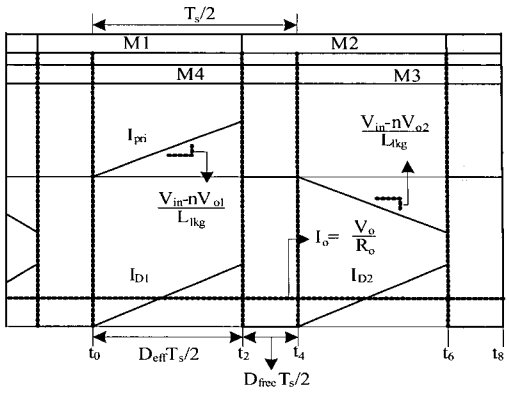


Fig. 4 Simplified waveforms

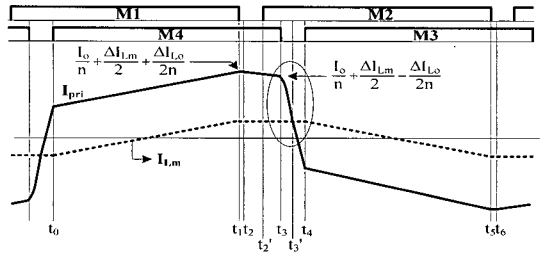
However, as mentioned above, the conventional PSFB converter will eliminate the ZVS operation of lagging leg switches at reduced load currents. During the resonant transition of lagging leg switches (t_3~t_4 as shown in Fig. 5(a)) the primary current I_{pri}, which is available for the ZVS is decreased rapidly because of the commutation of the secondary rectifier diodes. Hence the energy stored in the leakage inductor is insufficient to achieve the ZVS operation of M_3 at a light load. Therefore the ZVS operation of lagging leg switches can not be guaranteed according to load variations. On the other hand, due to the use of the magnetizing current, the proposed PSFB converter has a good performance in the ZVS operation of all power switches regardless of load conditions. In order to achieve the ZVS operation of the leading leg switch M_2, the energy E_{lkg_t1} stored in the leakage inductor at t_1 should be larger than the energy required to fully charge and discharge C_{oss} of M_1 and M_2. Although the leakage inductor and its primary current are not large enough to achieve the ZVS of M_2, the energy E_{Lm_t2} stored in the magnetizing inductor additionally helps the ZVS of M_2 at the next mode (t_2~t_2' as shown in Fig. 5(b)).

$$E_{lkg\_t1} = \frac{1}{2}L_{lkg}I_{pri}(t_1)^2 \geq \frac{1}{2}2C_{oss}V_{in}^2 \tag{8}$$

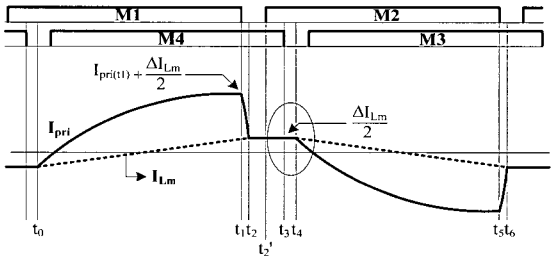
$$E_{Lm\_t2} = \frac{1}{2}L_mI_{Lm}(t_2)^2 \geq \frac{1}{2}2C_{oss}V_{in}^2 - \frac{1}{2}L_{lkg}I_{pri}(t_1)^2 \tag{9}$$

Where,

$$I_{pri}(t_1) = \frac{\Delta I_{Lm}}{2}\cos(\omega_r\Delta t) + \frac{(V_{in}-nV_{o1})}{Z_o}\sin(\omega_r\Delta t)$$



(a) Conventional PSFB converter



(b) Proposed PSFB converter

Fig. 5 Comparative analysis of the ZVS operation

$$I_{Lm}(t_2) = \frac{\Delta I_{Lm}}{2} = \frac{1}{2}\frac{nV_{o1}}{L_m}\Delta t$$

$$\Delta t = D_{eff}\frac{T_s}{2}$$

For the ZVS operation of the lagging leg switch M_3, only the energy E_{Lm_t3} stored in the magnetizing inductor is related to that operation.

$$E_{Lm\_t3} = \frac{1}{2}L_m I_{Lm}(t_3)^2 \geq \frac{1}{2}2C_{oss}V_{in}^2 \qquad (10)$$

Where,

$$I_{Lm}(t_3) = \frac{\Delta I_{Lm}}{2} = \frac{1}{2}\frac{nV_{o1}}{L_m}\Delta t$$

In order to guarantee the safety of the ZVS of lagging leg, the dead time (Δt_{dead}) can be calculated using the equation I_c=C(dV/dt).

$$\left|I_{Lm}(t_3)\right| = 2C_{oss}\frac{dV_{in}}{dt} \qquad (11)$$

where |▪| means the absolute value of '▪'. From this equation (11), the dead time can be expressed in the following equation

$$\Delta t_{\_dead} = C_{oss}\frac{V_{in}}{\left|I_{Lm}(t_3)\right|/2} \qquad (12)$$

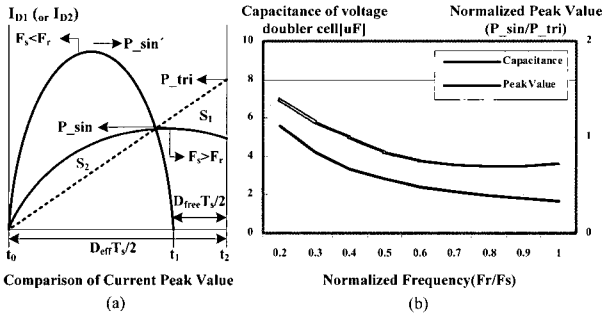


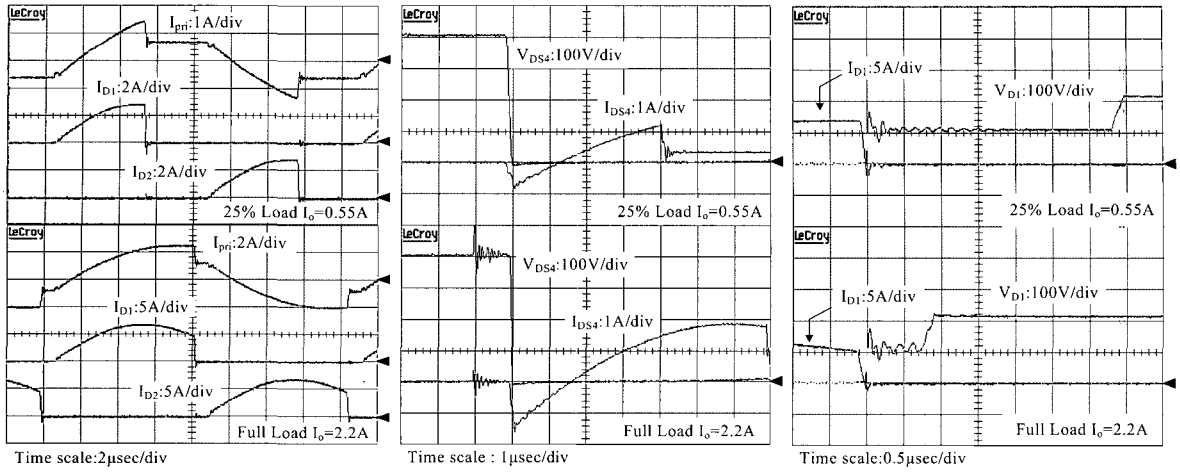
Fig. 6 Analysis of the current waveform

3.2 Reduction of current stress by using resonance

A disadvantage of the proposed converter is the current stresses of the rectifier diodes are rather large. This is because the proposed converter employs an output structure which is a half bridge configuration. However, the resonance between the leakage inductor and the capacitors of the transformer's secondary side reduces the current stresses of rectifier diodes. As mentioned above, the load current can be determined by averaging the current of the rectifier diode I_{D1} (or I_{D2}), i.e. it is closely connected with the area of I_{D1}. As shown in Fig. 6(a) when switching frequency F_s, is slower than F_r which is the resonant frequency, the peak value (= P_sin') of I_{D1} must be larger than P_tri. The peak value of I_{D1} in the current waveform is triangular.

To have the same area, P_sin' must rise to compensate for the reduced time period, $D_{free}T_s/2$. However, when F_s is faster than F_r, the peak value P_sin, can be smaller than P_tri. This is because S_2 is the same as S_1, both the area of the triangular form and that of the sinusoidal one are exactly same. Fig. 6(b) shows the variation of the normalized peak value (=P_sin/P_tri) according to the normalized frequency (=F_r/F_s). In this figure, the normalized peak value is only considered when $F_r<F_s$. The capacitance of the voltage doubler cell can be plotted when the leakage inductance of the transformer is $23\mu H$. Therefore, as shown in this figure, the capacitance should be selected when the normalized peak value is below 1.

$$C_{o1} = \frac{n^2}{4\pi^2 L_{lkg}F_s^2\left(F_r/F_s\right)^2} \qquad (13)$$



(a) I_{pri}, I_{D1}, and I_{D2} (b) ZVS of lagging leg switch (M_4) (c) ZCS of rectifier diode (D_1)

Fig. 7 Experimental waveforms at 25% and Full load

4. Experimental Results

A 450W prototype of the proposed converter was built. The parameters of this prototype circuit are listed in Table 1. Fig. 7 shows the experimental waveforms at 25% and at full load. As can be seen in Fig. 7(b), the ZVS of the lagging leg switches can be easily achieved using the magnetizing current regardless of the load condition. Since the voltages across D_1 and D_2 are always clamped at the output voltage V_o, there is no serious voltage ringing in the rectifier diodes. Furthermore, ZCS turn off can be achieved. The waveforms of I_{D1} and I_{D2} are not a triangular form but a sinusoidal one.

This results in low current stresses of D_1 and D_2. In addition, the DC offset of the transformer magnetizing current and magnetic flux are completely blocked. Therefore, the transformer magnetic core is fully utilized, and its power density can be considerably increased while the heat generation of the transformer can be greatly reduced. Also the currents of I_{D1} and I_{D2} are balanced.

Table 1 The parameters of prototype circuit

Item	Symbol	Value/Part
Switching Frequency	F_s	60kHz
Turn Ratio	n:1	3.23:1
Leakage inductance	L_{lkg}	23uH
Magnetizing inductance	L_m	1.4mH
Capacitance of doubler cell	C_{o1},C_{o2}	2.2uF/630V
Output Capacitance	C_o	1000uF/250V
Power Switches	$M_{1\sim4}$	FQP12N60
Rectifier Diodes	$D_{1\sim2}$	15ETH03

5. Conclusions

A new high efficiency phase shifted full bridge converter for a PDP power sustaining module is proposed in this paper. The proposed converter employs a voltage doubler type rectifier without output inductor to solve problems related to the voltage ringing of the secondary rectifier. In addition, since it has no large output inductor filter, it features a simpler structure, lower cost, less mass and lighter weight. Furthermore, the proposed converter has wide ZVS ranges with low current stresses of the primary switches. Also the resonance between the leakage inductor of the transformer and the capacitor of voltage

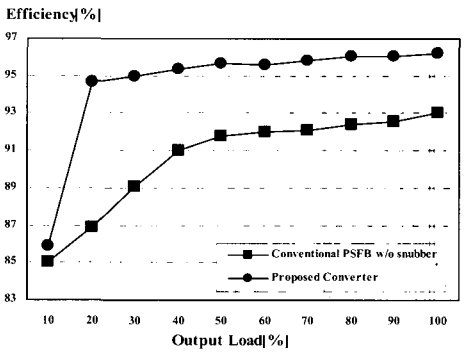


Fig. 8 The measured efficiency

doubler cell can reduce the current stresses of the rectifier diodes. A prototype was used in experiments to prove the validity of the proposed converter. Fig. 8 shows the measured efficiency. The measured efficiency with wide load ranges, as high as around 96%., demonstrated a higher efficiency than in conventional PSFB converters. Therefore, the improved efficiency of the proposed converter demonstrates its suitability as sustaining power module owing to its high reliability, low noise, and high efficiency.

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