Electrical Switching Characteristics of $Ge_1Se_1Te_2$ Chalcogenide Thin Film for Phase Change Memory

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The changes of the electrical conductivity in chalcogenide amorphous semiconductors, $Ge_1Se_1Te_2$, have been studied. A phase change random access memory (PRAM) device without an access transistor is successfully fabricated with the $Ge_1Se_1Te_2$-phase-change resistor, which has much higher electrical resistivity than $Ge_2Sb_2Te_5$ and its electric resistivity can be varied by the factor of 10^5 times, relating with the degree of crystallization. 100 nm thick $Ge_1Se_1Te_2$ thin film was formed by vacuum deposition at 1.5×10^{-5} Torr. The static mode switching (DC test) is tested for the 100 μm-sized $Ge_1Se_1Te_2$ PRAM device. In the first sweep, the amorphous $Ge_1Se_1Te_2$ thin film showed a high resistance state at low voltage region. However, when it reached to the threshold voltage, V_{th}, the electrical resistance of device was drastically reduced through the formation of an electrically conducting path. The pulsed mode switching of the 20 μm-sized $Ge_1Se_1Te_2$ PRAM device showed that the reset of device was done with a 80 ns-8.6 V pulse and the set of device was done with a 200 ns-4.3 V pulse.

Keywords : $Ge_1Se_1Te_2$, Nonvolatile, Phase change memory, Amorphous semiconductor

1. INTRODUCTION

Amorphous chalcogenide thin films have attracted much attention as a new advanced and replaceable technology material because of their interesting electrical, optical and thermal properties including resistance and reflectance change[1,2]. Especially, phase change nonvolatile memory is emerging as one of the candidate for the next generation of memory devices on amorphous chalcogenide thin film. The PRAM utilizes the reversible phase change phenomena between crystalline and amorphous states of chalcogenide materials by electrical resistive joule heating. The resistance of the crystalline phase(SET) is much lower than that of the amorphous phase(RESET). This resistance difference between the two states is known as more than three orders of magnitude, which provides a sufficient data sensing margin for the memory operation[3].

Improvements in phase-change materials technology subsequently paved the way for the development of rewritable CD and DVD optical memory media[4]. These advances, coming along with significant technology scaling and better understanding of the fundamental electrical device operation, have motivated the development of chalcogenide based memory technology at the present day technology node[5,6]. PRAM is nonvolatile devices which use a small volume of chalcogenide alloy material to be converted between low-resistance poly-crystalline and high resistance amorphous structural phases by resistive heating with programming current pulses[7]. Key advantages of PRAM nonvolatile technology are: write/read performance, endurance, low programming energy, process simplicity, cost, and CMOS embeddability.

The write/read performance of PRAM is comparable to that of DRAM[8]. It has been widely studied for the optical memory[9], which Te based chalcogenide material is easily to be vitreous by high speed quenching. It is well known that this material could not be easily converted a polycrystalline state. This state is not stable and slowly converts to polycrystalline state. Therefore the research on the crystallization speed for decreasing rewrite speed has been actively progressed.

The Ge-Sb-Te system, which is one of the chalcogenide materials, has been studied for phase-change random access memory, because of its fast crystallization and good data storage lifetime characteristics. We have studied Se doped phase change materials. In the present work, the memory device composed of the $Ge_1Se_1Te_2$ was fabricated and their characteristics were studied.

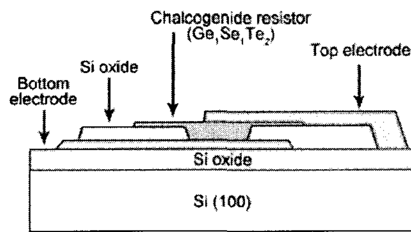


Fig. 1. Schematic cross-sectional view of PRAM test device.

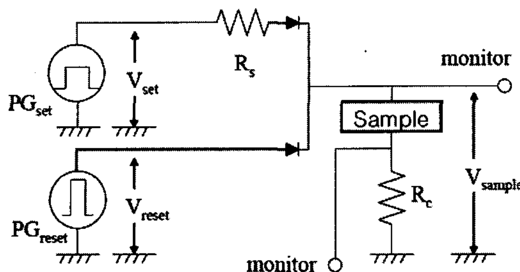


Fig. 2. Circuit view for measuring electrical characteristics of phase change memory.

2. EXPERIMENT

$Ge_1Se_1Te_2$ bulk was prepared by a conventional melt quenching technique. The constituent elements weighed in the appropriate ratio were sealed in evacuated quartz ampoules. Then, these were placed in a furnace and heated[10,11]. The ampoules were constantly stirred every 30 min to achieve the complete homogenization of the constituents in the melt and quenched successively in ice water after air. The 150 nm-thick Al electrode and Si oxide were deposited on a Si single-crystal wafer with (100) orientation by DC and RF sputtering. Films of amorphous $Ge_1Se_1Te_2$ were prepared by thermal evaporation of the bulk at a deposition rate of about 0.5 nm/s kept in vacuum at $\sim 2\times10^{-5}$ Torr. Film thickness was monitored and held constant at approximately 100 nm. The amorphous nature of the samples was confirmed by absence of any sharp peak in the X-ray diffraction pattern and differential scanning calorimetry. Schematic cross-sectional view of PRAM device is shown in Fig. 1. Phase change material is completely encapsulated by Si oxide and material electrode layer. Furthermore, heating is only done for few tens of nanoseconds. Thus, the transition of phase-change material is done under far from the thermodynamic equilibrium condition. Possibly, the crystalline structure of $Ge_1Se_1Te_2$ -phase-change film is not a pure single phase. However, it can be regarded as a homogenous material.

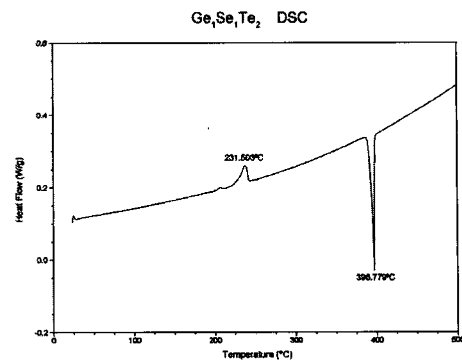


Fig. 3. DSC analysis curve with $Ge_1Se_1Te_2$ bulk.

We measured the electrical resistance change with the fabricated device by applying pulse (SET and RESET) on $Ge_1Se_1Te_2$ film. We made a circuit as Fig. 2. to measure each resistance change. A pulse on circuit was generated by pulse/function generator (HP8116A).

3. RESULTS AND DISCUSSION

Figure 3 shows a result of thermal characteristic of $Ge_1Se_1Te_2$ by DSC. As seen from the Fig. 3, the crystallization temperature was about 231.503 °C and the eutectic temperature is about 396.779 °C.

The change of thermal resistance of $Ge_1Se_1Te_2$ thin film, which were heat-treated at various temperature ranging from 0 °C to 300 °C for 10 min are shown in Fig 4. The resistance of $Ge_1Se_1Te_2$ thin film was very high. However, it was drastically decreased with annealing.

During annealing at higher temperature, both nucleation and growth rate of crystalline phase in enhanced. Therefore, the thermal resistance of the $Ge_1Se_1Te_2$ was reduced by a factor of up to 10^5 times along with crystallization. This result implies that $Ge_1Se_1Te_2$ might have an advantage in the multi-bit per cell operation of PRAM, due to its wider variation in thermal resistivity associated with crystallization, than the conventional $Ge_2Sb_2Te_5$ material.

The static mode switching of the 100 μm-sized PRAM test device is shown in Fig. 5. At low voltage, two different resistances are observed, depending on the crystalline state of the phase-change resistor. In the first sweep, the as-deposited amorphous $Ge_1Se_1Te_2$ showed very high resistance. However, when it reached the threshold voltage, the electrical resistance of device was drastically reduced through the formation of an electrically conducting path. This conducting path can be either the connected crystalline domains, the electrically conducting secondary phase along grain boundaries or the linked crystalline defects. After the formation of an

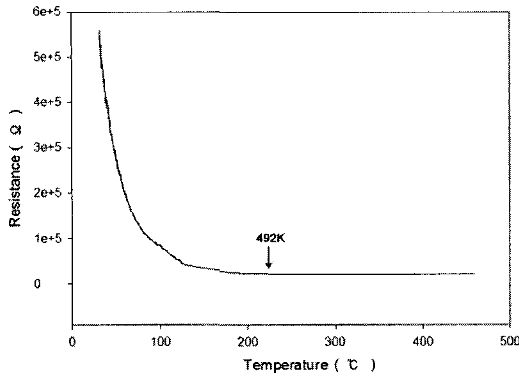


Fig. 4. Resistance of $Ge_1Se_1Te_2$ heated-treated under various temperature ranging from 0 ℃ to 300 ℃ for 10 min.

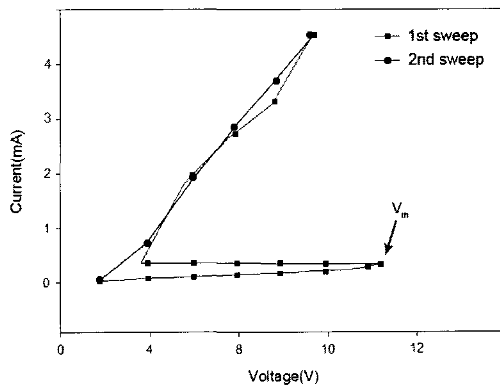


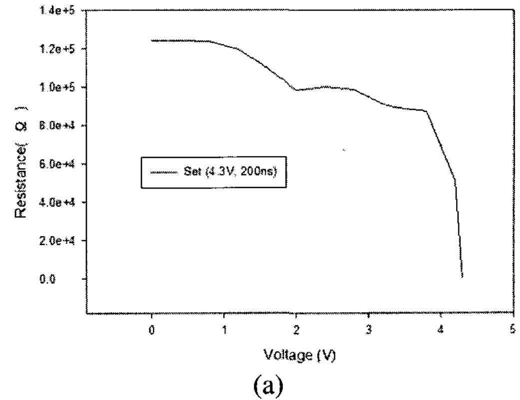
Fig. 5. Static mode I-V characteristics of $Ge_1Se_1Te_2$ PRAM device.

electrically conducting path, most of the current flows through the conducting path, and it begins to generate the heat as the current increases. Since the crystallization process is carried out with nucleation and growth steps, the amorphous-state phase-change material around the conducting path is then heated and crystallized.

Finally, a phase transition from an amorphous state to a crystalline state was completed, when the current was increased. Therefore, when the current was increased, the same resistance was observed, regardless of the crystalline state of the phase-change resistor.

This resistance is the so-called dynamic resistance. To increase the writing power and reduce the writing current, the dynamic resistance needs to be increased and this can be accomplished by simultaneously reducing with the interfacial area between the phase-change resistor and the electrode.

The pulsed mode switching characteristic of the 20 μm-sized PRAM test device was measured. For an amorphized phase-change device, 200 ns long pulse was



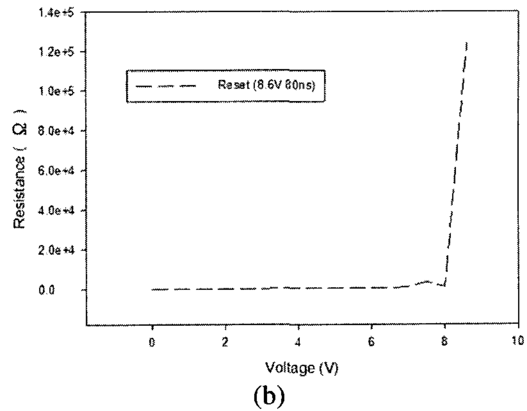


Fig. 6. Pulsed mode switching characteristics of $Ge_1Se_1Te_2$ PRAM device (a) Set mode(200 ns, 8.6 V) and (b) Reset mode(80 ns, 4.3 V).

applied. For low voltage (V < 4.0 V) pulses, an amorphized region of phase change device was not crystallized. Since the crystallization is governed by nucleation and growth step, if sufficiently long pulse is applied, the amorphized region of phase-change resistor can be crystallized at low voltage. For high voltage (V > 4.3 V) pulses, amorphized region is crystallized and electrical resistance was changed at low state.

Then, 80 ns short-pulse was applied. For low voltage (V < 8.0 V) pulses, phase-change resistor was not heated up to its melting temperature and no transition was observed. However, for sufficiently high voltage (V > 8.5 V) pulses, phase-change resistor was heated above its melting temperature. Since the pulse width was only 80ns, phase-change resistor was just melted and quenched. Thus, amorphization was occurred, and the electrical resistance was set to high resistance. Once transition is occurred, 80 ns short-pulse cannot supply sufficient energy for crystallization, since the electric resistance of amorphous resistor is too high (energy is proportional to voltage2xtime/resistance). The result of the pulsed mode switching of the PRAM device is shown in Fig. 6.

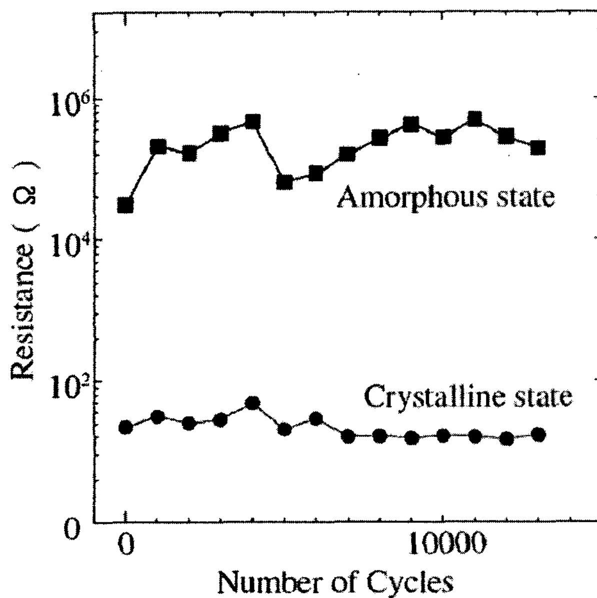


Fig. 7. Resistance change of the memory cell caused by the application of the set and reset pulses.

Figure 7 shows one of the results of the resistance changes of the memory cell of $Ge_1Se_1Te_2$ caused by the application of set and reset pulses. The average resistance of the crystalline (R_{cry}) and amorphous states (R_{amo}) were approximately 48 Ω and 124 KΩ, respectively. The ratio of R_{amo} to R_{cry} was (R_{amo}/R_{cry} =) 2.5×10^3. The ratio is sufficiently large for application to the memory devices.

4. CONCLUSION

One of the most important problems for PRAM is a large current which is required for write/erase operation. Particularly, the current for the reset operation is large, because the memory cell must be heated to a temperature higher than T_m in this operation. The write pulse (set operation) was determined the device operation speed. The use of chalcogenide glass with low T_m and just like lithography is the answers to the above problem.

In this paper, we fabricated and tested $Ge_1Se_1Te_2$ chalcogenide thin film based PRAM device. The device was successfully switched between amorphous and crystalline states by using a 80 ns–8.6 V pulse for resetting and a 200 ns–4.3 V pulse for setting and exhibited a switching dynamic range (ratio of R_{high} to R_{low}) as high as 10^3. As mentioned above, it will be possible that the phase-change of chalcogenide thin film by electrical pulse is the element of PRAM application.

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