SiGe pMOSFET의 전기적 특성 분석

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Analysis of electrical characteristics for p-type silicon germanium metal-oxide semiconductor field-effect transistors

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요 약

본 논문에서는 게이트길이가 0.9㎛, 0.1㎛를 갖는 p형 SiGe MOSFET에 대한 전기적 특성들을 TCAD 시뮬레이터를 이용하여 연구하였다. 또한 온도 300K와 77K일 때 2개의 캐리어 전송모델(하이드로 다이나믹 모델과 드리프트-확산 모델)을 사용하여 전기적 특성들을 비교 분석하였다. 본 논문에서는 드리프트-확산 모델보다는 하이드로 다이나믹 모델을 사용하였을 때 드레인 전류가 더 많이 흐름을 알 수 있었다. 게이트 길이가 0.9㎛일 때 문턱 전압은 온도가 300K, 77K에서 각각 -0.97V와 -1.15V의 값을 가짐을 알 수 있었다. 또한 게이트 길이가 0.1㎛일 때 문턱전압들은 게이트길이가 0.9㎛일 때의 값과 거의 같음을 알 수 있었다.

ABSTRACT

In this paper, we have designed the p-type metal-oxide semiconductor field-effect transistor(pMOSFET) for SiGe devices with gate lengths of 0.9㎛ and 0.1㎛using the TCAD simulators. The electrical characteristics of devices have been investigated over the temperatures of 300 and 77K. We have used the two carrier transfer models(hydrodynamic model and drift-diffusion model). We know that the drain current is higher in the hydrodynamic model than the drift-diffusion model. When the gate length is 0.9㎛, the threshold voltage shows -0.97V and -1.15V for 300K and 77K, respectively. The threshold voltage is, however, nearly same at 0.1㎛ for 300K and 77K.

키워드

pMOSFET, TCAD, hydrodynamic model, drift-diffusion model, threshold voltage

Ⅰ. INTRODUCTION

Over the last decade, many researchers have been developing high speed operation devices such as heterojunction bipolar transistors(HBTs) and modulation doped field effect transistors(MODFETs) for the wireless communication systems[1-2].

SiGe semiconductor has not yet been put to practical use, but it has based on silicon semiconductor. Since the SiGe semiconductor have been very excellent high speed operating characteristics and a low electric power characteristic with a high current gain in a low current, it can produce a low price ICs for a light communication and RFICs for a high frequency communication over several GHz range. A highly applied region of compound semiconductor is substituted for SiGe semiconductor instead of GaAs, and it will present possible system on a chip from general CMOS logic devices to high frequency devices since SiGe is based on silicon[3-5].

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In this paper, therefore, we have designed Si1-xGex pMOSFETs using TCAD simulators and investigated the electrical characteristics, in which the channel lengths are 0.9 ㎛ and 0.1㎛. In this time, we have applied the two models(hydrodynamic model and drift-diffusion model) for the simulation of carrier transport in devices. Also, we have compared with 300K and 77K.

Ⅱ. DESIGN AND CONDITION

We have designed p-type $Si_{0.8}Ge_{0.2}$ MOSFETs using the TCAD simulators. The channel lengths are 0.9㎛ and 0.1㎛, respectively. Figure 1 shows the schematic of designed p-type $Si_{0.8}Ge_{0.2}$ MOSFET.

In this paper, the devices have been designed in an ultra-high vacuum(UHV) compatible chemical vapor deposition(CVD) system using SiH_4 and GeH_4 gases in a H_2 carrier.

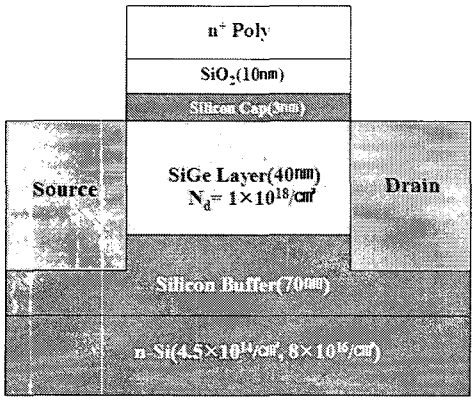

Figure 1. The schematic of the p-type SiGe MOSFET

The substrate is n-type (100) silicon wafer. When the channel length is 0.9㎛ and 0.1㎛, the substrate is doped with $4.5\times10^{14}/cm^3$ and $8\times10^{16}/cm^3$, respectively. The device structure consisted of an epitaxial Si buffer layer of 70nm, $Si_{0.8}Ge_{0.2}$layer of 40nm and 3nm undoped Si cap layer. Next, ultrathin gate oxide is grown on the Si cap layer. Since the electrical quality of this oxide and its inerface with the Si cap layer is paramountly important to the operation of the MOSFETs, dry oxidation is used for this step. It is common to incorporate some nitrogen at the Si-SiO_2interface, forming oxy-nitrides in which improve the interface quality in terms of hot electron effects. When the channel length is 0.9㎛ and 0.1 ㎛, the oxide layers are implanted with 50eV, $1\times10^{13}/cm^2$ and 100keV, $2\times10^{14}/cm^2$, respectively. Also, to reduce the strain relaxation in metastable $Si_{0.8}Ge_{0.2}$ layers, rapid thermal oxidation(RTO) at 950℃for 30s in oxygen ambient is used to form thegate oxide layer. After the oxidation, the poly gate layer is doped very heavily all the way to the poly-oxide interface in order to make it behave electrically like a metal electrode. Heavy doping of the gate material is very important, because otherwise a depletion layer can be formed in the poly gate.

We use the DIOS tool of TCAD simulators for simulation. Table 1 shows the conditions of simulation.

Table 1. The design conditions of p-type SiGe MOSFET for simulation

Channel length(㎛)	0.9	0.1
Substrate concentration	$4.5\times10^{14}/cm^3$	$8\times10^{16}/cm^3$
Silicon Buffer(nm)	70	
SiGe Layer(nm)	40	
Oxide thickness(nm)	10	
Silicon Cap(nm)	3	
Source/Drain doping concentration	$2\times10^{15}/cm^2$, 20keV	$5\times10^{15}/cm^2$, 10keV

When the channel length is reduced, we have not applied the scaling theory, since the balance of doping concentration problem is happened in simulation.

We, therefore, have empirically determined process conditions. For ideal scaling, power supply voltages should be reduced to keep the internal electric fields. But, in practice, power supply voltages are not scaled hand-in-hand with the device dimensions, partly because of other system-related constraints. The longitudinal electric fields in the pinch-off region, and the transverse electric fields across the gate oxide, increase with MOSFET scaling.

A variety of problems then arise which are generically known as hot electron effects and short channel effects. To solve theses problems, we found the most suitable conditions

of simulation(doping concentration, annealing time and temperature etc.).

Ⅲ. RESULTS AND DISCUSSION BASED ON THEORETICAL BACKGROUND

Figure 2 shows the drain current(I_D)-drain voltage(V_D) curve for demonstrating the superiority of designed device. When the channel length(L_{ch}) is 0.9㎛, the drain voltage is biased from 0 to -1.5V, and the gate voltage(V_G) is biased from -1.0 to -2.0V.

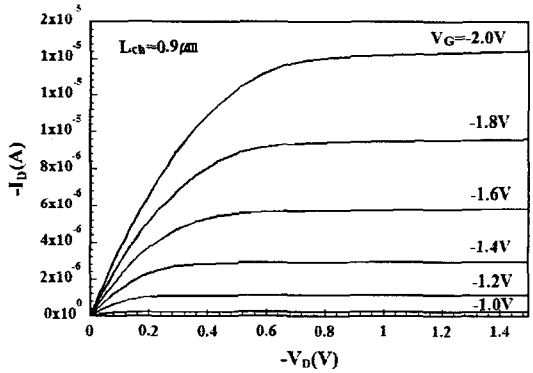

Figure 2. I_D-V_D output characteristics of $Si_{0.8}Ge_{0.2}$ pMOSFET at gate biases from -1.0V to -2.0V and L_{ch}=0.9㎛

The effect of a negative gate bias $-V_G$ is to increase the resistance of the channel and induce pinch-off at a lower value of current. Since the depletion regions are larger with negative V_G, the effective channel width is smaller and its resistance is higher in the low current range.

The slope of the I_D vs. V_D curves below pinch-off become more steep when the gate voltage is more negatively. The pinch-off condition is reached at a lower drain voltage, and the saturation current is lower than for the case of V_G=-2V. Therefore, we know that our device model is proper for I_D-V_D output characteristics of $Si_{0.8}Ge_{0.2}$ pMOSFET. For the simulation of carrier transport, we have used two models. One is the drift diffusion model. The drift diffusion model is widely used for the simulation of carrier transport in semiconductors and defined by the formulated set of basic semiconductor equation, where current densities for the holes are given by:

$$\overrightarrow{J_n} = -nq\mu_n \nabla \phi_n$$
$$\overrightarrow{J_p} = -pq\mu_p \nabla \phi_p \quad (1)$$

here μ_n, μ_p is the electron and hole mobilities, and $\varnothing_n$, $\varnothing_p$ is the electron and hole quasi-Fermi potentials. Another model is the hydrodynamic model given by:

$$\overrightarrow{J_n} = \mu_n (n\nabla E_C + k_B T_n \nabla_n + f_n^{id} k_B n \nabla T_n - 1.5 n k_B T_n \nabla \ln m_e)$$
$$\overrightarrow{J_p} = \mu_p (p\nabla E_V + k_B T_p \nabla_p + f_p^{id} k_B p \nabla T_p - 1.5 p k_B T_p \nabla \ln m_h) \quad (2)$$

here E_C and E_V are the conduction and valance band energies, i.e. the first term takes into account the contribution due to the spatial variations of electrostatics potential, electron affinity, and the band gap. The three remaining terms in the equations take into account the contribution due to the gradient of concentration, due to the carrier temperature gradients and due to the spatial variation of the effective messes m_e and m_h. In doped semiconductors, scattering of the carriers by charged impurity ions leads to degradation of the carrier mobility.

In this paper, therefore, we have used the Masetti model for doping dependent mobility degradation:

$$\mu_{dop} = \mu_{min1} \exp\left(\frac{P_c}{N_i}\right) + \frac{\mu_{const} - \mu_{min2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_1}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}} \quad (3)$$

here N_i=N_D+N_A denotes the total concentration of ionized impurities. And μ_{const} is determined by the constant mobility model.

In the channel region of a MOSFET the high transverse electric field forces the carriers to interact strongly with the semiconductor-insulator interface. The carriers are subjected to scattering by acoustic surface phonons as well as scattering due to surface roughness. The mobility degradation due to these two effects is simulated by the Lombardi model:

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} \tag{4}$$

here μ_b is the bulk mobility according to Mathiessen's rule. And the surface contribution due to acoustic phonon scattering has the form:

$$\mu_{ac} = \frac{B}{F_\perp} + \frac{C(N_i/N_0)^\lambda}{F_\perp^{1/3}(T/T_0)^k} \tag{5}$$

and the contribution attributed to surface roughness is given by:

$$\mu_{sr} = \frac{B}{F_\perp} + \left(\frac{(F_\perp/F_{ref})^{A^*}}{\delta} + \frac{F_\perp^3}{\eta} \right)^{-1} \tag{6}$$

In equation (6), the reference field F_{ref} is 1V/cm and A^* is equal to 2.

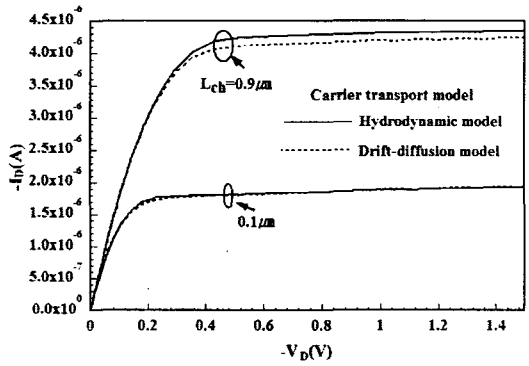

Figure 3. The I_D-V_D characteristics for two models at L_{ch}=0.9㎛ and 0.1㎛, respectively

Figure 3 shows the I_D-V_D characteristics for two models at L_{ch}=0.9㎛ and 0.1㎛, respectively.

We know that the hydrodynamic model drives higher drain currents than drift-diffusion model. But, when the channel length is 0.1㎛, the drain current is nearly both same. Although the channel length is reduced, we have found the excellent electrical characteristics in our device model. We have investigated the operating characteristics in temperatures.

Figure 4 shows the I_D-V_D characteristics for temperature, at 300K and 77K, respectively.

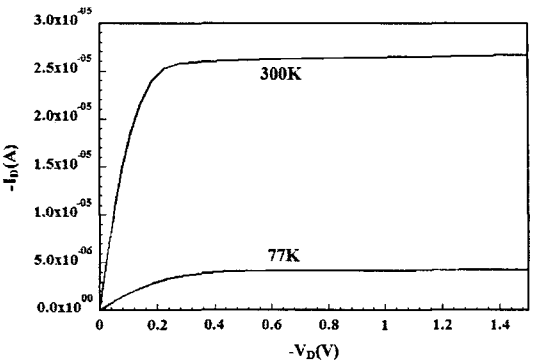

Figure 4. The I_D-V_D characteristics for the temperatures at L_{ch}=0.9㎛

Along to decrease of the temperature, the drain current is decreasing. That is, the electron-hole pairs(EHP) are difficult to be generated in a low temperature. But, although the temperature is low, we have obtained good I_D-V_D characteristics in our devices. In this paper, we have investigated the threshold voltages. Figure 5 shows the threshold voltage characteristics when the channel length is 0.9 ㎛ and 0.1㎛. When V_D is biased to -1.5V and the channel length is 0.9㎛, the threshold voltage is -0.97V at 300K. But, we have obtained the threshold voltage of -1.15V at 77K. Because the threshold voltage is high in a low temperature, we have used high doping concentration. The most valuable tool for controlling threshold voltage is ion implantation. Since very precise quantities of impurity can be introduced by this method, it is possible to maintain close control of threshold voltage. In this paper, therefore, the boron is implanted through the gate oxide of a device with $1\times10^{18}/cm^2$.

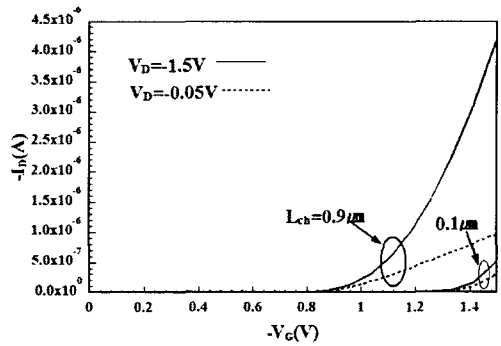

Figure 5. The threshold voltage characteristic when L_{ch} is 0.9㎛, 0.1㎛

Also, when the channel length is 0.1㎛, the threshold voltage is -1.4V and -1.42V at 300K and 77K, respectively. Along the channel length is reduced, the threshold voltage is increased.

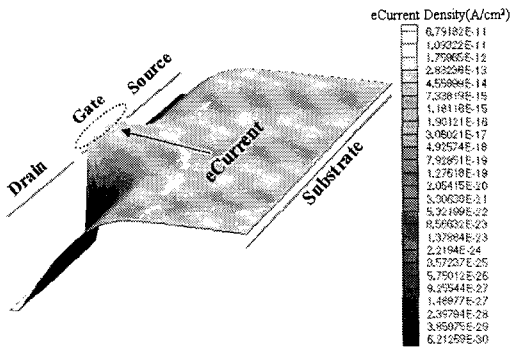

Figure 6. The distribution of hole density for SiGe pMOSFET when both gate and drain voltage is -1.5V at L_{ch}=0.9㎛

Figure 6 shows the distribution of hole density when the channel length of SiGe pMOSFET is 0.9㎛. And we enlarge a near drain to show the channel formation. Much hole density is formatted in channel as shown in Fig. 6. For this simulation, we have used the Tech-plot simulator one of the TCAD simulators.

Ⅳ. CONCLUSIONS

We have investigated p-type $Si_{0.8}Ge_{0.2}$ MOSFETs using the TCAD simulators. We have investigated the electrical characteristics when the channel lengths are 0.9㎛ and 0.1㎛, and the temperatures are 300K and 77K, respectively. For the investigation of the carrier transport characteristics, we have used the drift-diffusion model and hydrodynamic model.

Resultly, although the channel length is decreased to 0.1㎛, p-type $Si_{0.8}Ge_{0.2}$MOSFETs shows very excellent electrical characteristics. The hydrodynamic model drives the higher drain current than drift-diffusion model.

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