Effects of Thermal Treatment on the Characteristics of Spiral Inductors on Bragg Reflectors

Linh Mai*, Jae-young Lee, Minh-Tuan Le, Van-Su Pham and Giwan Yoon

Abstract—This paper presents the thermal technique to improve characteristic of planar spiral inductors. The spiral inductors were fabricated on silicon dioxide/silicon (SiO2/Si) wafer. The thermal treatment was done by annealing processes. The measure results showed a considerable improvement of return loss (S11). This thermal treatment seems very promising for enhancing spiral inductors based RF IC's.

Index Terms—On-chip inductor, Post-annealing, Return loss (S11)

I. INTRODUCTION

Nowadays, as the demands for radio frequency integrated circuits (RF IC's) continue to expand, the need for high performance characteristics of on-chip spiral inductors has become more important. Typical applications of the on-chip spiral inductors include low loss inductor for input matching of low noise amplifiers, inductively loaded pre-amplifiers, output matching networks for high efficiency power amplifiers, and high-Q tank circuits for low phase noise voltage control oscillators. Recently, many research activities have been focused on the design, model and optimization of spiral inductors on silicon substrate.

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Conventionally, on-chip inductors have been fabricated on the planar substrates such as silicon or glass [1-3]. Spiral inductors are commonly designed by placing metal in a planar spiral configuration. The two ends of the spiral are the terminals of the inductor. The losses caused by conductive substrates and metal strips are main drawback in improving the performance of those planar inductors. In order to improve the performance of on-chip spiral inductors, many methods have been used to decrease the substrate losses and ohmic loss. With the advances in the multi-layer metal interconnection process, inductors can be fabricated with acceptable quality by utilizing advances in process technology such as higher conductivity metal layers to reduce the loss resistance of the inductor [4], multi-metal layers to increase the effective thickness of the spiral inductor for reducing loss. Zu et al. [5] employed low loss substrates to reduce losses in the substrate at high frequency. Chang et al. [6] used thick oxide, or suspended inductors, to isolate the inductor from the lossy substrate. However, the high Q-value of on-chip inductors achieved by those conventional/uncoventional methods suffers from the cost of complex process and different technology or, together with decreasing the mechanical strength. Thus, they seem somewhat not easy for fabrication and commercialization.

In this paper, we present a study on the thermal treatment effects on the performance of the on-chip spiral inductors on silicon substrate.

II. EXPERIMENT

A range of inductors with varying sizes and shape s were fabricated on a SiO2/Si wafer by a MEMS t echnique.

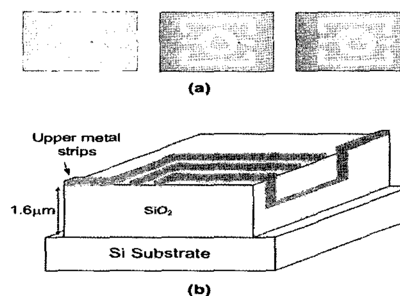

Fig. 1 (a) 8 sides, 12 sides and circular layout top-view inductor.
(b) Cross-sectional view of inductor fabricated on SiO2/Si wafer

These on-chip inductor geometry variations included variations in metal width, spaces, and number of turns. Square, circular, and multi-side spiral inductors were included on the SiO2/Si substrate. Several layouts and cross-sectional representation of typical planar on-chip inductors are shown in Fig. 1.

All the spiral inductors were made of aluminum (Al) and were separated from 4 inches Si wafer by 0.6μm silicon dioxide (SiO2). The structure of spiral inductors consists of a dielectric thin film SiO2 layer 1.0μm thick placed between top and bottom metal strips. Firstly, one SiO2 layer 0.6μm was deposited onto Si wafer by P5000 II TEOS Depo. machine. Secondly, a bottom metal (Al) layer with 1.0μm thick was deposited on the SiO2/Si wafer by Sputter Wavics machine. Thirdly, a dielectric material-SiO2 layer 1.0μm thick was covered with on the bottom metal layer. Lastly, the top-metal (Al) layer was coated with on the dielectric layer. The shapes of every inductor (top metal strip and underpass strip) were formed by using dry-etching technique (MEMS Metal Etcher equipment). The via-holes used for connection between top metal strip and underpass strip of inductor were dry-etched by P5000 II Etcher machine. All these MEMS processes were carried-out in Inter-University Semiconductor Research Center, Seoul National University. Finally, the spiral inductors on SiO2/Si substrate were obtained.

In order to investigate the thermal treatment effects, the spiral inductors were firstly measured to extract the de-embedded S-parameters (called M1). Then, these inductors were post-annealed in Ar gas ambient in an Electric Dehydrate Furnace (EDF) equipment at 2000C for 60 minutes and 4000C for 60 minutes. Right after each post-annealing time, all spiral inductors were measured to get S-parameters and called M2 & M3, respectively. The S-parameters measurements were done by Probe Station and Network Analyzer Hewlet Packard/HP 8722D.

III. RESULT AND DISCUTION

Fig. 2 shows the three types of spiral inductor layouts (as mentioned in Fig. 1, section 2) and their return loss S11 characteristics versus frequency for various post-annealing conditions.

All of the spiral patterns have 2.5 turns. There are two inductors with the number of sides 8 and 12, respectively. The last one has circular layout pattern. Fig. 2 (a), (b), (c) compare the return loss characteristics M1, M2, and M3 of the three spiral inductors with the same inductor layout, but different thermal conditions, respectively. The comparison of the S11 values clearly shows the relative effect of the thermal treatments. The S11 values for the three inductor layout patterns have the same increasing trend from the values of non-annealing M1, values of post-annealing 2000C/60min M2, and post-annealing 4000C/60min M3.

For the post-annealing treatments, the S11 characteristic of M2 curve is better than of M1 curve. And the return loss S11 value in the curve M3 is also better than M1 curve, but not much different when comparing between M2 and M3 curves. The return loss S11 value seems to be significantly improved since the inductors were post-annealed in Ar gas ambient. Certainly, thermal annealing can be one of important factors to enhance the return loss characteristics.

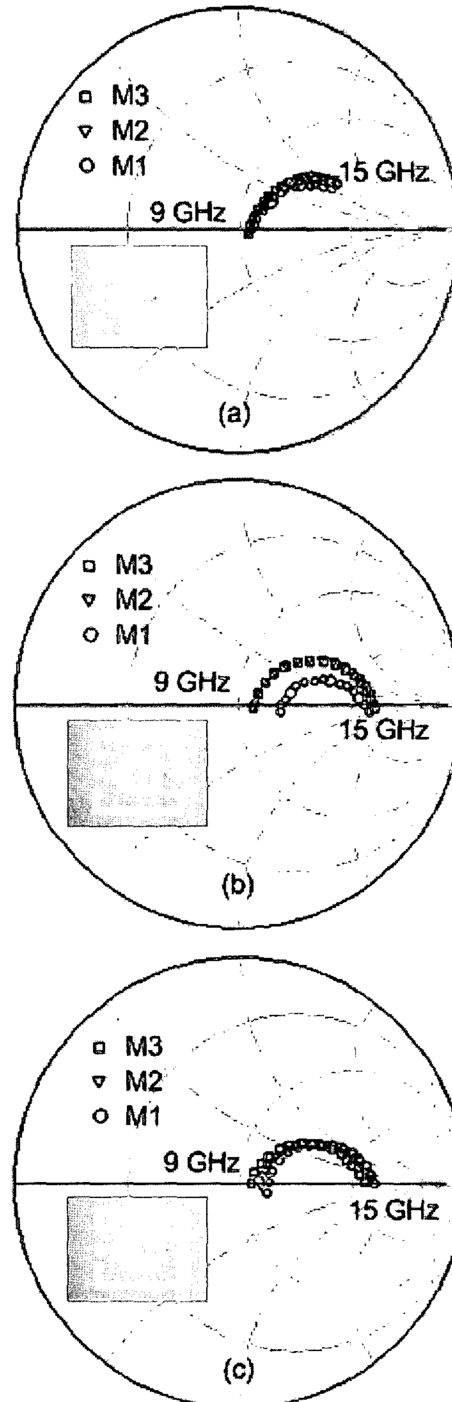

Fig. 2 Return loss characteristics versus frequency for various thermal conditions. (a) Case of 8 side inductor (b) Case of 12-side inductor (c)Case of circular inductor

Inside the original inductor structure-metal layers, SiO2 layer- may exist some physical imperfections in the

thin film microstructures. Beside these imperfections, there are imperfection adhesions at interfaces between the physically deposited films; the poor connection between top metal strip and bottom metal underpass through via-holes of each inductor. All of these imperfect problems made the spiral inductor performance degraded. Owning to use of the post-annealing process, the incomplete effects are believed somewhat to be reduced. This eventually leads to the improvement of inductor performances. From the measured S-parameters, these inductors can be used in the high frequency range from 9 GHz - 15 GHz.

Although further investigations need to be carried-out for more clear understanding, we strongly believe at this point that the use of post-annealing can improve the on-chip inductor performance.

IV. CONCLUSION

A study of effects of thermal treatment on spiral inductors, fabricated on a SiO2/Si substrate by MEMS technique, was presented. A description of on-chip inductor test structure, experiment and measurement procedures was given. The impact of using thermal treatment processes was investigated and discussed. The characteristics of on-chip inductor are observed depend on the annealing conditions and can be improved by the thermal annealing particularly at 2000C/60min. The optimum of the various thermal treatments appears to improve the performance of spiral inductors based RF IC's.

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