

Dependence of Nanotopography Impact on Fumed Silica and Ceria Slurry Added with Surfactant for Shallow Trench Isolation Chemical Mechanical Polishing

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Abstract The purpose of this study is to investigate the difference of the wafer nanotopography impact on the oxide-film thickness variation between the STI CMP using ceria slurry and STI CMP using fumed silica slurry. The nanotopography impact on the oxide-film thickness variation after STI CMP using ceria slurry is 2.8 times higher than that after STI CMP using fumed silica slurry. It is attributed that the STI CMP using ceria slurry follows non-Prestonian polishing behavior while that using fumed silica slurry follows Prestonian polishing behavior.

Key words nanotopography, STI, CMP, slurry, Preston's law.

1. Introduction

Ceria slurry with an ionic surfactant is widely used in the STI CMP process because it can reduce nitride erosion and widen the processing margin by offering high oxide-to-nitride selectivity in the polishing removal rate.¹⁻⁷⁾ Nojo *et al.* reported³⁾ that adding a surfactant to ceria slurry can result in “self-stopping polishing”, as the relationship between the polishing pressure and the polishing rate shows a non-Prestonian, or non-linear, correlation.⁸⁾ In previous articles, we demonstrated that the nanotopography impact depends on the surfactant concentration and the abrasive size in ceria slurry.⁹⁻¹⁰⁾

A typical shallow trench structure used to isolate “active” regions where devices will be built. The nitride layer has been etched and a shallow trench etched into the silicon as shown in Fig. 1. An oxide film has then been deposited into the trench, which also results in overburden oxide above the nitride active areas. In the ideal STI CMP process in mass production, the oxide film is removed completely in all active regions, leaving oxide film only in the trench regions using fumed silica for first and second CMP and ceria slurry for third CMP. 300 nm-depth oxide film is polished off during first and second CMP, while 250 nm-depth oxide film is polished off during third CMP.

In this paper, we investigated the difference in the dependence of nanotopography impact on fumed silica or ceria slurry added with surfactant for STI CMP. In addition, we characterized the mechanism by which the CMP using fumed silica showed a different nanotopography impact from the CMP using ceria slurry.

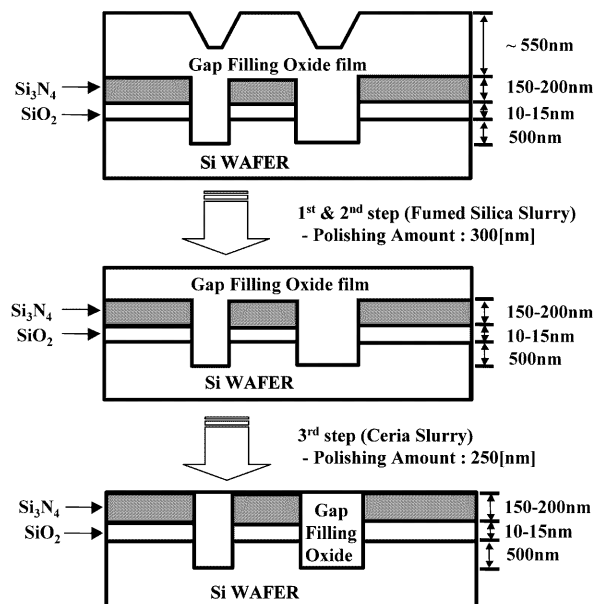


Fig. 1. Process flow of STI CMP proceeding three-step CMP; i.e., STI CMP 1, 2 and 3.

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2. Experiments

We used commercial 8 inch silicon wafers. Oxide films with a thickness of 7000 Å were deposited using the plasma-enhanced tetra-ethyl-ortho-silicate (PETEOS) method. The films deposited on wafers were polished on a Strasbaugh 6EC with a single polishing head and a polishing platen. We used an IC1000/Suba IV stacked pad (Rohm and Haas Co.). In addition, we used two kinds of slurries. One is fumed silica slurry (SS-12) from Cabot Co. and the other is ceria slurry (HS 8005HX) from Hitachi Co.. An anionic organic surfactant (water-soluble acrylic acid) of 0.8 wt% was optionally mixed with ceria slurry and deionized water (ceria slurry : surfactant : deionized water = 1 : 3 : 3 mixing ratio).

In our polisher, the actual polishing pressure was 4 psi (pounds per square inch), which is applied by an arm down-force, while a back pressure was not used. The rotation speeds of the head and the table were 70 rpm, and the relative velocity between the pad and wafer was 250 fpm (feet per minute). The slurry flow rate was 100 cm³/min. Break-in with a diamond dresser was carried out before each polishing. The oxide-film thickness before and after CMP was measured with a spectro-reflectometer, Nanospec 180 (Nanometrics) and a spectroscopic ellipsometer, ES4G (SOPRA). The nanotopography height of the wafer was measured with an optical interferometer, NanoMapper (ADE Phase Shift).

3. Results and Discussion

Fig. 2 shows an example of the nanotopography height (NH) map on the prepared wafers. The root-mean-square

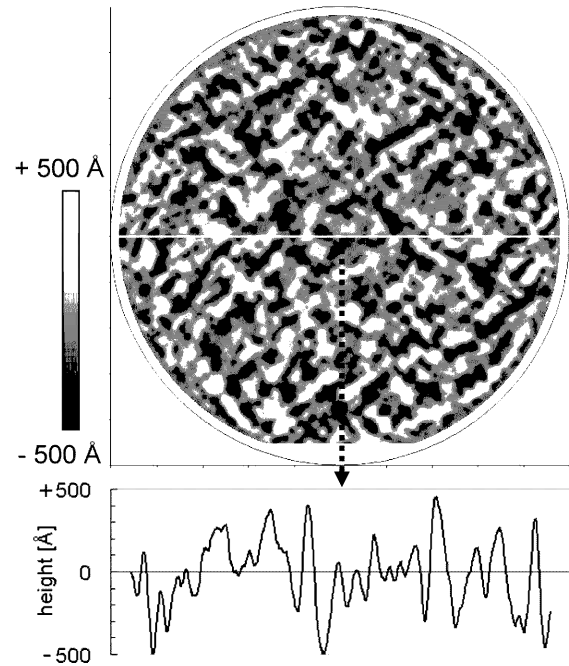


Fig. 2. An example of the nanotopography height map on the prepared wafers. The white line on the map corresponds to the path for the lateral profile measurement of the lower plot.

(rms) of the wafer nanotopography was 23.9 nm (see the lateral profile of wafer nanotopography in Fig. 2). We have confirmed that all wafers used for the experiment had similar characteristics and magnitude of nanotopography. First of all, we investigated the difference of the physical CMP behavior between fumed silica slurry and ceria slurry. Fig. 3 represents the dependency of polishing removal rate on the polishing down-pressure in the polisher.

It is well known that the polishing removal rate, RR , is generally proportional to the product of the polishing pressure, p , and the relative velocity between the wafer and

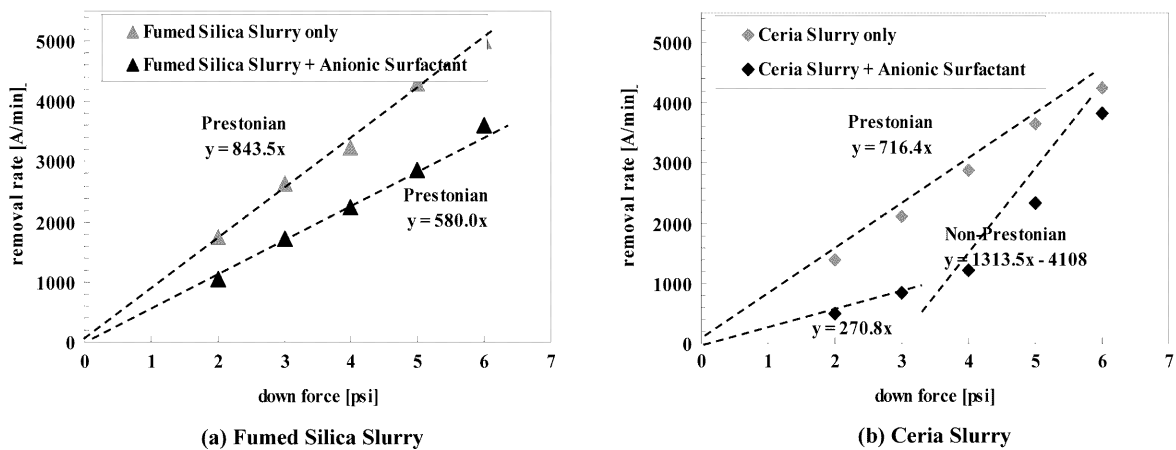


Fig. 3. Relationship between polishing removal rate and down force in the (a) fumed silica slurry and (b) ceria slurry.

pad, v , as given by this relation:⁸⁾

$$RR = k_p pv \tag{1}$$

where k_p is the Preston coefficient. The behavior modeled by this linear relationship between RR and p is called Prestonian. Both fumed slurries with or without the surfactant exhibit Prestonian behavior (see Fig. 3(a)). Otherwise, ceria slurry with an anionic surfactant clearly exhibits non-Prestonian behavior, which is consistent with the result reported by Nojo *et al*³⁾. This result indicates that the nanotopography impacts using ceria slurry will be different from that using fumed silica slurry after STI CMP.

Fig. 4 shows the simulated profiles of nanotopography and film thickness variations after consequent three-step CMP processes (fumed silica slurry + fumed silica slurry + ceria slurry). We used the simulator about the oxide-film thickness variation induced by wafer nanotopography.¹¹⁾ The removal amount from each of CMP process are 1500 Å, 1500 Å, and 2500 Å, respectively. According to our experimental result, Prestonian model has been used for STI CMP 1 and 2, while non-Prestonian model is used in the STI CMP 3 process. To see the correlation between wafer nanotopography and oxide-film thickness variation after STI CMP, the raw-profiles were filtered using a high-pass filter with a cutoff length of 20 nm. The peak and valley positions of the wafer nanotopography and oxide-film thickness variation are coincided well after each step of CMP. Thus, the variation in remaining oxide-film

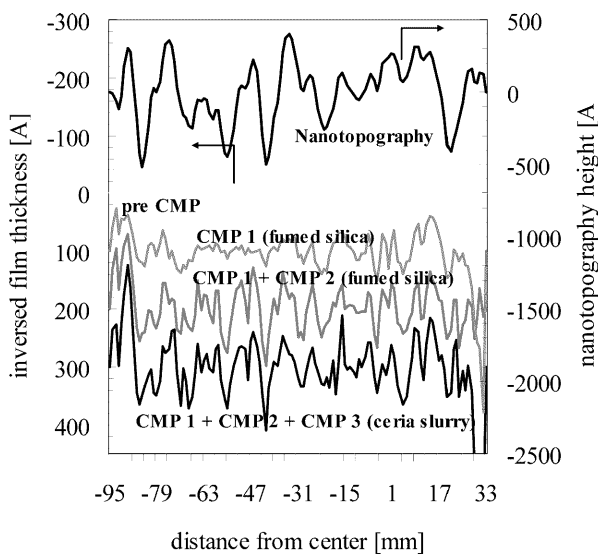


Fig. 4. Simulated profiles of nanotopography and remaining oxide-film thickness before/after CMP in STI process.

thickness after CMP is attributed to the wafer nanotopography. We confirmed that the magnitude of oxide-film thickness variation of STI CMP using ceria slurry is higher than after STI CMP using fumed silica slurry (see Fig. 4). This is attributed to the dependency of polishing removal rate on the slope of down-pressure in a polisher as shown in Fig. 3. The polishing removal-rate slope for the CMP using ceria slurry(non-Prestonian behavior), 1313.5, shows approximately 2.2 times higher than that using fumed silica slurry, 580.

Remind that the higher polishing removal-rate slope as a function of down pressure in a polisher leads to higher oxide-film thickness variation induced by the wafer nanotopography after STI CMP which is related to wear contact model.¹²⁻¹⁴⁾

Fig. 5 shows a correlation between root-mean-square (rms) value of wafer nanotopography and oxide-film thickness variation after each step of STI CMP as a function of the type of CMP slurry. The rms slope as a function of wafer nanotopography corresponds to how much the wafer nanotopography influences the rms of remaining oxide-film thickness; i.e., higher slope leads to more severe wafer nanotopography impact. The removal amount of CMP was 2000 Å. The rms slope for the CMP using ceria, 0.9664, is 2.8 times higher than that for the CMP using fumed silica slurry, 0.336. Thus, it is evident that the STI CMP using ceria slurry produces higher oxide-film thickness variation included by the wafer nanotopography than that using fumed silica slurry. Fig. 6 shows the rms of remaining oxide-film thickness after each step of STI CMP 1 and 2 using fumed silica slurry and STI CMP 3 using ceria slurry. The polishing removal amount

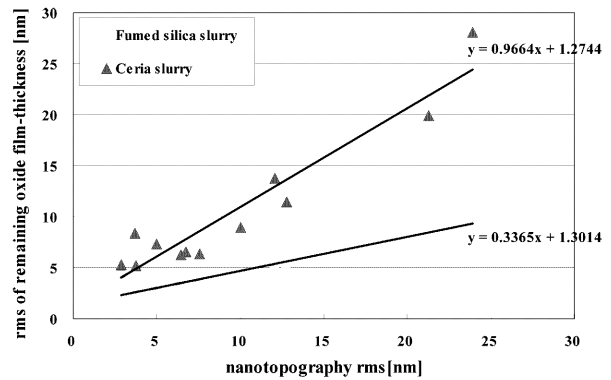


Fig. 5. Correlation between rms value of wafer nanotopography and oxide-film thickness variation after STI CMP for the two types of CMP slurries. The polishing removal amount was 2000 Å.

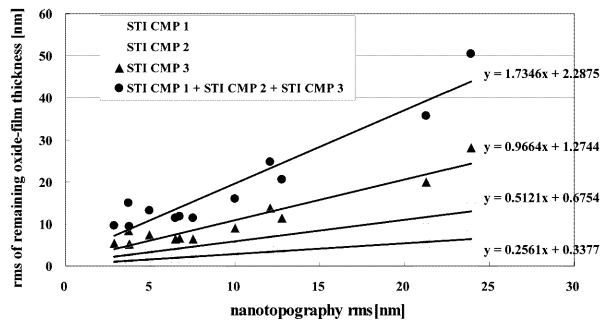


Fig. 6. Relationship between the rms of remaining oxide-film thickness variation and the wafer nanotopography after each step of STI CMP processes.

of STI CMP 1, 2 and 3 were 1500, 1500 and 2000 Å, respectively. The rms slope as a function of the wafer nanotopography for STI CMP 3 using ceria slurry is 1.9 times higher than STI CMP 1 & 2 using fumed silica slurry. Note that the rms slope for STI CMP 2 using fumed silica slurry is two times higher than that for STI CMP 1 using fumed silica slurry because the removal amount of STI CMP 2, 3000 Å was two times larger than that of STI CMP 1, 1500 Å. This result indicates clearly that the rms of remaining oxide-film thickness after STI CMP is mainly determined by the STI CMP using ceria slurry. Therefore, the minimum polishing removal amount using ceria slurry in STI CMP is necessary for obtaining lower remaining oxide-film thickness variation induced by the wafer nanotopography.

4. Conclusion

The wafer nanotopography influences the remaining oxide-film thickness variation after STI CMP; i.e., higher wafer nanotopography leads to higher remaining oxide-film thickness variation. Furthermore, the remaining oxide-film thickness variation induced by wafer nanotopography strongly depends on the type of the physical polishing behavior such as Prestonian or non-Prestonian polishing behavior. The physical polishing behavior is determined by the type of slurry in STI CMP. It was confirmed that the STI CMP using ceria slurry follows non-Prestonian polishing behavior while that using fumed silica slurry follows Prestonian polishing behavior. In addition, non-Prestonian polishing behavior produced higher remaining

oxide-film thickness variation induced by wafer nanotopography than Prestonian polishing behavior. Thus, the STI CMP using ceria slurry results in higher remaining oxide-film thickness variation induced by wafer nanotopography than the STI CMP using fumed silica.

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References

1. J.-G. Park, T. Katoh, H.-C. Yoo and J.-H. Park, *Jpn. J. Appl. Phys.*, **40**, L857 (2001).
2. J.-G. Park, T. Katoh, H.-C. Yoo, D.-H. Lee and U.-G. Paik, *Jpn. J. Appl. Phys.*, **41**, L 17 (2002).
3. H. Nojo, M. Kadera and R. Nakata, *Proc. IEEE idem*, San Francisco, CA, 1996 (The Institute of Electrical and Electronics Engineers, Piscataway, 1996) p. 349.
4. K. Hirai, H. Ohtsuki, T. Ashizawa and Y. Kurata, *Hitachi Chemical Tech. Report No.* **35**, 17 (2000).
5. Y. Tateyama, T. Hirano, T. Ono, N. Miyashita and T. Yoda, *Proc. Int. Symp. Chemical Mechanical Planarization IV*, Phoenix, 2000 (The Electrochemical Society, Pennington, 2000) p. 297.
6. Y. Homma, T. Furusawa, K. Kusukawa and M. Nagasawa, *Proc. CMP-MIC*, Santa Clara, CA, 1996 (Institute for Microelectronics Inter-Connection, Tampa, 1996) p. 67.
7. M. Miyajima, *Syosetsu Handoutai CMP Gijyutsu* (Details of Semiconductor CMP Technology) ed. T. Doi, (Kogyochosakai, 2000, Tokyo) p. 249 [in Japanese].
8. F. W. Preston, *J. Soc. Glass Tech.*, **11**, 247 (1927).
9. T. Katoh, S. J. Kim, U. Paik and J. G. Park, *Jpn. J. Appl. Phys.*, **42**, 5430 (2003).
10. H. G. Kang, T. Katoh, U. Paik and J. G. Park, *Jpn. J. Appl. Phys.*, **43**, L1 (2004).
11. T. Katoh, M. S. Kim, Ungyu Paik, J. G. Park, *Jpn. J. Appl. Phys.*, **43**, L217 (2002).
12. B. Lee, Ph.D Thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Massachusetts, 2002.
13. D. Boning and B. Lee, *Materials Research Society Bulletin*, **27**, 761 (2002).
14. O. G. Chekina and L. M. Keer, *J. Electrochem. Soc.*, **145**, 2100 (1998).