Unified Power Quality Conditioner for Compensating Voltage Interruption

Byung-Moon Han†, Bo-Hyung Cho*, Seung-Ki Sul* and Jae-Eon Kim**

Abstract - This paper proposes a new configuration for the Unified Power Quality Conditioner, which has a DC/DC converter with super-capacitors for energy storage. The proposed UPQC can compensate the reactive power, harmonic current, voltage sag and swell, voltage imbalance, and voltage interruption. The performance of the proposed system was analyzed through simulations with PSCAD/EMTDC software. The feasibility of system implementation is confirmed through experimental works with a prototype. The proposed UPQC has ultimate capability to improve the power quality at the point of installation on power distribution systems and industrial power systems.

Keywords: DC/DC Converter, PSCAD/EMTDC (Power System Computer Aided Design/Electro Magnetic Transients DC analysis program), Super-capacitor bank, UPQC (Unified Power Quality Conditioner), Voltage interruption

1. Introduction

As more sensitive loads, such as computers, automation equipments, communication equipments, medical equipments, and military equipments, have come into wide use, power quality has become a significant issue to both customers and the utility companies. Since these equipments are very sensitive in relation to input voltage disturbances, the inadequate operation or the fault of these loads brings about huge losses [1-3]. The elimination or mitigation of disturbances propagated from the distribution system is absolutely required to improve the operational reliability of these loads.

The terminology and the guidelines for power quality has been described in detail at IEEE-519 and IEC-555 [4]. According to these guidelines, the voltage sag or swell is allowed by 10%, the total harmonic distortion is allowed by 5%, and the voltage unbalance is allowed by 10% [5].
UPQC has been widely studied in order to improve universal power quality by many researchers [6-8]. The function of UPQC is to mitigate the disturbance that affects the performance of the critical load. The UPQC, which has two inverters that share one dc link capacitor, can compensate the voltage sag and swell, the harmonic current and voltage, and control the power flow and voltage stability. However, the UPQC cannot compensate for the voltage interruption because it has no energy storage in the dc link.

This paper proposes a new configuration for the UPQC that consists of a DC/DC converter and super-capacitors for energy storage. The operation of the proposed system was verified through simulations with PSCAD/EMTDC software, and the feasibility of hardware implementation was confirmed through experimental works with a prototype of 20kVA rating.

2. Configuration of proposed UPQC

The UPQC is utilized for simultaneous compensation of the load current and the voltage disturbance at the source side. Normally the UPQC has two voltage-source inverters of three-phase four-wire or three-phase three-wire configuration. One inverter, called the series inverter is connected through transformers between the source and the common connection point. The other inverter, called the shunt inverter is connected in parallel through the transformers. The series inverter operates as a voltage source, while the shunt inverter operates as a current source.

The UPQC has compensation capabilities for the harmonic current, the reactive power compensation, the voltage disturbances, and the power flow control. However, it has no compensation capability for voltage interruption because no energy is stored.

This paper proposes a new configuration for the UPQC that has the super-capacitors for energy storage connected to the dc link through the DC/DC converter. The proposed UPQC can compensate the voltage interruption in the

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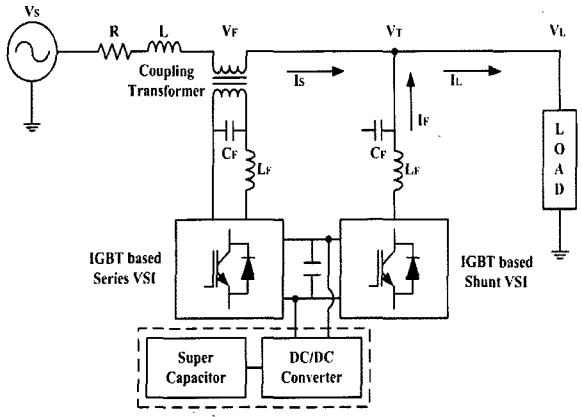


Fig. 1. UPQC system interconnected with energy storage

source side to make the shunt inverter operate as an uninterruptible power supply. Therefore, the shunt inverter operates as a voltage source in interruption mode as well as a current source in normal mode.

3. UPQC control strategy

The control system has four major elements, which are a positive sequence detector, a shunt inverter control, a series inverter control, and a DC/DC converter control. Fig. 2 shows the control system of the proposed UPQC, including the power circuit.

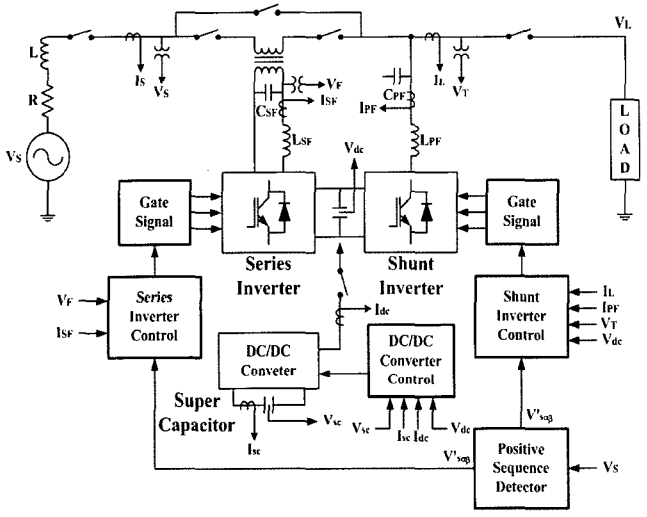


Fig. 2. Control system of proposed UPQC

The positive-sequence detector extracts the positive-sequence component from the disturbed three-phase source voltage. This detector derives the transformed reference voltage $V'_{S\alpha}$, $V'_{S\beta}$, based on the $\alpha-\beta-0$ transform. The measured source voltage passes through the PLL (Phase-Locked Loop) and the sine wave generator to calculate the fundamental component of the A-B transformed current, $i'_\alpha = \sin(\omega_1 t)$ and $i'_\beta = \cos(\omega_1 t)$. The calculated active power $\bar{p}'_S$ and reactive power $\bar{q}'_S$ includes the positive-sequence fundamental component of the source voltage V_S. So, the instantaneous value of the positive-sequence component is calculated as (1).

$$\begin{bmatrix} V'_{S\alpha} \\ V'_{S\beta} \end{bmatrix} = \frac{1}{i'^2_\alpha + i'^2_\beta} \begin{bmatrix} i'_\alpha & i'_\beta \\ i'_\beta & -i'_\alpha \end{bmatrix} \begin{bmatrix} \bar{p}'_S \\ \bar{q}'_S \end{bmatrix} \tag{1}$$

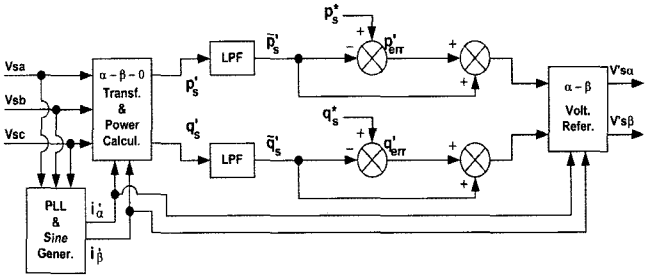


Fig. 3. Positive sequence voltage detector

3.1 Shunt Inverter Control

Two functions of the shunt inverter are to compensate the current harmonics and the reactive power, and to supply the active power to the load during voltage interruption. Fig. 4 shows the configuration of shunt inverter control, which includes the current control for harmonic compensation, and the output voltage control in voltage interruption.

In normal operation the shunt control calculates the reference value of the compensating current for the harmonic current and the reactive power, considering the power loss p_{loss} due to the system and inverter operation. This loss should be compensated to maintain the dc link voltage during operation of the series inverter. The reference value of the compensating current is derived using Equation (2).

$$\begin{bmatrix} i^*_{C\alpha} \\ i^*_{C\beta} \end{bmatrix} = \frac{1}{V'^2_{S\alpha} + V'^2_{S\beta}} \begin{bmatrix} V'_{S\alpha} & -V'_{S\beta} \\ V'_{S\beta} & V'_{S\alpha} \end{bmatrix} \begin{bmatrix} -\tilde{p} + p_{loss} \\ -q \end{bmatrix} \tag{2}$$

The reference voltage is determined using (3) and (4). The reference voltage V_1^* is expressed by the sum of the source voltage V'_S and the filter current difference ΔI_{PF} calculated by the PI controller.

$$\Delta I_{PF} = I^*_{PF} - I_{PF} \tag{3}$$

$$V_1^* = k_P \Delta I_{PF} + k_I \int \Delta I_{PF} dt \tag{4}$$

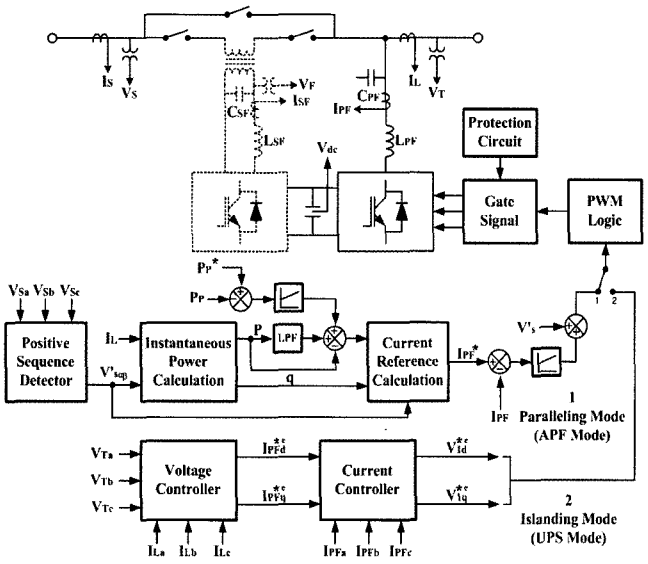


Fig. 4. Shunt inverter control block diagram

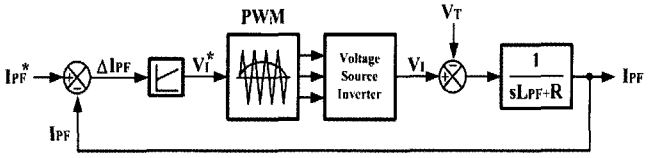


Fig. 5. Current control block diagram

If the shunt inverter is assumed to generate the reference voltage for each period of power frequency, the transfer function of the filter current can be derived as in (5).

$$\frac{I_{PF}}{I_{PF}^{*}}=\frac{(k_P/L_{PF})s+(k_I/L_{PF})}{s^2+\{(k_P+R)/L_{PF}\}s+(k_I/L_{PF})} \tag{5}$$

When the voltage interruption occurs, the operation mode is changed from normal compensation mode to interruption compensation mode. The super-capacitors provide the active power to maintain the load voltage constant. The shunt inverter starts to perform the voltage and current control using the PI controller.

The dynamic equations can be derived using the equivalent circuit of a shunt inverter. The state equations for the voltage control and the current control can be expressed by (6) and (7).

$$\begin{aligned} I_{PFd}^{*e} &= K_{PI}(V_{Td}^{*e}-V_{Td}^{e})-\omega C_{PF}V_{Tq}^{e}+I_{Ld}^{e} \\ I_{PFq}^{*e} &= K_{PI}(V_{Tq}^{*e}-V_{Tq}^{e})+\omega C_{PF}V_{Td}^{e}+I_{Lq}^{e} \end{aligned} \tag{6}$$

$$\begin{aligned} V_{1d}^{*e} &= K_{PI}(I_{PFd}^{*e}-I_{PFd}^{e})-\omega L_{PF}I_{PFq}^{e}+V_{Td}^{e} \\ V_{1q}^{*e} &= K_{PI}(I_{PFq}^{*e}-I_{PFq}^{e})+\omega L_{PF}I_{PFd}^{e}+V_{Tq}^{e} \end{aligned} \tag{7}$$

Fig. 6 presents the block diagram for implementing the above equations derived from the equivalent circuit.

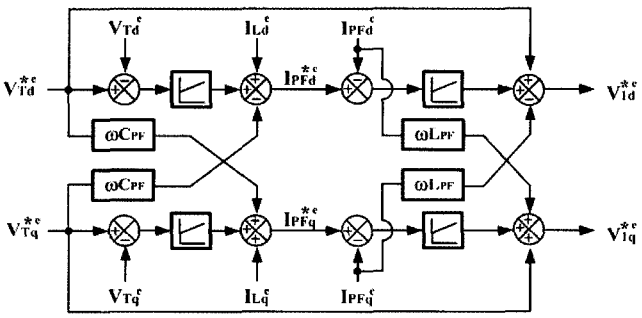


Fig. 6. Voltage control of shunt inverter

3.2 Series Converter Control

The function of the series inverter is to compensate the voltage disturbance on the source side, which is due to the fault in the distribution line. The series inverter control calculates the reference voltage to be injected by the series inverter, comparing the positive-sequence component with the disturbed source voltage. The reference voltage for PWM switching of the series inverter is obtained from the proportional control and the feed-forward control. Equation (8) shows the control equation needed to calculate the reference voltage. Fig. 7 presents the configuration of the series inverter control, which is based on this equation.

$$v_{ref}=[(v_s^{*}-v_s)-v_c]\times \mathrm{k}+v_c^{*} \tag{8}$$

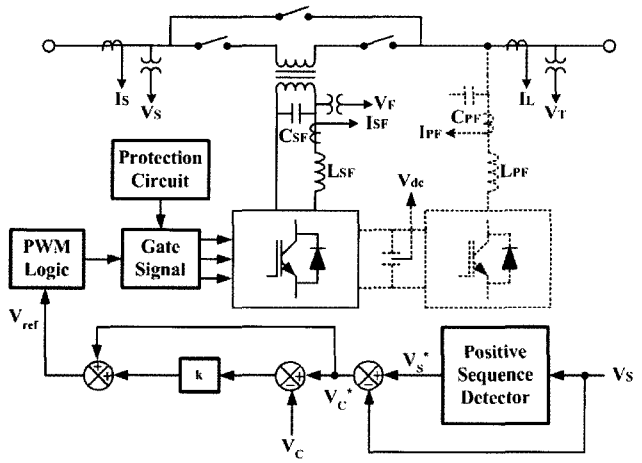


Fig. 7. Control block diagram of the series converter

4. DC/DC CONVERTER

The DC/DC converter is located between the energy storage and the DC-link capacitor. The DC/DC converter charges the super-capacitor for energy storage under normal operation, and discharges the super-capacitors for energy release during the voltage interruption. The DC/DC converter can operate in bi-directional mode using soft-switching scheme [9, 10].

4.1. Energy Storage Design

The size of the super-capacitors is determined depending on the duration of voltage interruption and the size of connected load. It is assumed that the voltage interruption has a duration of 2 sec and the load has a power rating of 20kW. Therefore, total energy to be released during the voltage interruption is 40kJ.

The bank of super-capacitors is designed considering three criteria, the expandability of storage capacity, the imbalance of unit voltage, and the current rating of each unit. HP1700P-0027A, manufactured by Ness Company was selected as a basic unit for the energy storage bank. Table 1 shows the specification of the selected super-capacitor unit.

Table 1. Specification of super-capacitor unit

Parameters	Specification
Capacitance	1700 F
ESR @25°C DC (100A)AC (100Hz)	0.7 M ohms 0.7 M ohms
Continuous operation voltage Peak operation voltage	2.7 V 2.85 V
Current rating	360 A

The bank is designed so as to utilize the upper 25% of maximum storage capacity considering the expandability of operation capacity while adding more super-capacitors. The super-capacitor is charged by 2.43V, 90% of the maximum charging voltage of 2.7V, considering 10% of deviation in the maximum charging voltage. The lowest discharged voltage is determined to be 2.1V using the following equation.

$$V_{bank\_\min} = 40kW / 360A = 111\,\mathrm{V} \tag{9}$$

The maximum current flows through the super-capacitor unit, when it discharges the maximum power and is at the lowest discharging voltage. The maximum voltage across the super-capacitor bank can be determined with the maximum discharge power and the maximum current as follows.

$$V_{unit\_\min} = \sqrt{3/4} \times V_{unit\_\max} = 2.1\,\mathrm{V} \tag{10}$$

Therefore, the lowest discharge voltage and the maximum allowable voltage of the super-capacitor determine the number of units to be connected in series as follows.

$$N = V_{bank\_\min} / V_{unit\_\min} = 53 \tag{11}$$

However, the bank was designed using a total of 56 units of super-capacitors for the purpose of safety margin.

4.2. Converter Design

The operation voltage of the super-capacitor bank is in the range between 115-135V, while the dc link voltage is about 700V. The ground point in the dc link should be isolated from the ground point in the super-capacitor bank. The converter should have a high current rating in the bank side and a high voltage rating in the DC link side. Considering these requirements, a DC/DC converter with two full-bridges was selected as shown in Fig. 8.

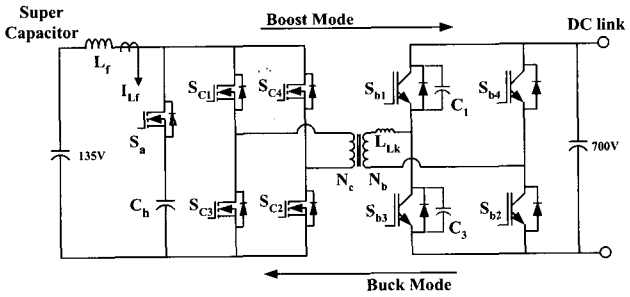


Fig. 8. DC/DC converter structure

A filter reactor is inserted between the bank and the full-bridge to reduce the ripple of the charging and discharging current, which can reduce the life of the super-capacitors due to unwanted heat generation. The full-bridge on the bank side works as a current-fed type, while the full-bridge on the dc link side works as a voltage-fed type.

In discharge mode, the DC/DC converter boosts the super-capacitor voltage up to the nominal dc link voltage. The super-capacitor voltage is controlled between 118-135V, while the dc link voltage increases up to 700V. The switches S_{C1} and S_{C4} operate with the duty ratio higher than 0.5. The current through the inductor L_f increases as all the switches are on conduction state. The voltage overshoot can be suppressed by the conduction of auxiliary switch S_a when two switches facing diagonal opposition are on conduction state. The current through the transformer rises linearly and its peak value becomes larger than the current through the boost inductor. When the auxiliary switch turns off, the magnetic energy stored in the leakage inductance of the transformer flows through the back-connection diode of the switch in off state. So, the zero-voltage turn-on condition is provided.

In charge mode, the DC/DC converter decreases the nominal dc-link voltage down to the level of super-capacitor voltage. When switches S_{b1} and S_{b2} turn on, the input voltage applied to the leakage inductance of

transformer L_{Lk} increases the input current. The power in the primary side is transferred to the secondary side. The secondary voltage charges the capacitor C_h through the reverse connected diode of auxiliary switch S_a. If the charging voltage is high enough to make the charging current zero, switch S_{b1} turns off. Switch S_{b3} turns off with zero-voltage scheme while capacitor C_1 is charged and capacitor C_3 is discharged. When auxiliary S_a turns on, the voltage across the auxiliary capacitor affects the primary voltage of the coupling transformer. This voltage is applied to the leakage inductance L_{Lk} with reverse polarity. This makes the primary current zero and switch S_{b2} turns off with zero-current scheme.

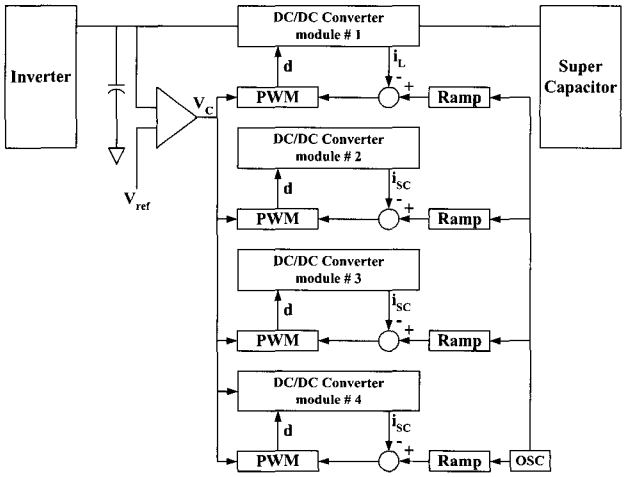


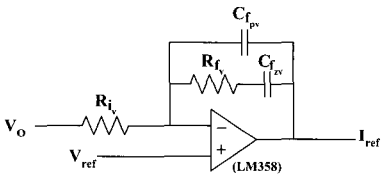
Fig. 9. Four module parallel operation and PWM pulse interleaving

From a design point of view it is not effective to build a single 20kW DC/DC converter due to the restriction in power rating of the switching unit. Since super-capacitors operate at low-voltage large-current, the switching frequency is limited by the critical value of di/dt, which depends on the leakage inductance of the coupling transformer. So, when the converter is designed in a single module, the switching ripple of charging or discharging current is high. Therefore, the proposed DC/DC converter has four modules of a 5kW converter connected in parallel instead of one module of a 20kW converter. When the multi-module is used, it is possible to expand the system rating and to increase the operation reliability. Also, the switching ripple of the charging or discharging current can be sharply reduced using the interleaving scheme of PWM switching.

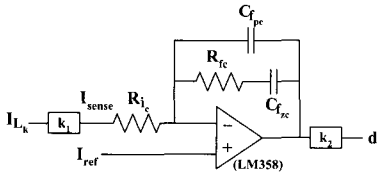
4.3. Controller Design

The controller of the DC/DC converter is comprised of the main control, charging control, and discharging control. One function of the main control is to select the charge mode and discharge mode according to the command from the UPQC main controller. The other function of the main control is to monitor the operation of each converter module and to remove the module in fault. The main control also monitors the maximum and minimum charge or discharge voltage.

The discharge control was designed to charge the super capacitors when the voltage interruption occurs in the ac side. The charge operation is performed with four modules in the 20kW power rating. The discharge control consists of two control loops, which are the outer loop of voltage control and the inner loop of current control as shown in Fig. 10. The voltage control loop measures the DC link voltage and compares it with the reference voltage. The error passes through the RC circuit to calculate the reference current for the inner-loop current control. The inner-loop current control measures the discharge current on bank side and compares it with the reference current obtained from the outer-loop voltage control. The error passes through the RC circuit to calculate the duty ratio for the DC/DC converter module.



(a) Outer-Loop voltage control



(b) Inner-Loop current control

Fig. 10. Discharge control structure

The charge control was designed to charge the super capacitor in a slow speed in order to prevent any DC link voltage change under normal operation. The charge operation is performed with only one module in the 2kW power rating and stops when the bank voltage reaches 135V. The operation of charge control has the same configuration as that of the battery charger.

5. Computer Simulation

Many computer simulations with PSCAD/EMTDC software were performed for the purpose of analyzing the operation of the proposed UPQC. The power circuit is modeled as a 3-phase 4-wire system with a non-linear load that is composed of a 3-phase diode-bridge with RL load

on the dc side. The controller was modeled using the built-in control block in the PSCAD/EMTDC software. The circuit parameters used in the simulation are shown in Table II. The maximum simulation time was set up by 700ms. It is assumed that the shunt inverter started to operate at 100ms, while the series inverter started to operate at 200ms.

Table 2. Simulation parameters

Source	Voltage	380V, 60Hz
	Impedance	R=0.001Ω, L=0.01mH
DC-Link	Capacitor	C1=6600uF, C2=6600uF
	Reference Voltage	700V
Shunt Inverter	Filter L, C	600uH, 40uF
	Switching Freq.	10kHz
Series Inverter	Filter L, C	600uH, 40uF
	Switching Freq.	10kHz
	Injection Trans.	500:100, 6KVA
Load	Non-linear Load	17.54KVA
	Linear Load	3.27KVA
DC/DC Converter	Boost Inductor L_f	100uH
	Capacitor C_h	35uF
	Switching Freq.	35kHz

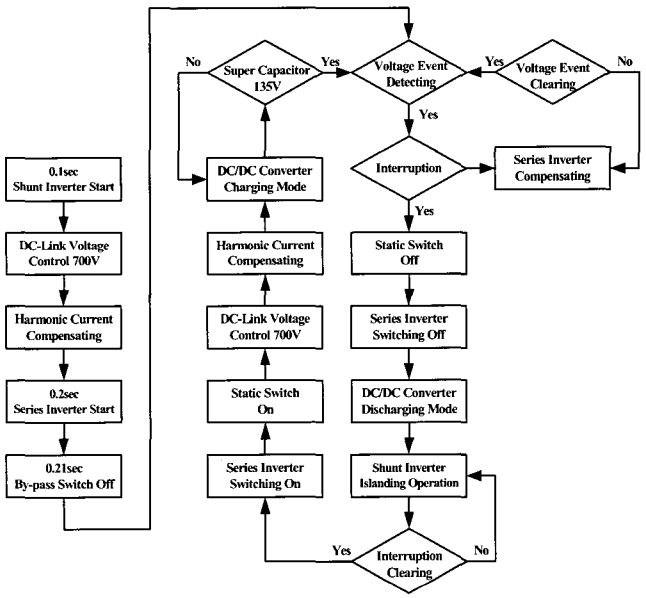


Fig. 11. UPQC operation diagram

Fig. 11 shows the entire procedure used in the simulation of the proposed UPQC operation. The voltage disturbance such as sag and swell can be compensated without the energy storage element, but the voltage interruption requires the energy storage element. The operational flow diagram explains the procedure to distinguish the voltage interruption from the voltage sag and swell.

Fig. 12 presents the shunt inverter operated in the active power filter mode. The 1st, 2nd, 3rd graph shows respectively the current waveform of the source, the shunt inverter, and the load, which confirms the operation of the active power filter.

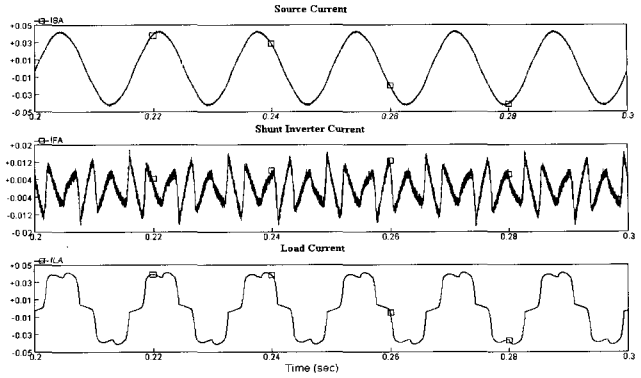


Fig. 12. Active-Power Filter operation

Fig. 13 shows the compensated result when the voltage sag occurs on the source side. It is assumed that phase A and B have 30% of sag voltage and phase C has no sag voltage as shown in the 1st graph. The 2nd graph indicates the output voltage of the series inverter. The last graph displays the load voltage compensated by the UPQC.

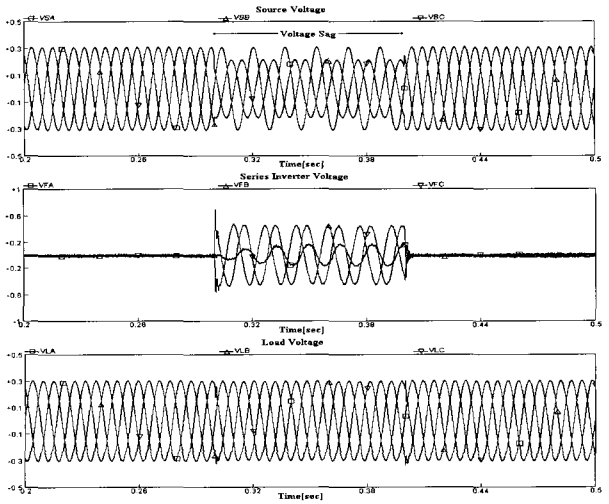


Fig. 13. UPQC operation during voltage sag

Fig. 14 shows the compensated result when the voltage swell occurs. It is assumed that Phase A has 30% of swell voltage and the other two phases have normal voltages as presented in the 1st graph. The 2nd graph shows the output voltage of the series inverter. The last graph presents the load voltage compensated by the UPQC.

Fig. 15 shows the compensated result when the voltage interruption occurs. It is assumed that three-phase fault takes place for 100ms as shown in the 1st graph. The 2nd graph indicates the output voltage across the load compensated by the UPQC. The 3rd graph shows the output current supplied by the DC/DC converter. The last graph displays the power variation during the voltage interruption

During the interruption the source voltage decreases and the shunt inverter provides the required power in the load.

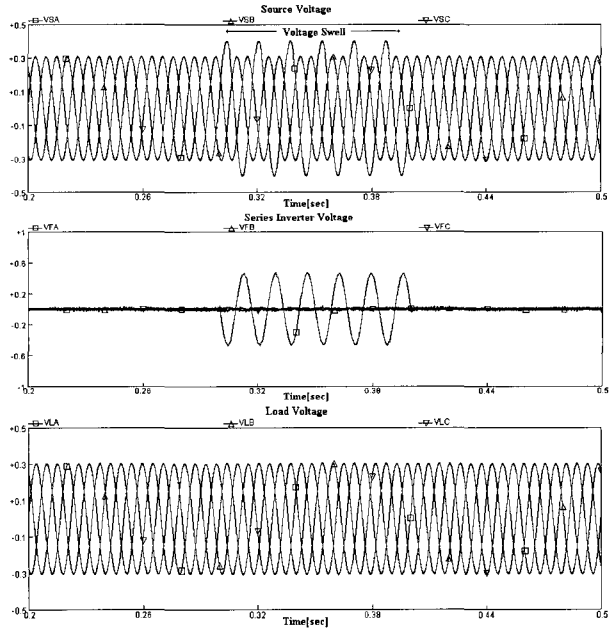


Fig. 14. UPQC operation during voltage swell

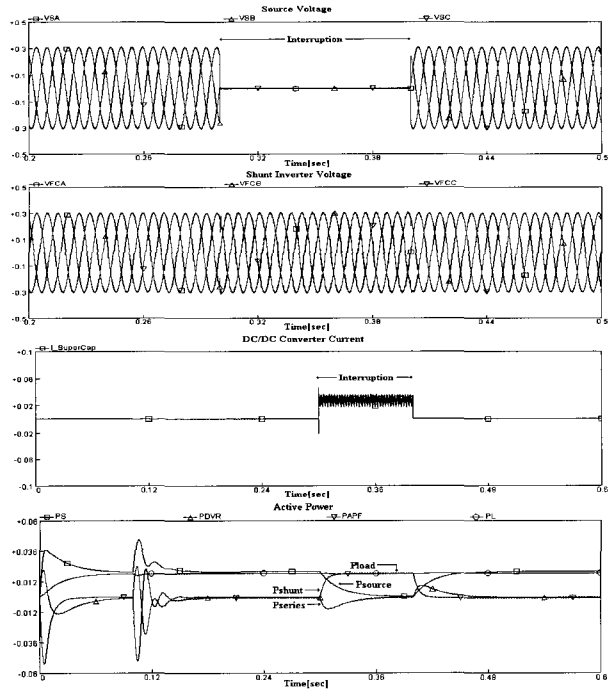


Fig. 15. UPQC operation during interruption

Fig. 16 shows the operational characteristics of the dc/dc converter in discharge mode. The 1st, 2nd, and 3rd graphs show respectively the current waveform through the main switch, the auxiliary switch, and the output current of the boost converter. The last graph indicates the voltage across the dc link, in which both are maintained as a constant value.

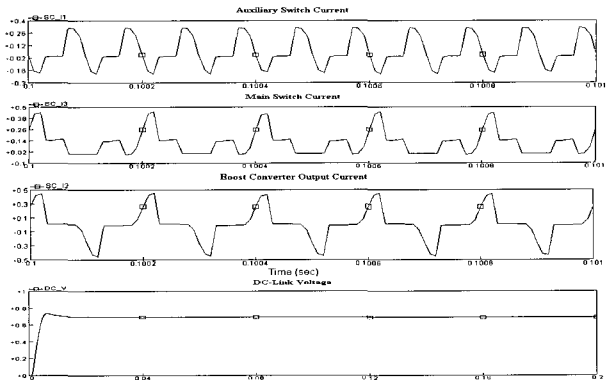
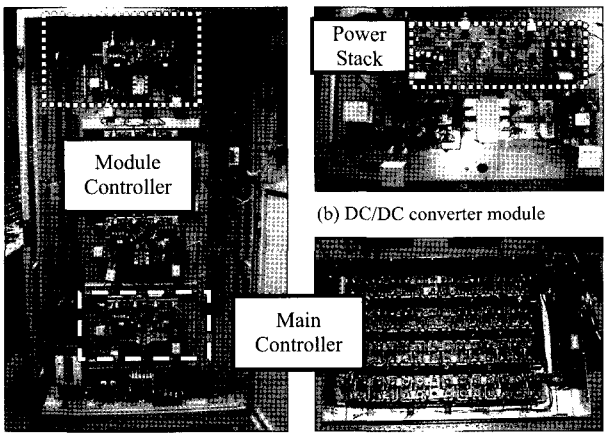


Fig. 16. DC/DC converter control results

6. Experimental Results

A prototype was built and tested to confirm the feasibility of actual hardware implementation. In order to simulate various fault cases, a source simulator using two inverters with a DSP processor was built in a separate cabinet, which can generate the voltage sag, the voltage swell, and the voltage interruption to simulate the voltage disturbance in the distribution system. Another UPQC was also built in a cabinet using two inverters with one solid-state switch and a DSP processor. A 20kW DC/DC converter with super-capacitors was built in a separate cabinet. There are four 5-kW DC/DC converter modules and four racks of super-capacitor banks, where each module is connected with each super-capacitor rack in an individual manner. Both linear and non-linear loads are built for experimental work. Each load is designed for simulating the various load conditions.



(a) DC/DC converter overall (c) Super-capacitor bank

Fig. 17. Hardware structure of DC/DC converter and super-capacitor bank

All the circuit parameters are exactly identical to those used in the computer simulation. All the experimental conditions are set up just the same as the simulation conditions. Fig. 18 shows the compensation of harmonic

current in the shunt inverter. Although there are some high-frequency harmonics, the experimental result is very close to the simulation result.

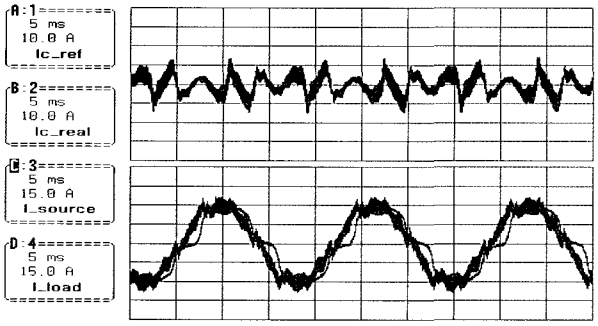


Fig. 18. Active-Power Filter operation

Figs. 19 and 20 show the experimental results when the unbalanced sag and swell occur. Both results are very close to the simulation results shown in Figs. 13 and 14.

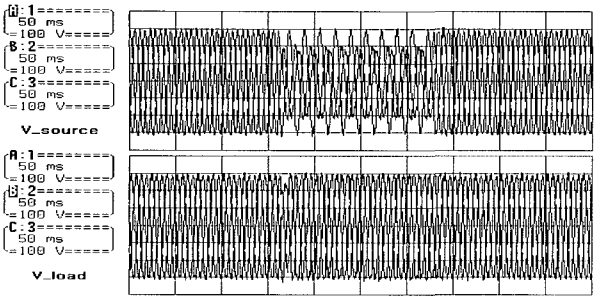


Fig. 19. UPQC operation during voltage sag

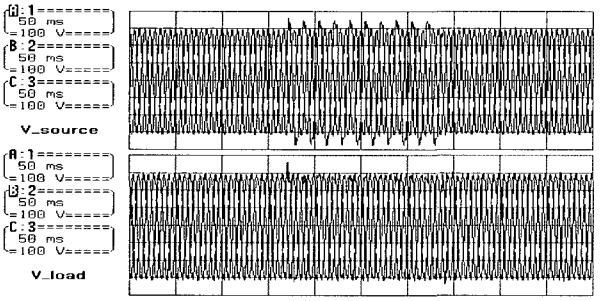
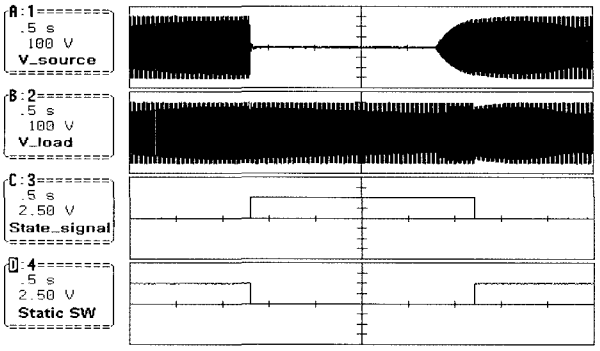


Fig. 20. UPQC operation during voltage swell

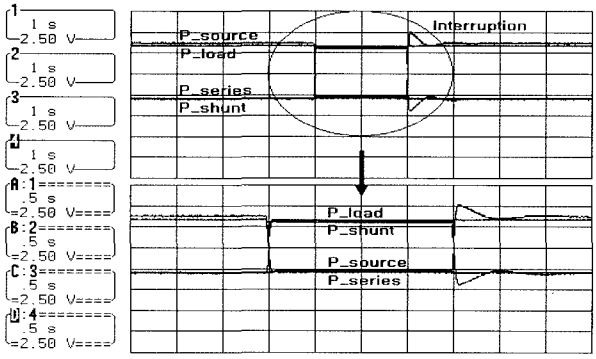
Fig. 21 shows the experimental results when the voltage interruption occurs. The 1st and 2nd graphs in Fig. 20(a) reveal the source voltage and the load voltage in the voltage interruption for 2 seconds. The load voltage can be maintained as a constant value as expected. The 3rd and last graph indicates the state signal for activating the solid-state breaker to isolate the source side.

Fig. 21(b) shows the active power variations during voltage interruption, which explains that the power required in the load is provided by the shunt inverter of the UPQC during the voltage interruption.

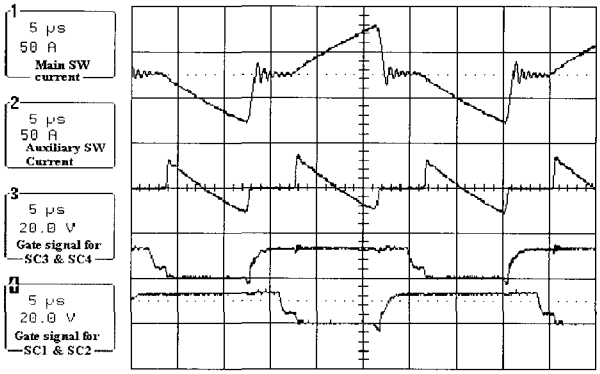
The 1st and 2nd graphs in Fig. 21(c) show the current through the main switch and the current through the



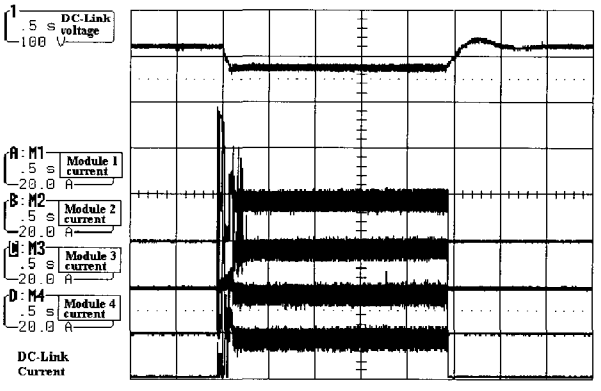
(a) Source voltage and load voltage, static switch gate signal



(b) Active power variation during voltage interruption



(c) DC/DC converter 1st output current, auxiliary switch current and main switch gate signal



(d) DC-Link voltage and converter module output current

Fig. 21. UPQC operation during interruption

auxiliary switch, which are very similar to the simulation result. The 3rd and last graph indicates the gate signal for activating the four main switches.

The 1st graph in Fig. 21(d) presents the voltage in the dc link, which is maintained at 680V less than the normal DC link voltage of 720V. But the control system increases the modulation index to maintain the output voltage properly. The 2nd, 3rd, 4th, and last graph presents the dc link current from each DC/DC converter module, which confirms that each module provides a balanced constant current.

5. Conclusion

This paper proposes a new configuration for the UPQC (Unified Power Quality Conditioner), which consists of series inverter, shunt inverter, DC/DC converter, and super-capacitors for energy storage. The proposed UPQC can compensate the reactive power, harmonic current, voltage sag and swell, voltage imbalance, and voltage interruption. The control strategy for the proposed UPQC was derived based on the instantaneous power method. The operation of the proposed system was verified through simulations with EMTDC software, and the feasibility of hardware implementation was confirmed through experimental works with a prototype of 20kVA rating.

The proposed UPQC has the ultimate capability of improving the power quality at the point of installation on power distribution systems or industrial power systems.

Acknowledgements

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References

[1] N. G. Hingorani, "Introducing Custom Power," IEEE Spectrum, pp. 41-48, June 1995.

[2] Jos Arrillaga, Math H. J. Bollen, Neville R. Watson, "Power Quality Following Deregulation", Proceedings of the IEEE, Vol. 88, No. 2, Feb. 2000.

[3] Prodanovic. M, Green. T. C, "Control and filter design of three-phase inverters for high power quality grid connection", IEEE Trans. on Power Delivery, Vol. 18, No. 1, pp. 373-380, Jan. 2003.

[4] W. Edward Reid, "Power Quality Issues - Standards and Guidelines". IEEE Transactions on Industry Applications, Vol. 32, No. 3, May/June 1996.

[5] Douglas S. Dorr, "Point of Utilization Power Quality Study Results", IEEE Transactions on Industry Applications, Vol. 31, No. 4, July/August 1995.

[6] Hideaki Fujita, Hirofumi Akagi, "The Unified Power Quality Conditioner: The Integration of Series- and Shunt- Active Filters", IEEE Transactions on Power Electronics, Vol. 13, No. 2, March 1998.

[7] Yunping Chen, Xiaoming Zha and Jin Wang, etc. "Unified Power Quality Conditioner (UPQC): The Theory, Modeling and Application", Power System Technology, 2000 proceedings. Power Con 2000. International Conference on, Vol. 3, pp. 1329-1333 2000.

[8] M. Aredes, K. Heumann, E. H. Watanabe, "An universal active power line conditioner", IEEE Trans. on Power Delivery, Vol. 13, No. 2, pp. 545-551, Apr 1998.

[9] A. Bendre, S. Norris, D. Divan, I. Wallace, R. Gascoigne, "New high power DC-DC converter with loss limited switching and lossless secondary clamp", IEEE Trans. on Power Electronics, Vol. 18 , No. 4, pp. 1020-1027, July 2003.

[10] J. Jacobs, A. Averberg, R. De Doncker, "A novel three-phase DC/DC converter for high-power applications", IEEE Conf. on PESC 04, Vol. 3, 20-25, pp. 1861-1867, June 2004.

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