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# 저전력 테스트 데이터 압축 개선을 위한 효과적인 기법

## ( An Efficient Technique to Improve Compession for Low-Power Scan Test Data )

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요 약

오늘날 시스템 온 칩 테스트에 있어서 많은 양의 테스트 데이터, 시간 및 전력 소모는 매우 중요한 문제이다. 이러한 문제들을 해결하기 위해서 본 논문은 새로운 테스트 데이터 압축 기술을 제안한다. 우선, 테스트 큐브 집합에 있는 돈 캐어 비트에 저전력 테스트를 위한 비트할당을 한다. 그리고, 비트할당이 된 저전력 테스트 데이터의 압축효율을 높이기 위해 이웃 비트 배타적 논리합 변환을 사용하여 변환한다. 최종적으로, 변환된 테스트 데이터는 효과적으로 압축 됨으로써 테스트 장비의 저장공간과 테스트 데이터 인가시간을 줄일 수 있게 된다.

Abstract

The huge test data volume, test time and power consumption are major problems in system-on-a-chip testing. To tackle those problems, we propose a new test data compression technique. Initially, don't-cares in a pre-computed test cube set are assigned to reduce the test power consumption, and then, the fully specified low-power test data is transformed to improve compression efficiency by neighboring bit-wise exclusive-or (NB-XOR) scheme. Finally, the transformed test set is compressed to reduce both the test equipment storage requirements and test application time.

**Keywords** : test data compression, low power, scan test, soc test

## Ⅰ. 서 론

Power dissipation is one of major challenges in today's circuit design. Generally, a circuit or system consumes more power caused by excessive switching activities in test mode than in normal mode, and it has been confirmed that the shift power in the scan chains is the dominant contributor to test power[1]. This extra power consumption can incur severe hazards in circuit reliability or, in some cases, can provoke instant circuit damage[1]. Thus, it is extremely important to reduce power consumption for SoC test, and so a number of techniques to reduce power consumption in test mode have been presented in literature[2]-[5].

In addition to power-related challenges, another emerging problem is the highly growing test data volume for SoC test. The ATE storage requirement depends on the amount of test data, and the total test time required for testing a chip also depends on the test data volume as well as the test data bandwidth for transferring the data. Thus, large test data volume can lead to increasing overall manufacturing

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cost. To tackle these problems, recently, a number of test data compression techniques have been proposed to reduce SOC test data volume[1], [6-14].

Therefore, recently, the test data compression techniques to achieve simultaneous reduction in both test data volume and test power consumption have been proposed[1], [7], [13], [14], which use the minimum transition count filling (MTC-filling) of don't-cares in the test set to improve the power reduction efficiency during scan test. We also used the MTC-filling for our low-power scan test. However, MTC-filling makes the tradeoffs between power reduction and compression efficiency. This is because fundamentally most data compression techniques take advantage of the redundancy of data, and thus the data which is biased can be more efficiently compressed. But, the fully specified test set by MTC-filling does not satisfy this nature.

Therefore, to improve test compression efficiency by biasing a data value against another, the test data transformation technique for the fully specified test data is proposed in [9], and it was shown in [6][8-10] that compressing a difference vector sequence made by using this scheme results in smaller test. However, this approach has the obvious drawback requiring a separate cyclical scan register (CSR) for decompressing[13]. Moreover, optimal scan vector reordering to get the best results is NP-complete problem.

In this paper, we propose a new test data compression/decompression technique for the simultaneous reduction of test data volume and scan power. The key idea of our approach is to use neighboring bit-wise exclusive-OR (NB-XOR) transformation technique to improve compression efficiency of low-power scan test data applied by MTC-filling. Experimental results for the various compression schemes show the efficiency of the proposed technique.

This paper is organized as follows. Our approach is described in section II and experimental results for ISCAS'89 benchmark circuits are presented in section III followed by concluding remarks.

## II. 본 론

### 1. Proposed approach

For compression, initially, don't-cares in a pre-computed test cube set are specified by using MTC-filling for low-power scan test, and then, the fully specified test set is transformed to improve compression efficiency by using the neighboring bit-wise exclusive-OR (NB-XOR) transform which results in skewed data containing a lot of consecutive 0s. Finally, the transformed test set can be significantly compressed by using various coding schemes which exploit the properties of biased test data.

#### 가. Don' t-care filling for low-power scan test

It is noted that the test patterns generated by automatic test pattern generator (ATPG) generally contain more don't-cares than fixed values. This is because, to detect a certain fault, only a small number of bits need to be specified in a scan vector. Therefore, by properly assigning fixed values to don't-cares, test data set for low-power scan test can be achievable.

Thus, in our technique, we adopted the minimum transition count filling (MTC-filling) technique which minimizes the weighted transition metric (WTM)[15] to reduce scan-in power consumption. The WTM model is proposed to estimate the power by counting transitions during scan shifting. For example, consider a scan vector "0XX1XX111", MTC-filling of don't-cares results in "000111111". For scan-out power consumption, it is experimentally shown in [13] that the number of transitions and the resulting WTM during scan out are also reduced by using MTC-filling.

In order to explain the experimental results in section III, we present how WTM, average and peak scan-in power are estimated as follows:

$$WTM_j = \sum_{i=1}^{l-1} (l-i) \cdot (b_{j,i} \oplus b_{j,i+1}) \qquad (1)$$

$$P_{avg} = \frac{\sum_{j=1}^{n}\sum_{i=1}^{l-1}(l-i)\cdot(b_{j,i}\oplus b_{j,i+1})}{n} \quad (2)$$

$$P_{peak} = \max_{j\in\{1,2,\ldots,n\}}\left\{\sum_{i=1}^{l-1}(l-i)\cdot(b_{j,i}\oplus b_{j,i+1})\right\} \quad (3)$$

Consider a scan chain of length l and a scan vector Vi = bj,1, bj,2,…, bj,l with bj,1 scanned in first. The WTM for jth vector Vj is given by (1). If n is the number of scan vectors, the average and peak scan-in power are estimated by (2) and (3), respectively.

### 나. Neighboring bit-wise exclusive-or transform

In this section, we describe our transform technique which is the pre-processing method before compressing low-power scan test data to achieve high compression.

Before describing our technique, we first briefly review the cyclical scan register (CSR) scheme[9] to compare with ours, because, to the best of our knowledge, this is the only state-of-the-art approach to transform the fully specified test data into the skewed dada with a lot of 0s for high compression.

In the CSR based technique, compression is performed on the difference vector set achieved by using correlation between scan vectors to generate a lot of 0s in order to enhance compression efficiency, so, as shown in [8], [9], [10]. However, this approach has the obvious drawback requiring a separate cyclical scan register (CSR) for decompressing. Furthermore, optimal scan vector reordering to get the best results is NP-complete problem, and in section Ⅲ, experimental results comparing between CSR and our techniques show the efficiency of ours.

In our technique, first, don't-cares in a pre-computed scan vectors are assigned by using MTC-filling to save scan test power, and then this yields the fully specified test set TD = {v1, v2, v3 ,…,vm}, where vi is the ith scan vector, having a lot of long runs of both 0s and 1s. Next, TD is transformed to improve compression efficiency by using the neighboring bit-wise exclusive-OR

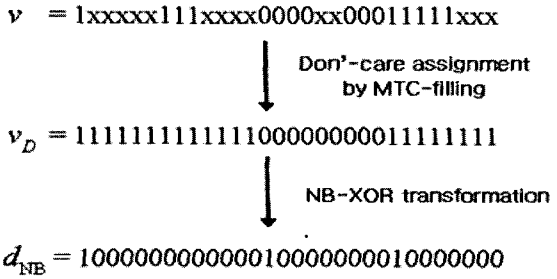


그림 1. NB-XOR 변환의 예
Fig. 1. Example of NB-XOR transform.

(NB-XOR) transform which performs XOR between neighboring bits on scan vector vi = {bi_1, bi_2, bi_3,…, bi_n}, where bi_j is the jth bit in it, and this results in the NB-XORed difference vector set TNB which is highly biased to 0s, and

compression is carried out on it. TNB is defined as follows:

TNB = {dNB1, dNB2, dNB3, …, dNBm}

dNBi = {bNBi_1, bNBi_2, bNBi_3,…, bNBi_n-1, bNBi_n}

= {bi-1_n⊕bi_1, bi_1⊕bi_2, bi_2⊕bi_3, …, bi_n-1 ⊕bi_n}

where dNBi and bNBi_j are the ith NB-XORed difference vector and the jth NB-XORed difference bit in it, respectively. bNBi_j is obtained by executing XOR between both neighboring bits bi_j-1 and bi_j in vi. It is noted that the first difference bit bNBi_1 of dNBi is obtained by performing XOR between both the last bit of vi-1 and the first bit of the following scan-in vector vi, except that the first difference bit bNB1_1 in dNB1 is equal to b1_1 in the first scan vector v1. Fig. 1 shows an example of NB-XOR transform procedure sequenced by v, vD and dNB, where v, vD and dNB are a pre-computed scan vector with don't-cares, a fully specified scan vector after don't-care assignment by MTC-filling and an NB-XORed difference vector we achieved at the end, respectively, and the left most bit for each vector is the first bit scanned into a scan chain with length 30. The total number of 1s in vD is 21 and

this is greatly reduced to a total of 3 as seen in dNB by NB-XOR technique.

Therefore, as shown in Fig. 1, after MTC-filling of don't-cares, NB-XOR scheme can fully exploit the characteristics of the low-power scan vectors due to a umber of long runs of both 0s and 1s which have consecutive bit values. Moreover, this technique can take additional advantage of runs of 1s which are specified already before MTC-filling so that, in some cases, there are more 0s in TNB than in the test data set applied by zero-filling for don't-cares. Finally, the transformed test set TNB can be substantially compressed by exploiting the test data highly biased to 0s.

### 다. Decompression Architecture based on NB-XOR technique

Fig. 2 shows the generic decompression architecture, where TE, TNB, and TD are the compressed scan data, the decompressed NB-XORed difference scan data, and the original low-power scan data, respectively. In Fig. 2, to test the CUT with a single scan chain, first, the compressed NB-XORed difference vectors (TE) from an ATE are transferred to an on-chip decoder which decompresses them into the original NB-XORed difference vectors (TNB). And then the decompressed vectors are fed into the inverse NB-XOR block, which consists of a simple pair of one XOR gate and one flip-flop, to transform them into the original low-power scan vectors (TD) under the assumption that the flip-flop is initialized to 0. Finally, the transformed vectors are shifted into the internal scan chain. The serial output of this flip-flop feeds the serial input of the scan chain, and at the same time it loops back and is XORed with the serial output of the decoder.

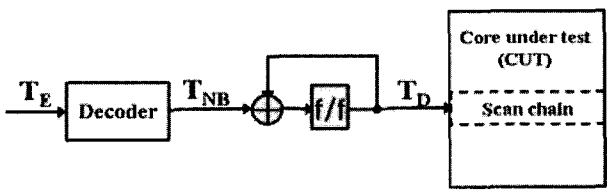


그림 2. NB-XOR 방식을 기반으로 한 일반적인 decompression 구조

Fig. 2. Generic decompression architecture based on NB-XOR technique.

It can be seen that our technique requires less area overhead than the CSR, since the CSR-based scheme includes separate cyclical scan chain which has the same length of the internal scan chain of the core under test, and the scan chain length is generally from hundreds to several thousands. But our technique requires only one flip-flop and XOR gate. Therefore, with very little hardware overhead, the NB-XOR technique enables us to achieve a significant test data compression for MTC-filled low-power scan test data. In addition, our technique does not require any knowledge or modification of the internal structure of the core.

## Ⅲ. 실 험

In this section, the experimental results are described for large ISCAS'89 benchmark circuits to evaluate the efficiency of the proposed technique. For each circuit, we have used the full-scan version with a single scan chain, and test patterns were generated by the test pattern generation program, MinTest. The computing environment was Pentium Ⅳ computer with 1 Gbytes memory.

$$\frac{P_{avg}(Zero-filling)-P_{avg}(MTC-filling)}{P_{avg}(Zero-filling)}\times 100(\%) \quad (4)$$

$$\frac{P_{peak}(Zero-filling)-P_{peak}(MTC-filling)}{P_{peak}(Zero-filling)}\times 100(\%) \quad (5)$$

Table 1 compares the results on the peak and average power consumption during the scan-in operation for two different don't-care filling techniques of the Zero-filling and MTC-filling. The equations (4) and (5) indicate the average and peak power reduction of the Zero-Filling and MTC-filling.

As shown in Table 1, the MTC-filling of the don't-cares leads to more significant savings in average and peak power consumption than the Zero-filling, in all cases.

표 1. 두 가지 don't-care filling 방식에 대한 전력소모 비교

Table 1. Comparison of power consumption results for two different don't-care filling techniques.

| Circuit | Test data (bits) | Zero-Filling | | MTC-Filling | | Power Reduction(%) | |
|---|---|---|---|---|---|---|---|
| | | $P_{avg}$ | $P_{peak}$ | $P_{avg}$ | $P_{peak}$ | Avg. | Peak |
| s5378 | 23754 | 4300 | 12085 | 3523 | 11732 | 18.07 | 2.92 |
| s9234s | 39273 | 6705 | 15395 | 4002 | 14092 | 40.31 | 8.46 |
| s13207 | 165200 | 12317 | 110129 | 8073 | 94879 | 34.46 | 13.85 |
| s15850 | 76986 | 19448 | 84360 | 13611 | 70875 | 30.01 | 15.99 |
| s38417 | 164736 | 194843 | 514716 | 118098 | 437884 | 39.39 | 14.93 |
| s38584 | 199104 | 133322 | 530464 | 86135 | 481158 | 35.39 | 9.29 |

표 2. MTC don't-care filling과 다른 변환 방식에 대한 영의 비율 비교

Table 2. Comparison of zero ratios for MTC' don't-care filling and transform techniques.

| Circuit | Test Data (bits) | Don't-Cares (%) | Ratios of '0'(%) | | |
|---|---|---|---|---|---|
| | | | MTC -Filling | MTC-Filling | |
| | | | | CSR[9] | NB-XOR |
| s5378 | 23754 | 72.62 | 49.83 | 79.94 | 86.87 |
| s9234 | 39273 | 73.01 | 48.71 | 78.10 | 87.54 |
| s13207 | 165200 | 93.15 | 54.93 | 85.52 | 96.72 |
| s15850 | 76986 | 83.56 | 49.65 | 77.14 | 92.70 |
| s38417 | 164736 | 68.08 | 46.32 | 75.24 | 91.66 |
| s38584 | 199104 | 82.28 | 52.84 | 64.58 | 91.83 |

표 3. 그룹 크기가 4인 Golomb[6] 코드를 이용한 압축 결과 비교

Table 3. Comparison of compression results using Golomb[6] code with group size of 4.

| Circuit | Test Data (bits) | MTC -Filling | MTC-Filling | |
|---|---|---|---|---|
| | | | CSR | NB-XOR |
| s5378 | 23754 | -60.52 | 20.01 | 42.03 |
| s9234 | 39273 | -63.77 | 15.54 | 44.57 |
| s13207 | 165200 | -48.30 | 34.65 | 67.05 |
| s15850 | 76986 | -62.08 | 11.65 | 57.13 |
| s38417 | 164736 | -71.05 | 7.27 | 54.34 |
| s38584 | 199104 | -53.15 | -21.26 | 55.03 |

Table 2 compares the efficiency of biasing to 0s for different transform techniques for MTC-filled test data, and NB-XOR approach outperforms both the pure MTC-filling and CSR-based technique[9] after MTC-filling, in all cases. To estimate compression

표 4. 그룹 크기가 8인 Golomb[6] 코드를 이용한 압축 결과 비교

Table 4. Comparison of compression results using Golomb[6] code with group size of 8.

| Circuit | Test Data (bits) | MTC -Filling | MTC-Filling | |
|---|---|---|---|---|
| | | | CSR | NB-XOR |
| s5378 | 23754 | -105.06 | 8.67 | 39.15 |
| s9234 | 39273 | -108.92 | 2.79 | 42.96 |
| s13207 | 165200 | -86.51 | 30.40 | 75.90 |
| s15850 | 76986 | -106.24 | -2.43 | 61.40 |
| s38417 | 164736 | -119.21 | -8.64 | 57.30 |
| s38584 | 199104 | -93.77 | -48.90 | 58.33 |

표 5. FDR[8] 코드를 이용한 압축 결과 비교

Table 5. Comparison of compression results using FDR[8] code.

| Circuit | Test Data (bits) | MTC -Filling | MTC-Filling | |
|---|---|---|---|---|
| | | | CSR | NB-XOR |
| s5378 | 23754 | -14.88 | 38.20 | 49.96 |
| s9234 | 39273 | -20.70 | 33.12 | 45.13 |
| s13207 | 165200 | 2.39 | 62.19 | 80.15 |
| s15850 | 76986 | -12.85 | 37.64 | 65.63 |
| s38417 | 164736 | -19.33 | 32.07 | 60.64 |
| s38584 | 199104 | -7.67 | 11.10 | 61.09 |

표 6. RL-Huffman[14] 코드를 이용한 압축 결과 비교

Table 6. Comparison of compression results using RL-Huffman[14] code.

| Circuit | Test Data (bits) | MTC -Filling | MTC-Filling | |
|---|---|---|---|---|
| | | | CSR | NB-XOR |
| s5378 | 23754 | 52.44 | 50.96 | 53.09 |
| s9234 | 39273 | 44.87 | 48.23 | 47.77 |
| s13207 | 165200 | 81.78 | 82.11 | 82.62 |
| s15850 | 76986 | 66.12 | 61.66 | 67.55 |
| s38417 | 164736 | 62.46 | 58.94 | 65.76 |
| s38584 | 199104 | 60.49 | 52.59 | 63.73 |

efficiency, compression ratio is defined as (6).

$$\frac{(OriginalBits - BitsAfterCompression)}{OriginalBits} \times 100(\%) \quad (6)$$

Compression ratios of various coding techniques are shown in Table 3, 4, 5 and 6, and these show that the scan test vectors transformed by NB-XOR technique after MTC-filling can be more efficiently compressed using well-known prior works such as Golomb[6], FDR[8] and RL-Huffman[14] code. The

negative value in compression ratio denotes that the original test data size is increased.

In the experimental results, it is noted that, in most cases, compression is improved by applying our technique to the various coding schemes for MTC-filled test data and then confirmed that significant reduction in both test data volume and scan test power consumption can indeed be achievable simultaneously.

## IV. 결 론

In this paper, a new test compression/ decompression technique is introduced to reduce test data volume and scan test power consumption, simultaneously. First, the don't-cares of the pre-computed scan test data are mapped to logic values to minimize transitions during scan shifting thereby to reduce test power, and next the low-power scan test data is transformed to improve compression efficiency by using NB-XOR technique which results in skewed data containing a lot of 0s. Finally, the transformed test set can be significantly compressed by various coding schemes which can exploit the test data highly biased to 0s. In the experimental results, considerable reduction in test data volume is achieved by applying our method to various coding schemes. Consequently, our technique provides a base work to improve the compression for low-power scan test data.

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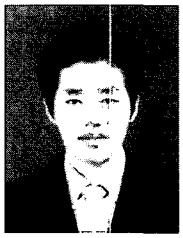

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