IEEE802.11p 기반의 OFDM-DSRC 통신을 위한 임베디드 시스템 구현

곽재민*

Implementation of Embedded System for IEEE802.11p based OFDM-DSRC Communications

Jae-Min Kwak*

요 약

본 논문은 IEEE802.11p 기반의 OFDM-DSRC 통신을 위한 임베디드 시스템의 구현에 대한 것이다. IEEE802.11p 표준의 물리계층 규격에 대해 먼저 설명하고, 규격에 따른 모뎀의 BER 성능을 시뮬레이션을 통해 평가하고, 본 논문에서 구현한 시스템 구조와 설계방식, 구현 결과에 대해 설명한다. OFDM-DSRC 통신을 위해 구현한 임베디드 시스템은 FPGA, 플래쉬 메모리, ARM9 CPU 및 기타 주변장치들로 구성하였다. 구현 결과로부터, 본 논문에서 구현한 IEEE802.11p를 따르는 OFDM-DSRC 시스템이 정상적으로 동작함을 확인하였다. 구현한 IEEE802.11p에 따른 임베디드 시스템에 대한 최적화를 통해 ITS와 같은 무선 통신 응용 시스템에 적용할 수 있을 것으로 예상된다.

ABSTRACT

In this paper, embedded system implementation for IEEE802.11p based OFDM-DSRC is presented. After the IEEE802.11p physical layer specification is introduced and BER performance of the modem is evaluated by simulation, implementation aspects of the system such as system architecture, design method and implementation results are addressed. Implemented embedded system for the OFDM-DSRC communication consists of FPGA, flash memory, ARM9 CPU Core, peripherals, etc. From the results, it is shown that the implemented system operates well according to IEEE802.11p specification. It is expected that implemented embedded system shall be used for wireless communication system such as ITS application by enhancing system optimizing.

키워드

Embedded System, OFDM, DSRC, IEEE802.11p

Ⅰ. INTRODUCTION

DSRC (Dedicated Short Range Communication) system is important communication service that serves as wireless infrastructure supporting various functions such as electronic toll collection, traffic management, etc. But conventional 1Mbps ASK based DSRC in Korea shows capacity limitation for supporting various ITS(Intelligent Transport Systems) requirement including contents downloading, wireless internet, etc. To accommodate higher data rate requirement in ITS service, a subcommittee of ASTM(American Society of Testing and Materials) E17.51 selected IEEE802.11a and R/A (Roadside Applications) as the preferred physical layer for DSRC based communication between vehicle to vehicle or

* 전자부품연구원

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vehicle to road side unit [1]. FCC allocated 5.850-5.925GHz band as for OFDM based DSRC system, and standardization work is now being developed in IEEE802.11p task group. IEEE802.11p task group is creating the standard of 5.9GHz band OFDM based DSRC system. That is to say, project IEEE802.11p is defining enhancements to 802.11 required to support ITS(Intelligent Transport System) applications. The project scope includes data exchange between high-speed vehicles and between these vehicles and the roadside infrastructure in the licensed ITS band of 5.9GHz [2].

At first, we overview the specification of IEEE802.11p physical layer specification and the performance of the system is evaluated through high level simulation. The performance of OFDM-DSRC system according to frame structure defined in the IEEE802.11p physical layer standard is evaluated in AWGN channel and fading channel. Then, we describe the implemented IEEE802.11p based embedded system for OFDM-DSRC communication.

The embedded system for IEEE802.11p based OFDM-DSRC communication basically comprise FPGA for base band modem, ADC/DAC for RF interface, CPU for modem control, SDRAM for information data storage, and flash memory for firmware program storage, and so on. These design methods of the system was described and system operation verification results are shown. Finally, summary and future works are described.

Ⅱ. IEEE802.11p based OFDM-DSRC System

2.1. IEEE802.11p Overview

IEEE802.11p based DSRC physical layer is the extension of IEEE802.11a physical layer. That is, the system structure and frame format are the same as IEEE802.11a PHY standard. However it uses only 10MHz frequency bandwidth and the frequency band used is 5.850~5.925GHz [3].

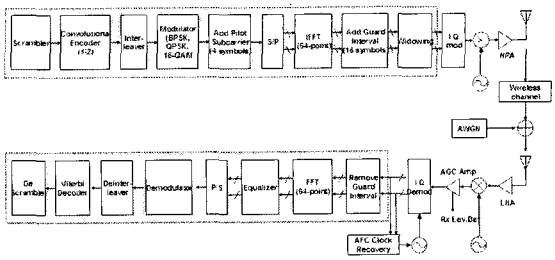

Figure 1. IEEE802.11p physical layer system model

Figure 1 shows the block diagram of IEEE802.11p physical layer system model. In the transmitter part input data is scrambled, convolution encoded, interleaved, and subcarrier modulated. In the transmission process, according to data rate, unique code rate, interleaver size, and modulation mode are allocated. It defines data rates of 3, 4.5, 6, 9, 12, 18, 24, and 27Mbps in which 3, 6, and 12Mbps are mandatory data rate.

Table 1. System parameters according to data rate

Data Rate [Mbps]	Modulation Scheme	Code Rate	Coded Bits/ subcarrier	Data bits/ OFDM symbol
3	BPSK	1/2	1	24
4.5	BPSK	3/4	1	36
6	QPSK	1/2	2	48
9	QPSK	3/4	2	72
12	16QAM	1/2	4	96
18	16QAM	3/4	4	144
24	64QAM	2/3	6	192
27	64QAM	3/4	6	216

Table 1 shows the system parameters according to data rate. For mandatory data rates, code rate of convolutional code is set to only 1/2.

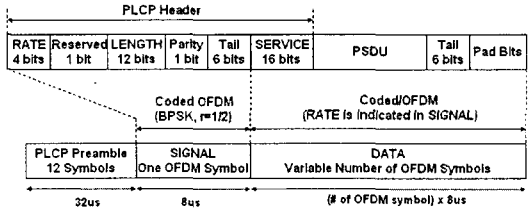

Figure 2. PPDU frame format of IEEE802.11p physical layer

Figure 2 shows frame format which consists of OFDM PLCP(Physical Layer Convergence Protocol) preamble, PLCP header, PSDU(PLCP Service Data Unit), Tail bits, and Pad bits. In the PLCP header, RATE, Reserved, LENGTH, Parity, Tail bits are SIGNAL field of one OFDM symbol, which is transmitted only in rate 1/2 coded BPSK modulation for higher communication performance. SERVICE, PSDU, Tail, Pad bits are defined as DATA which is transmitted according to data rate indicated by RATE of header.

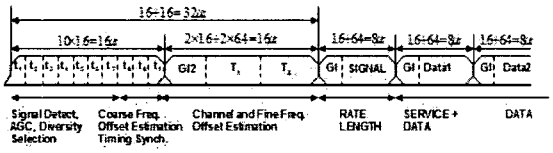

Figure 3. PLCP preamble structure

In the PLCP preamble field shown in figure 3, we can see total preamble period is 32us and it consists of 10 short training symbols and 2 long training symbols. Short training symbol is used for coarse frequency offset estimation and long training symbol is for fine frequency offset estimation.

2.2 Channel Model & Simulation Setup

Using high level simulation tool, Matlab, the performance of IEEE802.11p based OFDM-DSRC system according to frame format is evaluated under AWGN and frequency selective fading channel considering vehicular environment.

Table 2. Simulation channel for modified HIPERLAN/2 model D profile

Tap Number	Delay (ns)	Average Relative Power(dB)	Ricean factor	Doppler Spectrum
1	0	0.0	10	Class+spike
2	100	-1.55	0	Class
3	200	-3.54	0	Class
4	300	-7.03	0	Class
5	400	-8.98	0	Class
6	500	-14.29	0	Class
7	600	-15.80	0	Class
8	700	-inf	0	Class
9	800	-19.59	0	Class
10	900	-22.68	0	Class
11	1000	-inf	0	Class
12	1100	-27.70	0	Class

We designed the channel model for simulation which is time variant frequency selective fading model. For performance evaluation we modified HIPERLAN/2 channel simulation model D delay profile. HIPERLAN/2 channel model is tapped delay line type of channel model basically described in [4],[5]. Original model D corresponds to LOS conditions in a large open space indoor or outdoor environment and its rms(root mean square) delay spread is about 140ns. Modified model D profile is shown in table 2.

We designed high level simulation model of IEEE802.11p physical layer for performance simulation. Simulation setup is as shown in Table 3. System bandwidth is set to 10MHz and subcarrier spacing is 156.25KHz. For mobile application, modified HIPERLAN/2 channel is used and vehicle velocity is set to 100Km/h. In the channel maximum and rms delay is about 1100ns and 242 ns, respectively.

Table 3. Simulation setup

Simulation Parameter	Value
Modulation/data rate	QPSK/6Mbps
Constraint length	7
Trellis depth	34
Vehicular speed	100Km/h(546hz)
Rms delay spread	242ns
Center frequency	5.9GHz
Eb/No	15dB
Data length per frame	50~500 bytes

III. Implementation of IEEE802.11p based OFDM-DSRC Platform

The OFDM-DSRC communication test platform consists of high-capacity FPGA, two 8-bit ADC, two 10-bit DAC, octal buffers, and a few analog devices such as OP amplifiers. Although the used ADC/DAC resolution is 12bits, we used limited resolution 8bit for ADC and 10bit resolution for DAC. The figure 4 shows the OFDM-DSRC system platform for the evaluation.

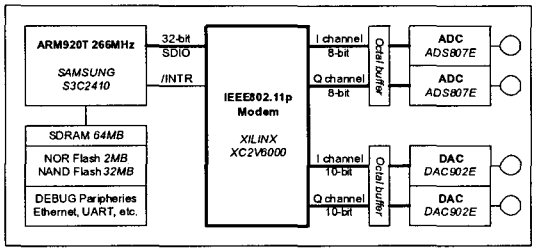

Figure 4. The hardware block diagram of the OFDM-DSRC platform

The IEEE802.11p based OFDM-DSRC modem logic was programmed in the target FPGA XILINX Virtex2 device ofthe high capacity FPGA for evaluation. Virtex2 family supports various solutions for networking, communication, and DSP applications [6]. We designed IEEE802.11p physical layer modem using VHDL, which is synthesized and implemented in Xilinx ISE 6.3. Target device is XC2V6000 -6 FF1152 which includes 33,792 slices, 144 multiplier, and 144 RAM blocks. Implemented IEEE802.11p modem is operates in 20MHz clock speed. The figure 5 is the synthesized top block circuit of the OFDM-DSRC modem logic.

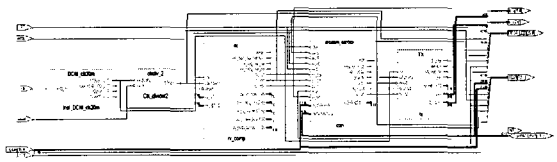

Figure 5. The IEEE802.11p physical layer block diagram

The OFDM-DSRC modem logic communicates with the ARM9 RISC processor through the 32-bit SDIO interface; the modem_control block in the figure 5. The data from the modem_control is stored in the FIFO of the Tx block and the data includes the length and the command in addition to the physical PDU. The Tx block modulates the data as defined in IEEE802.11p specification; scrambled, coded, interleaved, modulation mapped, pilot inserted, IFFT processed, and transmitted. The Rx block demodulates the received I/Q OFDM signal, FFT processed, equalized, pilot removed, modulation de-mapped, de-interleaved, decoded, descrambled, etc. Then, it moves the de-modulated data to the FIFO. As soon as the modem_control block receives the data, the reception interrupt is emerged.

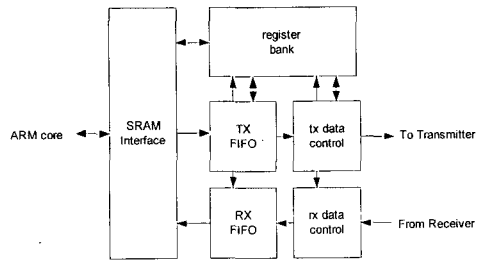

Figure 6. The block diagram of modem_control block

The figure 6 illustrates the brief block diagram of modem_control block. The modem_control block consists of SRAM interface, Tx FIFO, Rx FIFO, register bank, tx data control and rx data control. Input data format of IEEE802.11p based OFDM-DSRC transmitter is 1-bit serial stream and receiver output is the same that. But SRAM interface is 32-bit parallel interface. Tx data control and rx data control convert data from 32-bit parallel form to 1-bit serial form.

Tx data control operation starts when receiving start signal from register bank. First 40 bits located in two word of Tx FIFO always contain information of 4bit data rate, 1bit reserved bit, 12bit data length in octet, even parity bit, 6bit tail, and 16bit service field. As soon as reading data length information from Tx FIFO, tx data control calculates total bit length to be transmitted. According to transmitter serial interface, data read in word is changed to serial bit stream in tx data control and counter value of total bit length are fed to transmitter with decreasing total bit length by one. If total bit length becomes zero, the register bank generates interrupt signal to ARM core indicating that transmission being completed so that ARM prepare for another transmission packet data. Rx data control operates in the reverse procedure of Tx data control block.

The register bank has control registers, command registers, status registers of IEEE802.11p based OFDM-DSRC and FIFOs. By reading status registers in register bank, ARM core can be known that Tx/Rx data control are busy or not, TX/RX FIFO status are empty, almost empty,

almost full, or full. Also it can obtain the information about current write point address and current read point address for reliable FIFO control.

The communication test software was implemented for the verification of transmission and reception on the OFDM-DSRC embedded hardware platform as shown in the figure 7. In the figure 7, the platform A initiates the test data and transmits it to the platform B. The data is converted into the OFDM digital bit-stream by the Tx block of the OFDM-DSRC modem. The data is also changed into the OFDM analog signal by the analog circuit of the OFDM-DSRC platform. On receiving the data, the platform B copies it into the FIFO of the Tx block and transmits it promptly and then the platform A receives the echoed data and compares the source data with the received data. Finally, the platform A verifies the communication function on the AD/DA analog connection. In the hardware and software experiment, it was shown that there was not any packet error while testing 200 repetitive packet message communication.

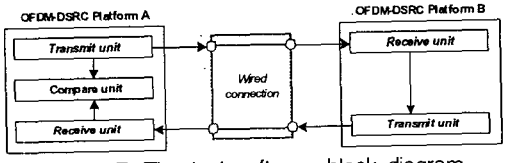

Figure 7. The test-software block diagram

Ⅳ. Results

Figure 8 shows BER performance of the IEEE802.11p high level simulation model. The simulation setup is as shown at the table 3.

This curve shows system BER performance according to packet length under AWGN and doppler fading channel. In the condition of target BER of 10^{-3}, for OFDM-DSRC communication, packet length must be less than approximately 125bytes for 100Km/h vehicle speed.

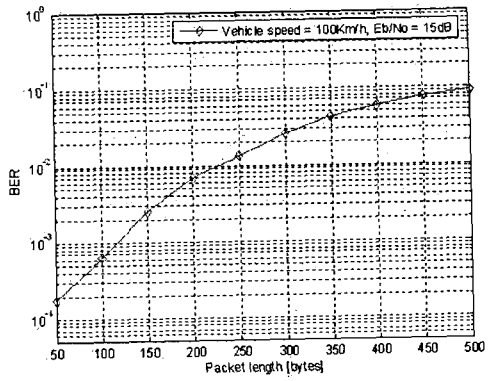

Figure 8. BER evaluation of IEEE802.11p physical layer by simulation (Eb/No=15dB)

Figure 9 shows implemented platform board for evaluation of IEEE802.11p based OFDM-DSRC system. As mentioned in chapter 3, major components of the implemented platform are Samsung ARM9 RISC processor, 2MB NOR flash memory, 128MB SDRAM, Xilinx Vertex2 FPGA, octal buffers, TI ADS807 12bit 53Msps A/D converters, and TI DAC902 12bit 165Msps D/A converters.

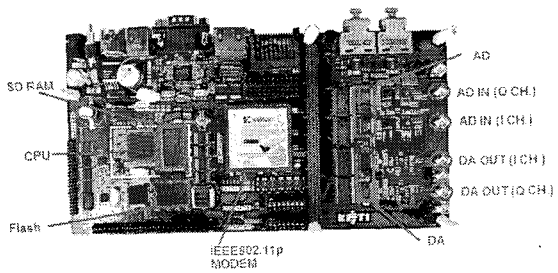

Figure 9. Implemented Test Platform for IEEE802.11p based OFDM-DSRC

Figure 10 shows functional simulation results for modem test using modelsim. In the figure, transmitted OFDM signal(tx_i : I channel, tx_q : Q channel) with 10 bits resolution is shown, in which first part is preamble and signal field and data field follows. We have confirmed that signal rx_out of final receiver part output data is the same as transmitter input data.

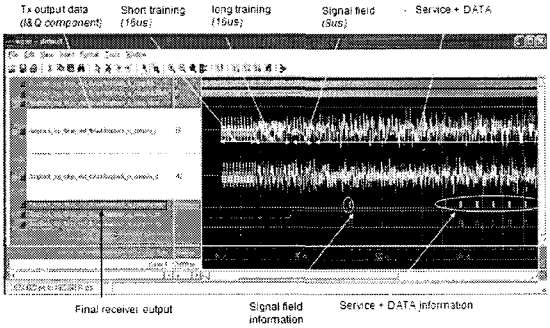

Figure 10. Functional simulation results with modelsim simulator

The physical layer IEEE802.11p modem is targeted to XC2V6000 -6 FF1152 using Xilinx ISE 6.3 tool. The results are that all modules of modem requires about less than 20%. The timing reports show no timing conflict in the modem circuit. Maximum frequency estimated is about 35MHz, which is higher frequency than 20MHz that is used as clock speed in the designed FPGA modem. Related area and timing results are shown at table 4 and 5.

Table 4. Area results

Area metrics for a XC2V6000 -6 FF1152 device		
Parameter	Used	%
Number of slices	7562	22
Number of slice flip flops	6457	9
Number of 4 input LUTs	11951	17
Number of bonded IOBs	99	12
Number of BRAMs	22	15
Number of GCLKs	2	12

Table 5. Timing results

Timing metrics for a XC2V6000 -6 FF1152 device	
Parameter	Time (ns) Frequency (MHz)
Minimum period	28.440
Maximum frequency	35.162
Minimum input arrival time before clock	10.623
Maximum output required time after clock	13.015

V. Conclusion

In this paper we presented the design, validation and implementation of embedded system for IEEE802.11p based OFDM-DSRC system. At first, we designed high level simulation model for modem simulation, and showed that the system BER performance under the AWGN and time varying frequency selective fading channel. The system implementation work was performed using high level simulation tool like Matlab, hdl functional simulator like modelsim, and implementation tool like Xilinx ISE. The implemented system consists of ARM9 core, flash memory, FPGA, SDRAM, flash memory, AD/DA, etc. Test results show that transmitter connected receiver via AD/DA communicates each other with no error. It is expected that implemented embedded system shall be used for wireless communication system such as ITS application by enhancing h/w efficiency optimizing.

Our future works shall be IEEE802.11p MAC design and enhancement of current physical layer chip in the point of area and speed optimization for realizing high performance IEEE802.11p based OFDM-DSRC system.

Reference

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저자소개

곽 재 민(Jae-Min Kwak)

1998년 2월 한국항공대학교 통신정보공학과 (공학사)

1999년 8월 한국항공대학교 대학원 통신정보공학과 (공학석사)

2002년 8월 한국항공대학교 대학원 통신정보공학과 (공학박사)

2002년 7월~2003년 7월 한국전자통신연구원 네트워크 연구소 (Post-doc.)

2003년 7월~현재 전자부품연구원 SoC연구센터 (선임연구원)

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