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A Three Phase Three-level PWM Switched Voltage Source Inverter with Zero Neutral Point Potential

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ABSTRACT

A new three phase three-level Pulse Width Modulation (PWM) Switched Voltage Source (SVS) inverter with zero neutral point potential is proposed. It consists of three single-phase inverter modules. Each module is composed of a switched voltage source and inverter switches. The major advantage is that the peak value of the phase output voltage is twice as high as that of a conventional neutral-point-clamped (NPC) PWM inverter. Thus, the proposed inverter is suitable for applications with low voltage sources such as batteries, fuel cells, or solar cells. Furthermore, three-level waveforms of the proposed inverter can be achieved without the switch voltage imbalance problem. Since the average neutral point potential of the proposed inverter is zero, a common ground between the input stage and the output stage is possible. Therefore, it can be applied to a transformer-less Power Conditioning System (PCS). The proposed inverter is verified by a PSpice simulation and experimental results based on a laboratory prototype.

Keywords: multi-level inverter, switched voltage source

1. Introduction

In recent years, industry has begun to demand higher power equipment. Multi-level inverters have been attracting increasing attention for power conversion in high-power applications due to their lower harmonics, higher efficiency, and lower voltage stress compared to two-level inverters. Numerous topologies for multi-level inverters have been introduced and widely studied[1-5]. The most important of these topologies, as shown in Fig. 1, are the diode-clamped (neutral-point-clamped) inverter[6], the capacitor-clamped (flying capacitor) inverter[7], and the cascaded H-bridge inverter with separated DC sources. In the diode-clamped inverter, the circuit proposed by Nabae et al in 1981, as shown in Fig. 1(a), the DC-bus voltage is split into three-levels by two series-connected bulk capacitors, and two diodes clamp the switch voltage to half of the level of the DC-bus voltage. The output voltage v_{UN} has three states: $V_{dc}/2$, 0, $-V_{dc}/2$. It is noted that although the output voltage v_{UN} is alternating current (AC), v_{UG} has a direct current (DC) component. Therefore, the difference between v_{UN} and v_{UG} is the voltage across C_2, which is $V_{dc}/2$. Two series-connected switches of the diode-clamped inverter can achieve the multi-level output waveforms and reduce the voltage stress to half of the input voltage. However, in this circuit, the static and dynamic sharing of the voltage across the switches is quite difficult. Furthermore, the diode-clamped inverter has undesirable features such as fluctuation of the neutral

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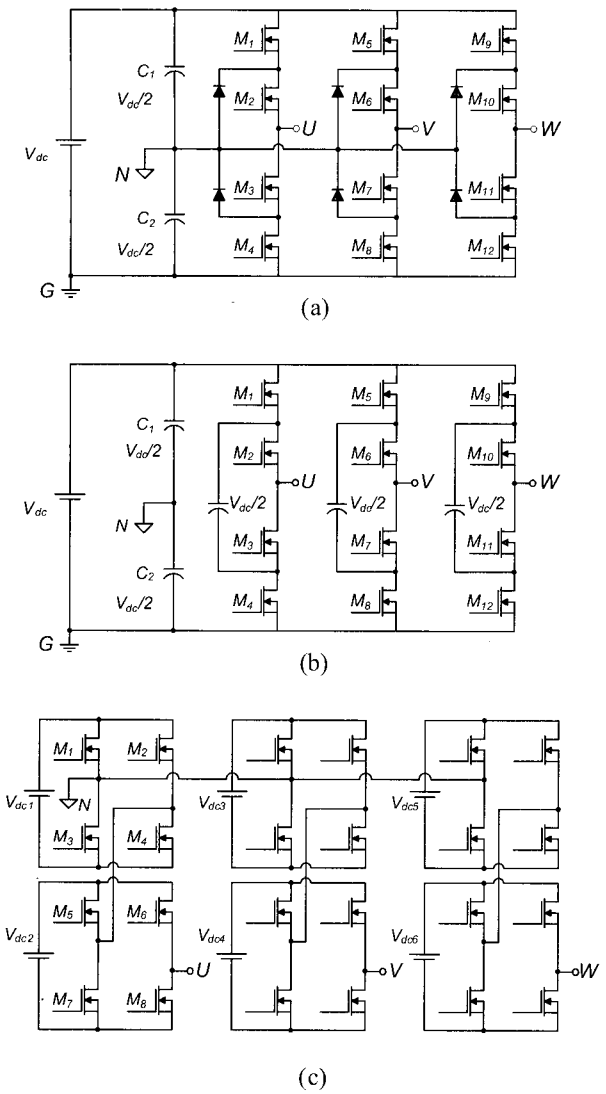

Fig. 1 The major topologies of multilevel inverters
(a) diode-clamped inverter (b) capacitor-clamped inverter (c) cascaded H-bridge inverter

point voltage due to a difference of the switching characteristics and over voltage problems across the inner switching devices. Meynard et al proposed a multilevel structure where the device off state voltage clamping was achieved by using clamping capacitors rather than clamping diodes as shown Fig. 1(b)[7]. Although this topology solves the problem of static and dynamic sharing of the voltage across the switches, it still has the voltage imbalance problem of the diode-clamped inverter and DC offset voltage of the output. The cascaded H-bridge inverter shown in Fig. 1(c) is an alternative approach to achieve multilevel waveforms based on the series connection of full-bridge inverters with a multiple isolated DC bus. Although the modular structure solves the voltage imbalance problem, this approach requires many isolated DC sources and link voltage controllers.

To solve all of these drawbacks of conventional multi-level inverters, a new three-level PWM Switched Voltage Source (SVS) inverter is proposed. Fig. 2 shows the circuit configuration of the proposed three-level PWM SVS inverter. It consists of three single-phase inverter modules. Each module is composed of a main inverter stage and a switched voltage source stage which includes two switches, one flying capacitor, one diode and a small snubber inductor as shown in Fig. 3. It provides a three-level output across U and N, i.e., v_{UN}=V_{dc}, 0, or $-V_{dc}$. Therefore, the peak value of the phase voltage is V_{dc}, and the peak value of the line to line voltage is $2V_{dc}$. Since the phase voltage of the SVS inverter is twice as high as that of the conventional NPC inverter, it is well suited for an inverter with low input voltage such as a fuel cell, battery, or solar cell. In addition, the SVS inverter does not have the voltage imbalance problem [4] which often occurs in conventional three-level inverters with a divided input source. Furthermore, since the DC offset of the output phase voltage is zero, the neutral point of the output load stage can be connected to the ground, and the SVS inverter is safe without an electrical isolation. Therefore, it can easily be applied to a transformer-less power conditioning system.

2. Operational principles

2.1 Circuit operation

The circuit configuration of the three-level PWM SVS inverter consists of three single-phase inverter modules as shown in Fig. 2. Each module can be independently operated with a single input source. The basic operational modes of the SVS inverter are shown in Fig. 3 and Fig. 4. Since the flying capacitor C_1 is charged to input voltage V_{dc} when the switch M_1 turns on, voltage across C_1 can be assumed to be a constant voltage source V_{dc}, and snubber inductor L_1 can be ignored. As can be seen in Fig. 3, the voltage of node A can be changed to input voltage V_{dc} and 0V by switch M_1 and M_3, respectively. The difference

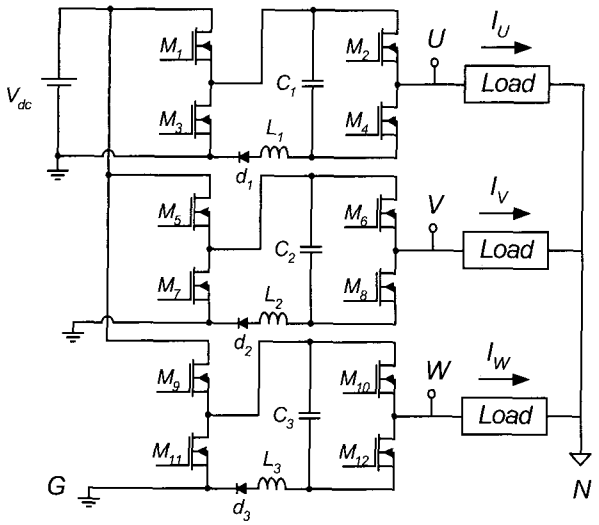

Fig. 2 Circuit diagram of the proposed SVS inverter

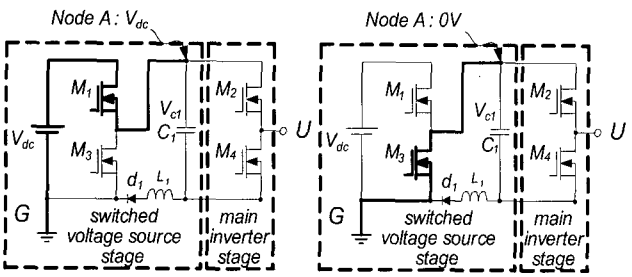

Fig. 3 Operational principles of the switched voltage source

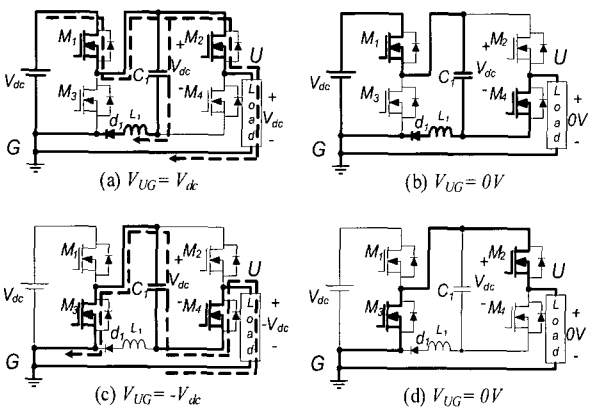

Fig. 4 Operational modes of the three-level SVS inverter

between node A and U is 0 and $-V_d$ by switch M_2 and M_4, respectively, as shown in Fig. 4. Therefore, the SVS inverter has four different cases and three states of the output terminal voltage v_{UG}: V_{dc}, 0, and $-V_{dc}$ which are twice those of the conventional NPC inverter. Furthermore, v_{UG} does not have a DC component.

Case 1 (Fig 4. (a)): The output voltage v_{UN} is V_{dc} and C_1 is charged to V_{dc}, when switches M_1 and M_2 turn on. The snubber inductor limits the inrush current of M_1 when the voltage of C_1 is different from V_{dc}.

Case 2 (Fig 4. (b)): The output voltage v_{UN} is 0V when switches M_1 and M_4 turn on.

Case 3 (Fig 4. (c)): When switches M_3 and M_4 turn on, the diode d_1 turns off. In addition, the output voltage v_{UN} is clamped to $-V_{dc}$ and the flying capacitor C_1 is discharged.

Case 4 (Fig 4. (d)): The output voltage v_{UN} is 0 and diode d_1 is off, when switches M_3 and M_4 turn on.

The same analysis can also be applied to the other modules.

2.2 PWM signal generation

To generate the three-level PWM waveform, the sine-triangular PWM method[10, 11] is used. The sine-carrier PWM is generated by comparing the three reference control signals with two triangular carrier waves. Three reference sinusoids are 120° apart to produce a balanced three-phase output, and the corresponding output signals for a three-level PWM can be expressed as

$$v_{xN} = \begin{cases} V_{dc} & \text{for } V_{ref,x} > V_{tri,1} \\ 0 & \text{for } V_{tri,1} > V_{ref,x} > V_{tri,2} \\ -V_{dc} & \text{for } V_{ref,x} < V_{tri,2} \end{cases} \quad (1)$$

where, $x = U, V, W$.

For the first module, the reference signal, two triangular carrier waves, and corresponding switch gate signals are shown in Fig. 5. When the reference signal is positive, switch M_1 turns on and switch M_3 turns off as shown in Fig. 4 (a) and (b). In this mode, switch M_2 turns on when the instantaneous value of the reference signal is larger than the triangular carrier ($V_{tri,1}$), and switch M_4 turns on when the instantaneous value of the reference signal is less than the carrier ($V_{tri,1}$). When the reference signal is negative, switch M_4 turns on and switch M_2 turns off as shown in Fig. 4 (c) and (d). In this mode, switch M_1 turns on when the instantaneous value of the reference signal is less than carrier ($V_{tri,2}$), and switch M_3 turns on when the instantaneous value of the reference signal is larger than carrier ($V_{tri,2}$).

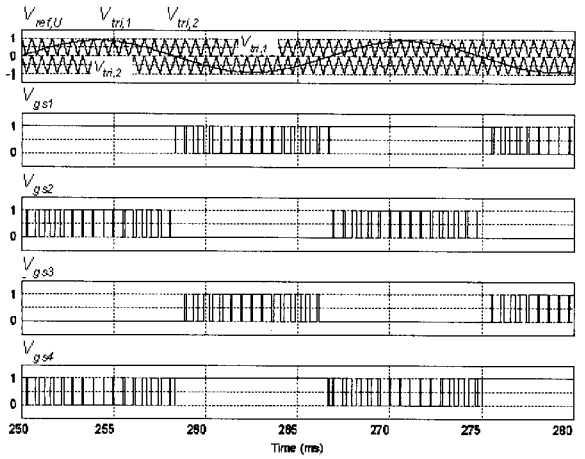

Fig. 5 Gate signals of one of three modules

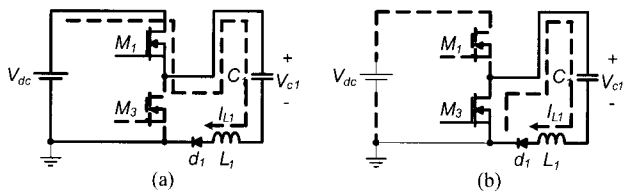

Fig. 6 Operation of the SVS inverter
(a) powering mode (b) freewheeling mode

3. Analysis of the proposed inverter

In the preceding section, the voltage across capacitor C_1 of the switched voltage source (SVS) stage shown in Fig. 2 was assumed to be a constant voltage source V_{dc}. However, the voltage across the capacitor C_1, V_{C1} is slightly different from the input voltage source V_{dc}. The difference between the voltage across the capacitor C_1 and the input voltage source V_{dc} may cause an inrush current on the switch M_1 and diode d_1 when the switch M_1 turns on. To solve this problem, a small snubber inductor L_1 is inserted between the diode d_1 and capacitor C_1. However, this small snubber inductor does not affect the operation of the proposed SVS inverter. The effect of the small snubber inductor L_1 is considered in this section.

Fig. 6 shows the circuit operation when $V_{ref,1}<V_{tri,2}$, and Fig. 7 shows the buck circuit. The SVS stage shown in Fig. 2 is operated as a buck converter as seen in Fig. 6 and Fig. 7. Therefore, to analyze the operation of the SVS stage according to the value of the inductor, the simple buck converter must be considered. If the snubber inductor L_1 is

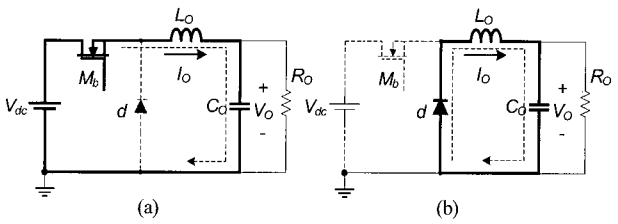

Fig. 7 Buck converter
(a) powering mode (b) freewheeling mode

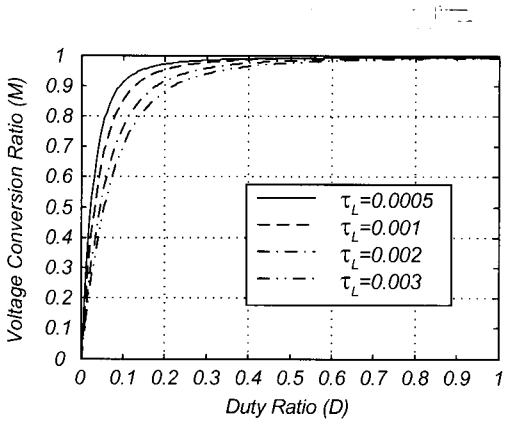

Fig. 8 Voltage conversion ratio in the DCM buck converter

small, the buck converter operates in Discontinuous Conduction Mode (DCM). When the buck converter is operated in DCM, its voltage conversion ratio is expressed as

$$M=\frac{V_o}{V_{dc}}=\frac{2}{1+\sqrt{1+\frac{8\cdot\tau_L}{D^2}}} \tag{2}$$

where $\tau_L=(L_o/R_o\cdot T_s)=L_o\cdot I_o/(V_o\cdot T_s)$
T_s=switching period, D=duty ratio
R_o=load resistance.

Based on this equation, the voltage conversion ratio M can be plotted as shown in Fig. 8. This figure shows that the less inductance can make the voltage conversion ratio M close to the unity for a wide range of the duty ratio. In the case of the laboratory prototype, the modulation index m_a is less than 0.8, and the duty ratio of the switch M_1 is greater than 0.2 as shown in Fig. 9. Also, the parameter τ_L is about 0.0005, and the voltage conversion ratio M at D=0.2 is 0.976. This means that the difference between the voltage across the capacitor C_1 and the input voltage source V_{dc} is 2.4%. Therefore, V_{C1} can be assumed to be a

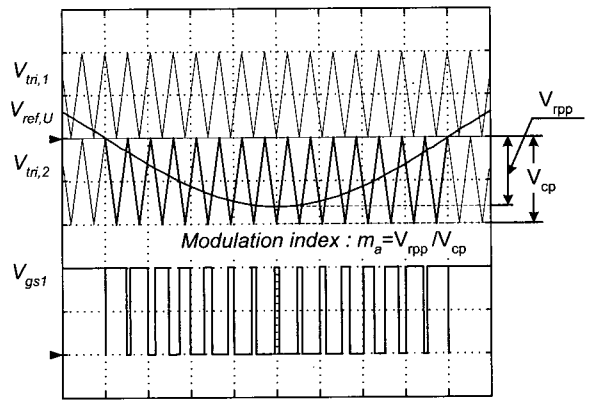

Fig. 9 Gate signal of switch M_1

voltage source charged with V_{dc}. In addition, the design equation of L_1 can be derived from (2) and expressed as

$$L_1 = R_o \cdot T_s \cdot \frac{D^2}{8} \cdot \left\{ \left(\frac{2}{M} - 1 \right)^2 - 1 \right\} \quad (3)$$

$$= \frac{V_{c1}}{I_{L1}} \cdot T_s \cdot \frac{(1-m_a)^2}{8} \cdot \left\{ \left(\frac{2}{M} - 1 \right)^2 - 1 \right\} \quad (4)$$

where T_s=switching period, D=duty ratio
R_o=load resistance, m_a=modulation index.

If the rated output voltage, the rated output current, and the allowed error of the output voltage are known, the proper value of inductance L_1 and modulation index m_a can be determined from (4).

4. Applications consideration

The SVS inverter has three important advantages compared to the NPC inverter. First, the output phase voltage is twice as high as that of the NPC inverter. This means that the SVS can generate twice the output power. Second, the DC offset voltage of the output is zero. This makes the power system more reliable and safer. This is very important especially for high power applications. Finally, the SVS inverter has no voltage imbalance problem. It can make the control algorithm simple to drive motor. These advantages for some applications are considered in the following section.

4.1 Motor drive system

Conventional two-level PWM inverters and multilevel

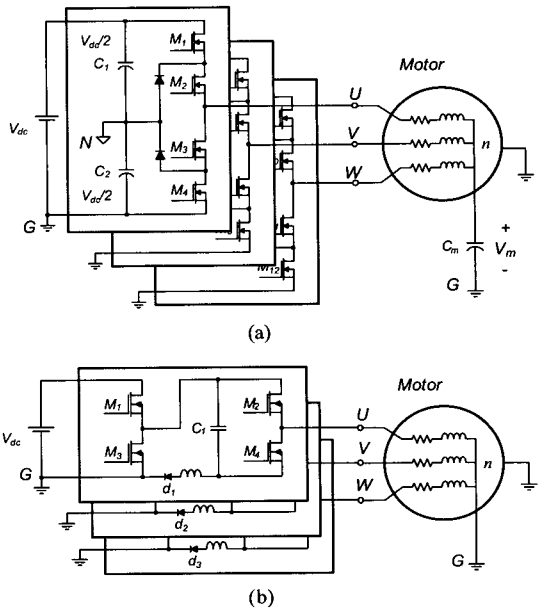

Fig. 10 Motor drive systems (a) NPC inverter (b) SVS inverter

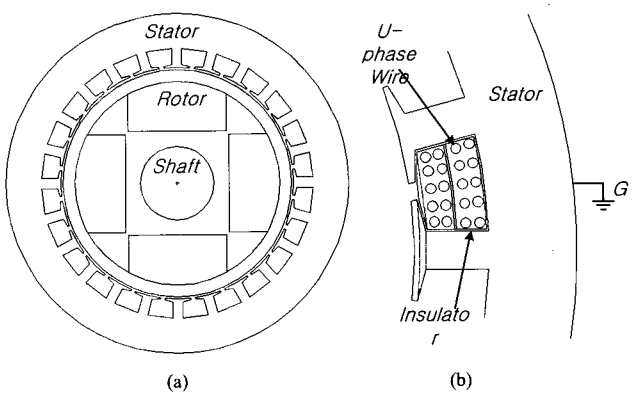

Fig. 11 PMSM (a) Structure of PMSM (b) Structure of stator

PWM inverters generate common-mode voltage or a "neutral shift effect" within the motor windings. This common mode voltage may build up the motor shaft voltage through electrostatic couplings between the rotor and the stator windings and between the rotor and the frame [12]. Moreover, since the conventional inverters have DC offset voltage between ground and motor neutral point n as shown in Fig. 10 (a), the common mode voltage becomes higher and the motor line-to-ground voltage may be much higher than its rated line-to-neutral (phase) voltage. Therefore, the transformerless design of the drive with the conventional PWM inverter may cause a much larger common-mode leakage current to flow into the

ground [12] and cause a high voltage stress on motor insulation life [13, 14]. Although the isolation transformer can solve these problems, it increases the cost and reduces the efficiency of the drive, which is undesirable, especially for high-power systems.

In the case of the proposed SVS inverter, the neutral point of the motor stator windings can be grounded as shown in Fig 10 (b), and the motor line-to-ground voltage is identical to its phase voltage. Therefore, the "neutral shift effect" disappears, and as long as the motor phase voltage is kept within its rated value during operation, the motor insulation will not be deteriorated.

For example, a 400V input voltage source can generate

Table 1 Comparison of NPC Inverter and SVS Inverter with Same Output Power

	NPC Inverter	SVS Inverter
Input Voltage (V_{dc})	400V	200V
Phase Voltage (V_{UN})	-200V, 0V, 200V	-200V, 0V, 200V
V_{UG}	0V, 200V, 400V	-200V, 0V, 200V
Voltage Stress of Insulator	400V	200V
Problems	Voltage Unbalance	.

Table 2 Comparison of NPC Inverter and SVS Inverter with Same Input Voltage Source

	NPC Inverter	SVS Inverter
Input Voltage(V_{dc})	400V	400V
Phase Voltge(V_{UN})	-200V, 0V, 200V	-400V, 0V, 400V
V_{UG}	0V, 200V, 400V	-400V, 0V, 400V
Voltage Stress of Insulator	400V	400V
Problems	Voltage Unbalance	.

200V of the peak value of the phase voltage in the NPC inverter and a 200V input voltage source can generate 200V of the peak phase voltage in the proposed SVS inverter as shown in TABLE I. In this case, the phase voltages are the same. However, the maximum line-to-ground voltages of the NPC inverter are twice as high as those of the SVS inverter due to the DC offset voltage of the output. Since the motor stator is grounded, the line-to-ground voltage is the voltage stress of the motor insulator as shown in Fig. 11. Therefore, the voltage stress of the motor insulator in the NPC inverter is twice as high as that of the SVS inverter.

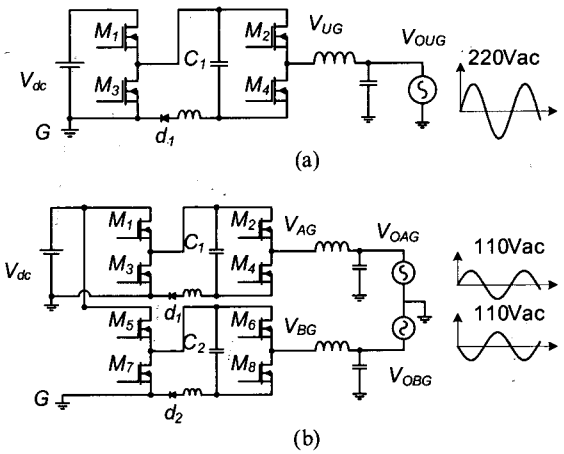

Fig. 12 PCS (a) single phase 2-line type (b) single phase 3-line type

In the case of the same input voltage source, the output phase voltage of the SVS inverter has twice as high as that of the NPC inverter as shown in TABLE II. In this case, the output voltage of the SVS inverter is twice as high as that of the NPC inverter. However, the voltage stress of the motor insulator is the same. Therefore, since the output current of the SVS inverter is half of that of the NPC inverter with the same output power, the proposed SVS inverter has less conduction loss and higher efficiency than the NPC inverter. Thus, since the proposed SVS inverter has desirable features such as high reliability, high efficiency, and high safety, it is expected that the proposed SVS inverter is well suited for use in motor drive systems.

4.2 Power conditioning system

Recently, the importance of distributed energy generation and renewable energy sources (e.g., solar-cell or fuel-cell applications having batteries or supercapacitors) has been increased due to the exhaustion of fossil energy. The importance of the Power Conditioning System (PCS), which efficiently transforms power from DC to AC, has also been increased. In general, renewable energy sources have low voltage sources. Therefore, to boost the voltage up to the grid levels, an additional power conversion system which consists of a DC/DC converter and transformer is required with the inverter. However, since a PCS is generally an individually owned single-phase system in the power range of up to 10kW, a PCS requires low cost, high

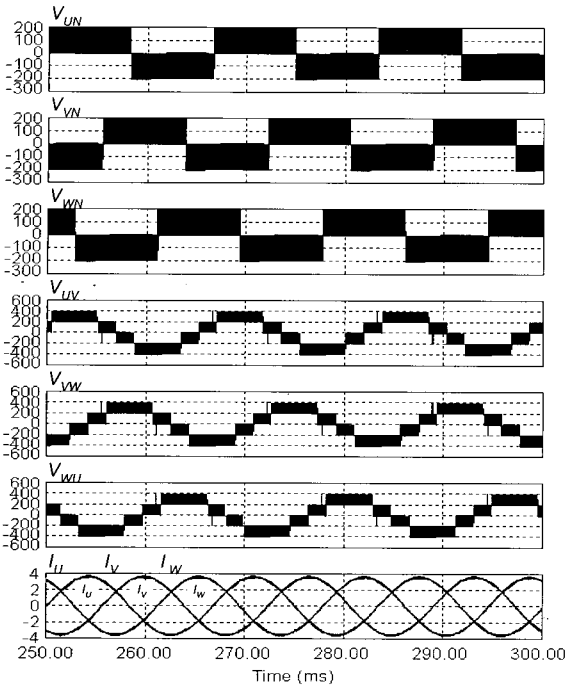

Fig. 13 Simulation results of the SVS inverter

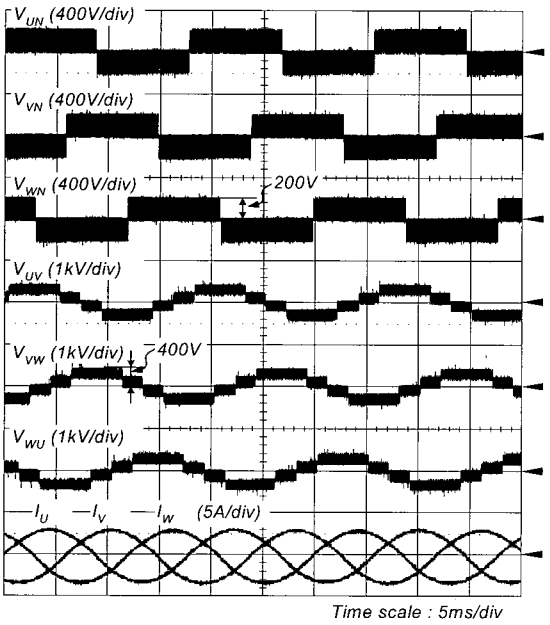

Fig. 14 Experimental results of the SVS inverter

efficiency, and reliability such as transformerless inverter. If the conventional inverter topologies which show undesirable DC offset output voltage are applied to transformerless PCS, the electrical isolation between the inverter and the grid should be considered for safety. However, since the DC offset voltage of the SVS inverter output is zero, the proposed SVS inverter can be safely applied to a transformerless PCS. Two different types of PCS example circuits are shown in Fig. 12 (a) and (b), respectively. Moreover, since the output voltage is twice as high as that of the NPC inverter, the proposed SVS inverter is suitable for applications with low input voltage sources such as battery cells, fuel cells, or solar cells. Thus, the SVS inverter is well suited for the transformerless PCS as it has many desirable features such as safety, high reliability, high efficiency, and low cost.

5. Experimental results

The operational principles of the SVS inverter shown in Fig. 2 have been investigated by Pspice simulation and experimental results. For the three-level inverter drive, the sine-triangular wave modulation scheme was used to obtain a three-level PWM pattern. The laboratory prototype with 200VDC of the input voltage and a triangular carrier wave of 9kHz frequency is employed to the 50Ω resistive load with a switching frequency LC filter. Fig. 13 and Fig. 14 show the simulated and experimental results of the phase voltages, line to line voltages, and load currents of the three-level voltage source inverter, respectively. As can be seen in Fig. 13 and Fig. 14, the peak value of the phase voltages V_{dc} is 200V and the peak value of the line to line voltage $2V_{dc}$ is 400V. These are twice as high as those of the conventional NPC inverter. Therefore, the larger amplitude of the output voltage can be obtained compared with the conventional NPC inverter and it is well suited for an inverter with a low input voltage source. Moreover, since the phase and line voltage show three and five levels, respectively, the multi-level waveform can be implemented by employing the interconnected modules without isolated DC sources or the voltage imbalance problem. Furthermore, the proposed multi-level SVS inverter can considerably reduce the voltage harmonics and output filter size. In addition, since the average value of the phase voltages to the ground during one period is zero, the neutral point can be connected to the ground and it can be applied to a transformer-less grid connected photovoltaic (PV) and fuel cell power conditioning system.

6. Conclusions

A new three phase three-level SVS inverter with zero neutral point potential is proposed. Its phase voltage and line to line voltage are twice as high as those of the conventional neutral-point-clamped PWM inverter and a three-level waveform can be achieved without the switch voltage imbalance problem. Therefore, it is well suited for an inverter with low input voltage such as a fuel cell, battery, or solar cell input. Furthermore, its average neutral point potential is zero. Therefore, the proposed SVS inverter can be widely applied to motor drive systems and transformer-less grid connected power conditioning systems.

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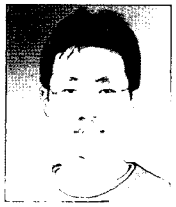

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