4H-SiC Planar MESFET for Microwave Power Device Applications

Hoon Joo Na*, Sang Yong Jung*, Jeong Hyun Moon*, Jeong Hyuk Yim*, Ho Keun Song*, Jae Bin Lee and Hyeong Joon Kim***

Abstract—**4H-SiC planar MESFETs were fabricated using ion-implantation on semi-insulating substrate without recess gate etching. A modified RCA method was used to clean the substrate before each procedure. A thin, thermal oxide layer was grown to passivate the surface and then a thick field oxide was deposited by CVD. The fabricated MESFET showed good contact properties and DC/RF performances. The maximum oscillation frequency of 34 GHz and the cut-off frequency of 9.3 GHz were obtained. The power gain was 10.1 dB and the output power of 1.4 W was obtained for 1 mm-gate length device at 2 GHz. The fabricated MESFETs showed the charge trapping-free characteristics and were characterized by the extracted small-signal equivalent circuit parameters.**

Index Terms—**SiC (Silicon Carbide), MESFET, Ion-implantation, Semi-insulating Substrate, Surface Passivation, Charge Trapping Effect, Small-Signal Equivalent Circuit**

I. Introduction

SiC is a promising material due to its superior electrical, chemical and thermal properties on the basis of the technology for producing high quality bulk substrates and epitaxial films. The high electric breakdown field, high saturated electron drift velocity, and high thermal conductivity make SiC an attractive material for high power microwave devices. 4H-SiC MESFET has the capability of high voltage, high output impedance, easy matching, and wide bandwidth through X-band. Recent progress in device process technology has demonstrated the superiority of SiC [1,2].

In this work, planar 4H-SiC MESFETs were fabricated using ion-implantation without recess gate etching to eliminate potential damage to the gate region. Ion-implantation was used to obtain a lower contact resistance [3]. The DC and RF performances of MESFETs fabricated on semi-insulating substrates were characterized. Small-signal equivalent circuit parameters were extracted using conventional models to characterize the device performance [4].

Manuscript received April 15, 2005; revised June 5, 2005.
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II. Fabrication Process

The used substrate was a semi-insulating 4H-SiC purchased from Cree, Inc., with a lightly doped, 0.55 μm-thick p-type buffer layer and a 0.3 μm-thick n-type channel layer doped at 2.79×10^{17} cm^{-3}. The fabrication process included mesa isolation, ion-implantation and activation, field oxide formation, ohmic contact formation, gate contact definition, and pad metallization. Because the cleaning of the substrate is critical for obtaining a high quality interface between SiC and the upper layer, such as a contact metal or oxide film, a modified RCA method was used to clean the substrates. To form highly doped n-type source and drain regions with a doping concentration > 10^{20} cm^{-3}, high-temperature and multiple-energy ion-implantation with phosphorous was performed. Activation of the implanted

ions was achieved by the induction heating system at 1650°C for 2 min in an Ar atmosphere. Growing a sacrificial layer is also important to passivation of the substrate surface and to obtaining a well controlled interface between the substrate and the contact metal. A thin thermal oxide layer of 200 Å-thick was grown as a sacrificial layer at 1100°C, and then a thick layer of 4000 Å-thick was deposited by plasma enhanced chemical vapor deposition (PECVD). Electron-beam evaporated Ni was used for the source and drain ohmic contacts. Post-deposition annealing (PDA) was performed at 1000°C for 2 min in an Ar atmosphere to form low resistive silicides. Gate Schottky contacts, also deposited by electron-beam evaporation, were formed using Ni followed by the formation of a capping layer of Pt, without recess etching. Electron-beam lithography was used to define the gate, and Au was used as the pad metal for electrical characterization. A SEM image of the fabricated MESFET is shown in Fig. 1.

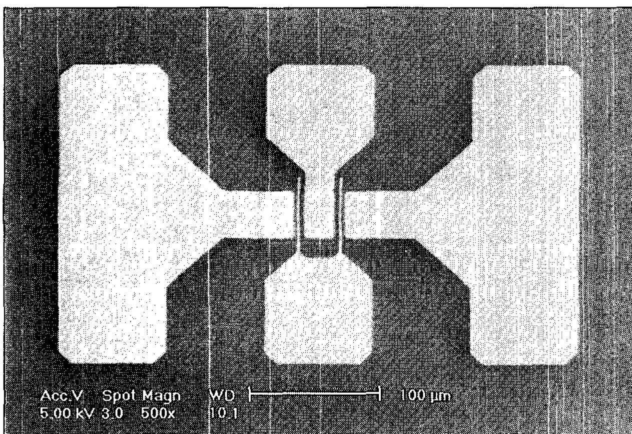


Fig. 1. SEM Images of the fabricated MESFET with a gate width of 50 µm×2

III. Experimental Results and Discussion

1. Characteristics of Fabricated MESFET

The DC characteristics of a fabricated MESFET with a gate length of 0.5 µm and a gate width of 100 µm were shown in Fig. 2. The saturation drain current was over 500 mA/mm at a drain voltage of 40 V and a gate voltage of 1.0 V. The transconductance was 41 mS/mm at a drain voltage

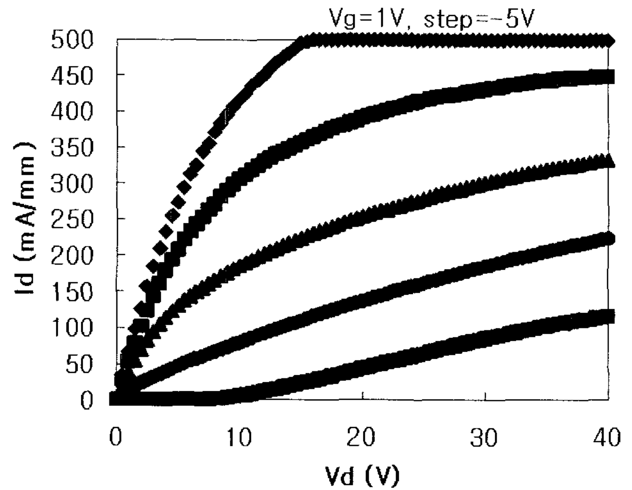


Fig. 2. DC characteristics of MESFETs with a gate length of 0.5 µm

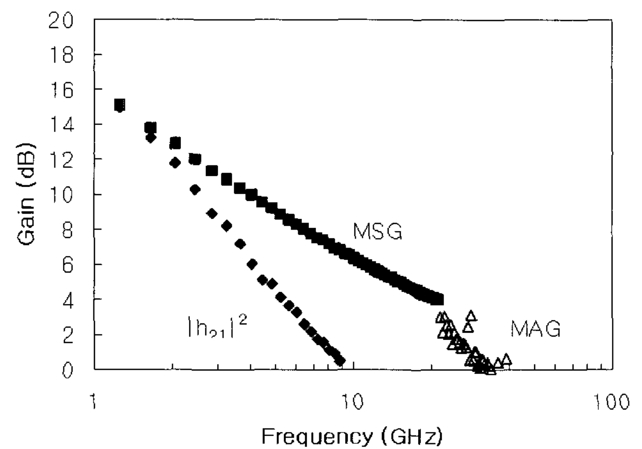
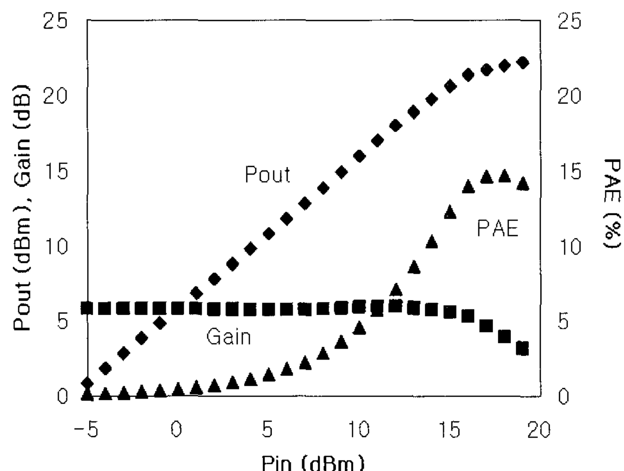
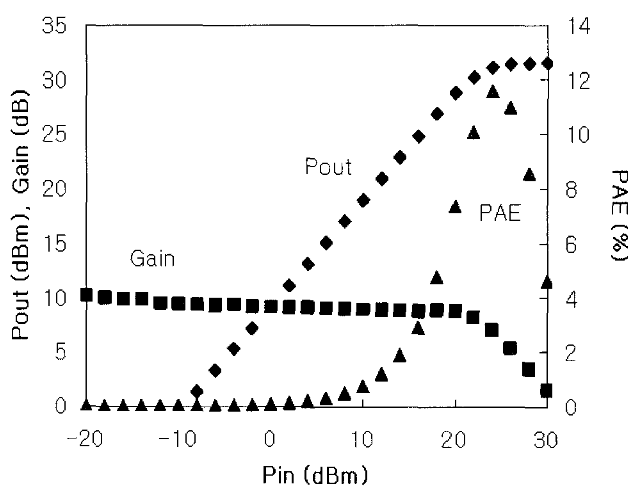


Fig. 3. RF small-signal characteristics of MESFETs with a gate length of 0.5 µm

of 30 V and a gate voltage of 1.0 V. The pinch-off voltage was -24 V. Fig. 3 shows the RF small-signal characteristics of the MESFET. The maximum oscillation frequency was 34 GHz and the cut-off frequency was 9.3 GHz at a drain voltage of 40 V and a gate voltage of -10 V. And the maximum stable power gain was 12.9 dB at 2 GHz. The RF large-signal characteristics were measured using a load-pull measurement system and the results are shown in Fig. 4(a). The measurements were performed in the condition of class A at a drain voltage of 40 V and using continuous wave (CW) single tone at 2 GHz. The power gain was 5.9 dB and the power added efficiency (PAE) was 14.6 %. The P1dB of 21.7 dBm and the output power density of 1.5 W/mm were obtained. Large impedances caused by the short gate width of 100 µm caused a relatively lower power gain compared to the maximum stable power gain calculated from the measured S-parameter.



(a)



(b)

Fig. 4. RF large-signal characteristics of the MESFET with a gate length of 0.5 μm and a gate width of of (a) 100 μm and (b) 1 mm measured at 2 GHz

For the application in microwave power amplifiers, MESFETs must have large gate width. The RF characteristics of a 1 mm-gate width MESFET were shown in Fig. 4(b). The power gain was 10.1 dB and the power added efficiency (PAE) was 11.6 % at 2 GHz. It is believed that this increased power gain is due to the decrease of the impedances which is caused by larger gate width. The output power of 1.4 W was obtained, which is 10 times larger than that of a 100 μm-gate width MESFET. This indicates that the device performance is not degraded with the increase of the gate width.

2. Charge Trapping Effect

One prominent issue of the microwave field-effect transistors (FETs) is the carrier trapping effect associated with the surface and epi-layer defects [5,6]. This trapping effect results in the reduction of the DC drain current as the RF input power is increased under RF operation. This phenomenon is very detrimental to RF performance because it decreases the transistor available power and device linearity. Fig. 5 shows the DC drain current with the RF input power and it clearly shows no drain current instability. An increase of the DC drain current with the RF input power is the common phenomenon of a component without trapping effects.

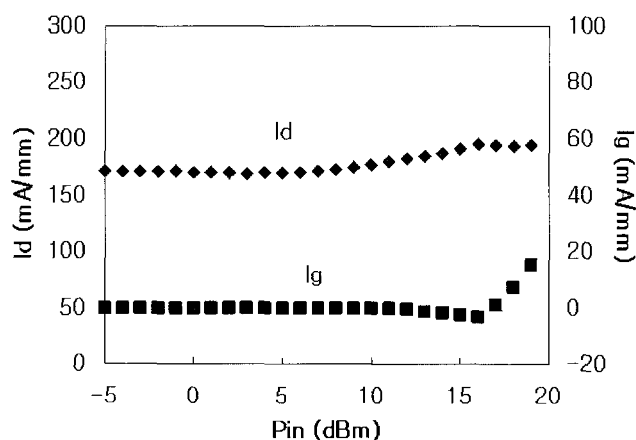


Fig. 5. *DC drain current versus input power without drain current instability*

To demonstrate our result, drain current recovery characteristics were investigated. After stressing the device for 2 min with the drain bias voltage of 30 V under the

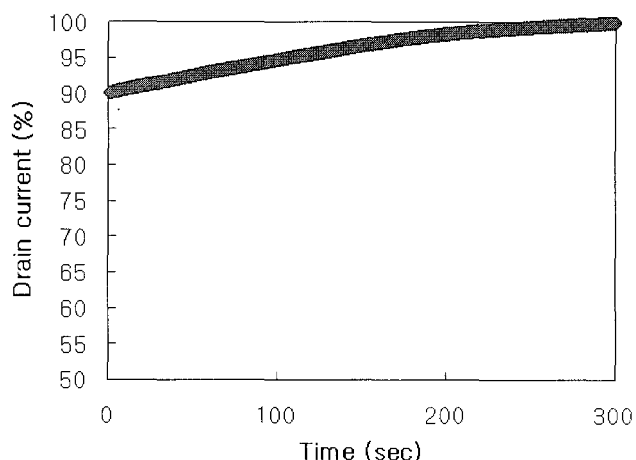


Fig. 6. Recovery characteristics of drain current after stress impression

pinch-off gate bias condition, the drain current was measured versus time with the drain bias voltage of 10 V and the gate bias voltage of 0 V. Fig. 6 shows the recovery characteristics of the drain current. Just 10 % reduction of the drain current was observed immediately after the stress impression. Fig. 7 shows the drain current versus drain bias characteristics. Significant drain current instability was not observed which verifies that the device performance is not affected by the charge trapping effect. It is believed that the surface passivation of our MESFETs using the thermal oxide layer prevent the charge trapping at the surface.

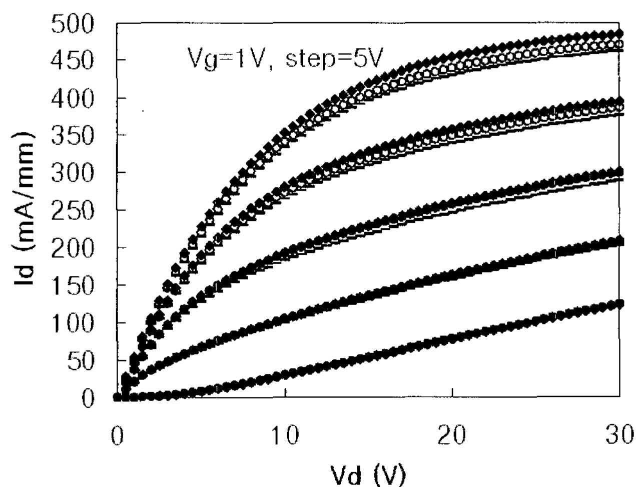
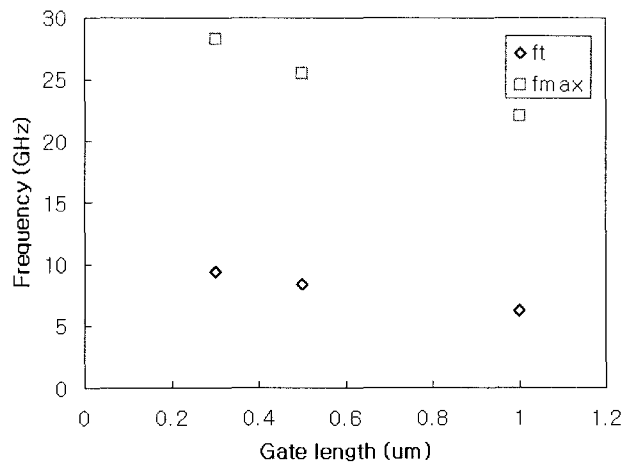


Fig. 7. Drain current versus drain bias characteristics. (♦) : Forward drain voltage sweep with the time interval of 150 sec for each gate bias, (○) : forward drain voltage sweep from V_g = 1 V toward -19 V without time interval, (-) : backward drain voltage sweep from V_g = -19 V toward 1 V without time interval

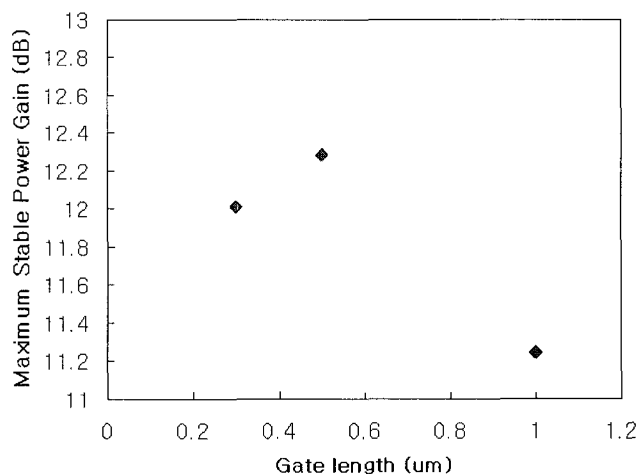
3. Effect of Gate Dimension Shrinkage on the MESFET Performance

Gate shrinkage is important to improve the device performance. With an advanced fabrication process, the gate length and the gate-to-source spacing could be reduced.

The RF small-signal characteristics were investigated as a function of the gate length and the results are shown in Fig. 8. The maximum oscillation frequency and the cut-off frequency were increased as the gate length is reduced. However, the maximum stable power gain was degraded for the 0.3 μm gate device. For a gate electrode to have adequate control of the current transport across the channel, the gate length (L) must be larger than the channel depth (a) [7]. To reduce the channel length and keep L/a, the channel depth has to be reduced, which implies a higher doping level. This high doping level causes easy breakdown phenomena. Therefore, a trade-off exists between high channel current and high breakdown voltage. To maximize the output power, the channel layer structure must be carefully designed as well as the gate structure.



(a)



(b)

Fig. 8. RF small-signal characteristics of submicron gate MESFETs as a function of the gate length. (a) maximum oscillation frequency and cut-off frequency and (b) maximum stable power gain

4. Analysis of the MESFET Performance using Small-signal Equivalent Circuit

The performance of the fabricated MESFETs was characterized by analyzing the small-signal equivalent circuit parameters extracted from the measured

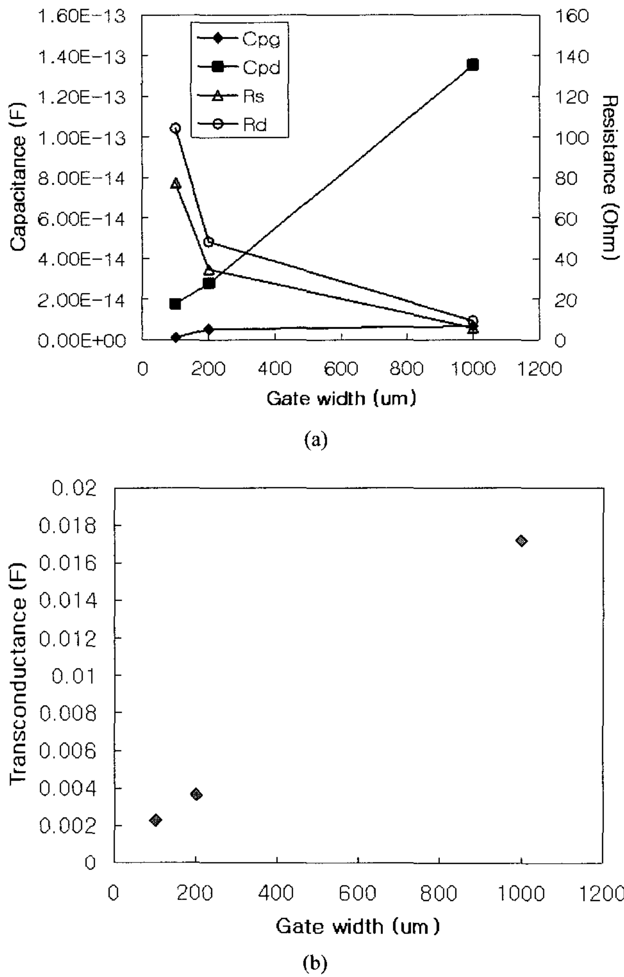


Fig. 9. (a) Extracted parasitic parameters and (b) transconductance as a function of the gate width

parameters. The measured MESFET performances were well explained from the analysis of the small-signal equivalent circuit. The extracted parameters were compared with the variations of gate width in Fig. 9. The parasitic source and drain resistances of a longer gate width MESFET were decreased while the parasitic gate resistance was increased. The transconductance was increased with the increase of the gate periphery due to the decrease of the source resistance. The increase of the transconductance caused the increase of the cut-off frequency and the maximum stable power gain of the longer gate width MESFET. The decrease of the maximum oscillation frequency can be explained by the increase of the gate resistance.

The effect of the gate length on the device performance was also analyzed by the extracted small-signal equivalent circuit parameters. Fig. 10 well shows the increase of the gate resistance with the reduction of the gate length as expectation. The decrease of the input capacitance and the feedback capacitance causes the increase of the maximum oscillation frequency and the cut-off frequency as the gate length reduces. It has to be noticed that the transconductance of the 0.3 μm gate device was degraded like the maximum stable power gain. The results indicate that both the channel layer structure and the gate structure must be carefully designed to maximize the output power.

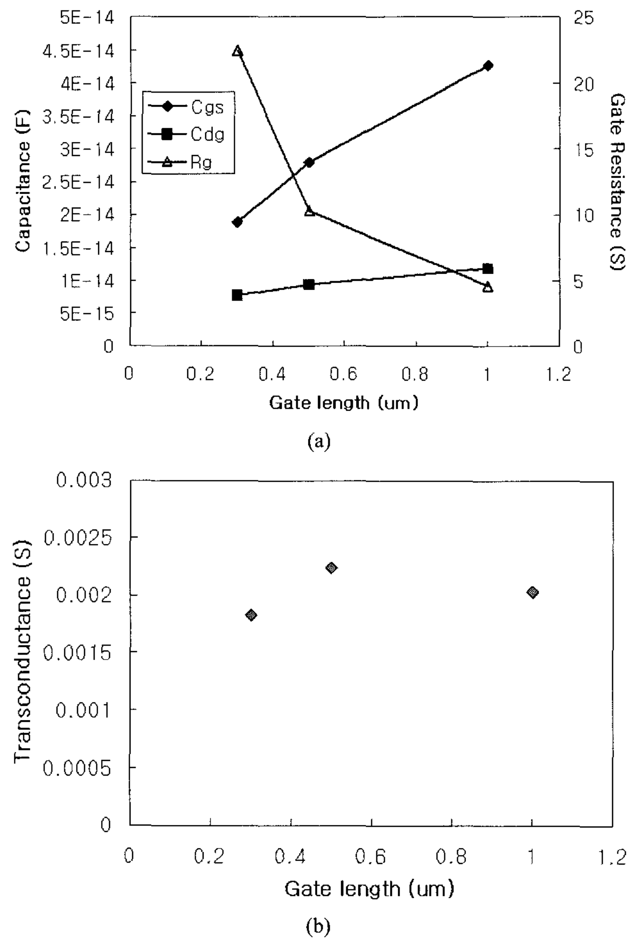


Fig. 10. (a) Extracted intrinsic capacitances and gate resistance and (b) transconductance as a function of the gate length

IV. CONCLUSIONS

Planar 4H-SiC MESFETs were fabricated by using ion-implantation. The saturation drain current and the transconductance of the fabricated MESFET were over

500 mA/mm and 41 mS/mm, respectively. And the maximum oscillation frequency of 34 GHz and the cut-off frequency of 9.3 GHz were achieved. The fabricated MESFET with a gate width of 1 mm showed the power gain of 10.1 dB and the output power of 1.4 W at 2 GHz. The performance was not degraded with the increase of gate width. And no drain current instability under RF operation was observed. It is believed that the surface passivation with a thermal oxide layer prevents the charge trapping at the surface. The performance of fabricated MESFETs was characterized by analyzing the small-signal equivalent circuit parameters extracted from the measured parameters.

ACKNOWLEDGMENTS

This work was done as a part of SiC Device Development Program (SiCDDP) supported by Ministry of Commerce, Industry, and Energy (MOCIE), republic of Korea

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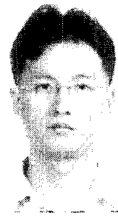

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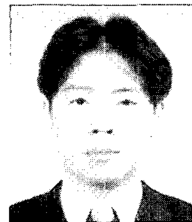

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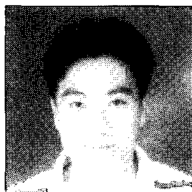

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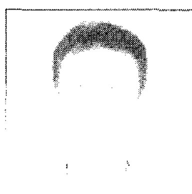

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