Characterizations of Interface-state Density between Top Silicon and Buried Oxide on Nano-SOI Substrate by using Pseudo-MOSFETs

Won-Ju Cho

Abstract—**The interface-states between the top silicon layer and buried oxide layer of nano-SOI substrate were developed. Also, the effects of thermal treatment processes on the interface-state distributions were investigated for the first time by using pseudo-MOSFETs. We found that the interface-state distributions were strongly influenced by the thermal treatment processes. The interface-states were generated by the rapid thermal annealing (RTA) process. Increasing the RTA temperature over 800°C, the interface-state density considerably increased. Especially, a peak of interface-states distribution that contributes a hump phenomenon of subthreshold curve in the inversion mode operation of pseudo-MOSFETs was observed at the conduction band side of the energy gap, but it was not observed in the accumulation mode operation. On the other hand, the increased interface-state density by the RTA process was effectively reduced by the relatively low temperature annealing process in a conventional thermal annealing (CTA) process.**

Index Terms—**Nano-SOI substrate, Pseudo-MOSFETs, Back interface states, Thermal annealing**

I. INTRODUCTION

As the gate lengths of MOSFETs are scaled down to a sub-100 nm regime, the operation of transistors is limited due to the short-channel effects (SCE). Several technologies have been suggested to overcome the SCE in extremely small size devices. The silicon-on-insulator (SOI) devices, especially the fully depleted (FD) SOI devices are expected to become a main stream of high performance technology because it can relax the SCE compared to the bulk-silicon devices [1,2]. Also, SOI devices are expected to use for the bio-device applications as well as electronic-device applications [3,4]. In SOI MOSFET devices, there are two interfaces at the channel, i.e., the front interface at the gate oxide-silicon channel and the back interface at the silicon channel-buried oxide. Therefore, the electrical characteristics of SOI MOSFET devices are significantly influenced by the back interface as well as front interface. The thickness of silicon channel will continuously decreases with scaling-down of the integrated circuit dimensions. Hence, an optimization of the back interface properties becomes one of the key technologies in SOI device applications. However, much less work has been done in studying the electrical properties of back interface; instead, the physical qualities such as Si thickness, doping concentration, Si precipitates in buried oxide, interface roughness and dislocation are inferred from the TEM or SIMS analysis.

In this work, therefore, we investigated the electrical properties of SOI substrate and obtained the interface-state distribution of back interface using the pseudo-MOSFETs [5,6]. The effects of thermal treatment processes by the rapid thermal annealing (RTA) or the conventional thermal annealing (CTA) on the donor- and acceptor-type traps were extracted for the first time for the nano-SOI substrate.

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II. EXPERIMENTAL

P-type (100) UNIBOND SOI wafers with a silicon film thickness of 100 nm and buried oxide (BOX) thickness of 200 nm were used. The doping density is on the order of 10^{15} cm^{-3}. The thickness of silicon film was reduced to 50 nm by wet etching process with a 2.38 % diluted tetramethylammonium hydroxide (TMAH) solution. The oxidation methods or dry etching methods for reducing the silicon film thickness were avoided because such processes can introduce the electrical effects on the back interface of SOI substrate. For fabricating the pseudo-MOSFETs, the silicon film was patterned into rectangular active patterns of approximately 60μm×20μm area to prevent leakage current from the silicon film to the substrate across the BOX layer. The wafers were then cleaned in a SPM (Sulfuric Peroxide Mixture, H_2SO_4:H_2O_2=1:1) chemical for 10 minutes, rinsed in DI water for 10 minutes, followed by diluted HF (H_2O:HF=100:1) for 1 minute. Two tungsten probes were placed on the Si active to form the source and drain contacts. The RTA process over 400-900°C temperature ranges was carried out to evaluate the repercussions on back interface D_{it} distributions in pseudo-MOSFETs. The ramp-up rate and ramp-down rate of RTA process were adjusted to 30°C/s and 20°C/s, respectively. A CTA process over 300-800°C temperature ranges was carried out in the conventional furnace system after the RTA of 950°C. The ramp-up rate and ramp-down rate of CTA process were fixed at 10°C/m and 3°C/s, respectively. Also, to verify the effectiveness of CTA process after RTA even on the SOI MOSFET devices with diffused source/drain, we fabricated the conventional type SOI MOSFETs devices and the electrical characteristics were measured. The plasma doping technique was used to form the source/drain region of conventional SOI MOSFETs and the RTA process at 950°C was followed to activate the implanted impurity atoms [7]. Additionally, some of these samples were annealed at 500°C for 30 minutes in nitrogen ambient using conventional furnace system.

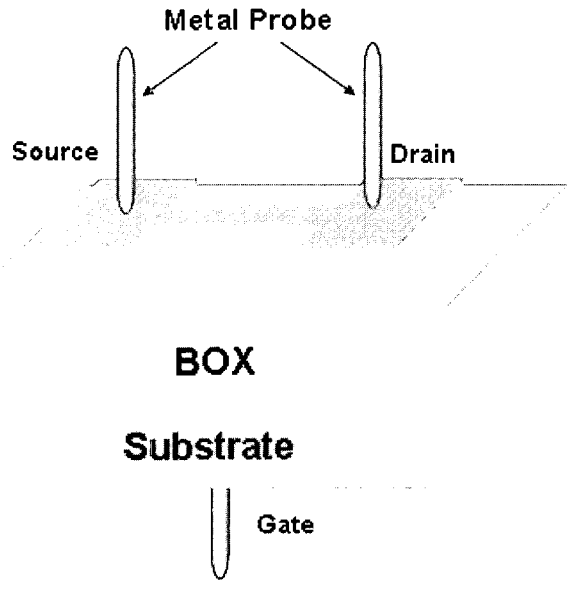


Fig. 1. Schematic representation of pseudo-MOSFET devices fabricated on the nano-SOI substrate. Two tungsten probes were placed on the Si active to form the source and drain contacts.

III. RESULTS AND DISCUSSIONS

Figure1 shows schematic representation of pseudo-MOSFET devices. The pseudo-MOSFET has been proposed as a simple electrical technique to characterize as-grown SOI wafers prior to any device processing. This device takes full advantage of vertical, MOS-like configuration of SOI wafers. The point contacts with Schottky barrier made to the top silicon film act as the source and drain while BOX and bulk substrate act as the gate oxide and gate electrode, respectively. Biasing the bulk substrate induces inversion channel or accumulation channel at the Si/BOX interface.

Figure 2 shows the *I-V* characteristics of pseudo-MOSFET fabricated on the SOI substrate with a 50 nm thick Si channel. It is clear from the Fig. 2 (a) that the drain current versus drain voltage (I_d-V_{ds}) curves of pseudo-MOSFETs exhibits both n-channel and p-channel operation characteristics. When the gate voltage is increased in the positive polarity, the film is fully depleted until the inversion threshold is reached. Then, the pseudo-MOSFET shows n-channel characteristics. On the other hand, when the gate voltage is increased in the negative polarity, the surface potential at the Si/BOX interface decreases until it reaches flat band and then decreases further to become slightly negative. At this point the film is accumulated and the pseudo-MOSFET exhibits p-

channel characteristics. Therefore, both the accumulation and inversion channels are measured simultaneously on the same sample, and hence we can get the insights into the electrical properties of Si/BOX interface without additional diffused source/drain structures. The drain current of pseudo-MOSFETs in linear region, strong inversion or accumulation, are correctly described by the elementary MOS transistor equations for the saturation regions [8].

For inversion channel, the drain current I_{dN} is given by [6]

$$I_{dN} = \mu_e f_g C_{ox} V_D \left(V_G - V_{TH} - \frac{V_D}{2} \right) \quad (1)$$

where C_{ox} is the BOX capacitance, V_{TH} is the threshold voltage, μ_e and is the effective mobility of electrons, f_g is geometric coefficient ($W/L=0.33$).

On the other hand, the drain current for accumulation channel I_{dP} is given by [6]

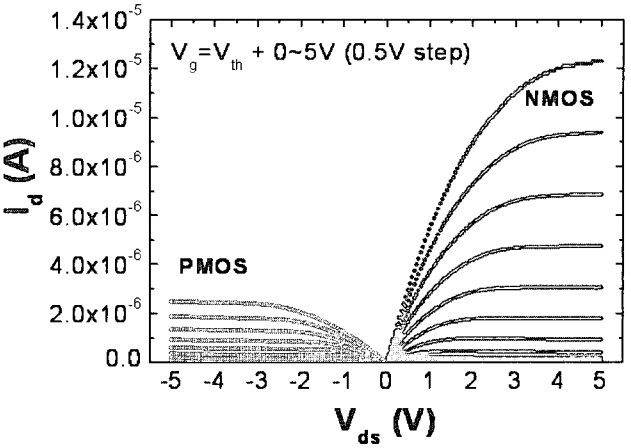
$$I_{dP} = \mu_h f_g C_{ox} V_D \left(V_G - V_{FB} - \frac{V_D}{2} \right) \quad (2)$$

where V_{FB} is the flat-band voltage and μ_h is the effective mobility of holes. The estimated threshold voltage and flat-band voltage using these relationships and measured results are 1.8 V for n-channel and -4.5 V for p-channel, respectively.

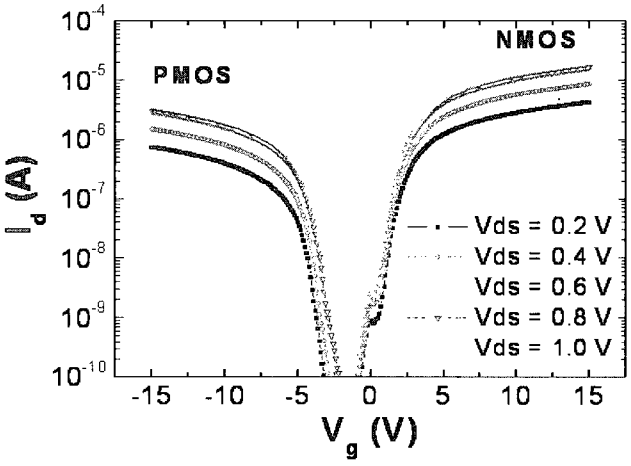
Figure 2 (b) shows the subthreshold current verses gate voltage (I_d-V_g) for n-channel and p-channel. From the subthreshold characteristics in weak inversion region, the subthreshold swing and the density of back interface, D_{it}, can be determined by using the following relations [6]

$$I_d = I_0 \exp\left(\frac{V_g}{S} \right), \quad S = 2.3kT \left(1 + \frac{C_{si} + qD_{it}}{C_{ox}} \right) \quad (3)$$

where C_{si} are the depletion region capacitance of Si film. Interestingly, a weak distortion (hump) of drain current at low gate bias (0-0.5 V) was observed in the n-channel region, whereas it was not appeared in the p-channel region. We consider that this weak hump is related to the interface-state at the Si/BOX interface of initial SOI substrate. The interface-state at specific energy level may originate mainly from the mechanical stress between two layers or the process induced defects during the SOI fabrication processes.



(a)



(b)

Fig. 2. Drain current to drain voltage characteristics (a), and drain current to gate voltage characteristics (b) for both n-channel and p-channel operations of pseudo-MOSFETs

Figure 3 shows the I-V characteristics for various RTA temperatures. The subthreshold swing S of I_d-V_g characteristics in Fig. 3(a) is defined as the gate voltage V_g required to vary the subthreshold current I_d by one decade. As the RTA temperature increases, it is evident that the degradation of subthreshold swing, particularly in n-channel regime, increases as a function of RTA temperature. Especially, a considerable distortion of subthreshold swing in n-channel region was found at the RTA temperature higher than the 800°C. In general, the degradation of subthreshold swing is due to the increase of interface state density, decrease of oxide capacitance and increase of doping concentration of MOS transistor's channel. Since the BOX thickness and substrate doping concentration were same in this study, the increase of interface-state density D_{it} between the Si film and BOX

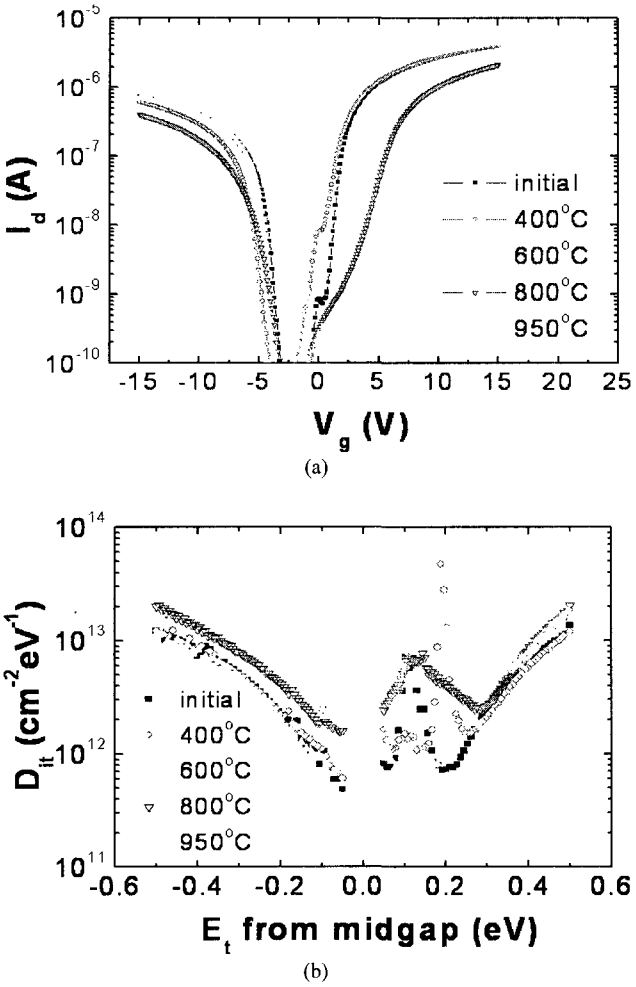


Fig. 3. I_d-V_g characteristics (a), and the back interface-state distributions (b) of pseudo-MOSFETs for various RTA temperatures

layer is considered as the origin of the subthreshold swing degradation. Fig. 3(b) shows the corresponding back interface D_{it} of pseudo-MOSFETs, which was extracted from the subthreshold swing according to the following equation [6].

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{S}{2.3kT/q} - \left(1+\frac{C_{si}}{C_{ox}}\right)\right) \quad (4)$$

A narrow and small peak of interface-states was observed between the conduction band and midgap, and such interface-states act as acceptor-type traps. As the RTA temperature increased above 800°C, the peak of interface-states increased in the vicinity of conduction band. The increase of back interface D_{it} is attributed to a large stress generated at the Si/BOX interface. The RTA is a major annealing technology that can replace a number of the conventional thermal process due to a low thermal budget and less turnaround time. The RTA is used for activation and redistribution of the implanted dopants, formation of the silicide, and reflow of dielectric layers. However, the rapid rise and fall of temperature, which is inherent feature of the RTA, is known to affect the Si-SiO_2 interface properties, which play a central role in performances of MOSFET [8,9]. It is reported that RTA significantly increases local Si/SiO_2 interface trap density at surface potential in vicinity of center of weak inversion, because a large mechanical stress is produced at the Si/SiO_2 interface due to the difference in the thermal expansion coefficient [10,11].

Figure 4 shows the *I-V* characteristics of pseudo-MOSFETs for various temperatures of the CTA process after RTA of 950°C. It is found that the subthreshold characteristics in Fig.4 (a) were varied with the CTA temperatures.

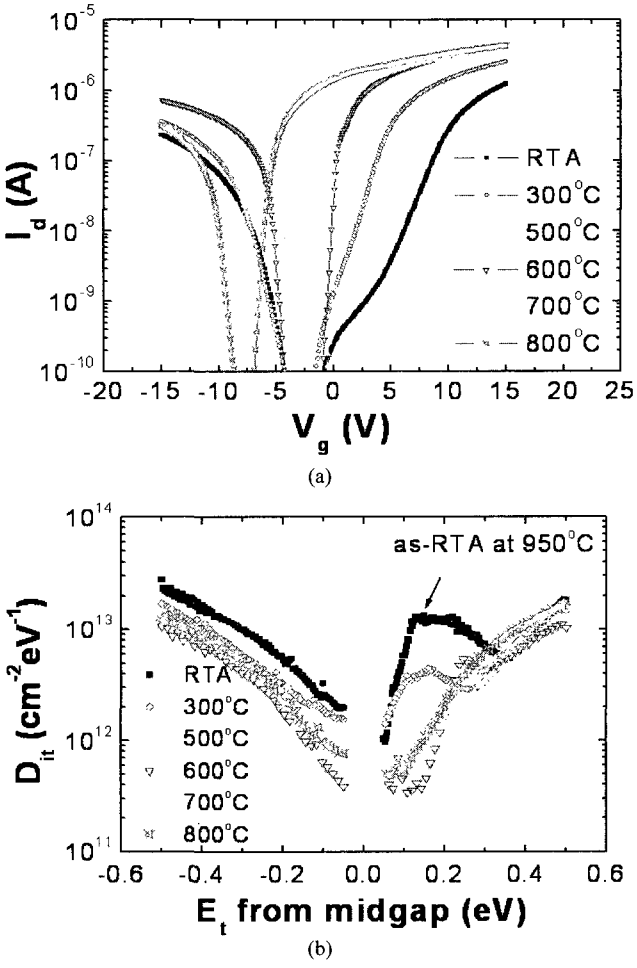


Fig. 4. I_d-V_g characteristics (a), and the back interface-state distributions (b) of pseudo-MOSFETs for various CTA temperatures after RTA. The RTA was carried at 950°C for 30s

As the CTA temperature increased from 300°C to 800°C, the distortion of subthreshold curve was improved. Especially, the 500-600°C CTA process showed most excellent subthreshold characteristics without shift of subthreshold curve. When the CTA temperature exceeds 700°C, the considerable shift of subthreshold curves to negative gate bias voltage was observed. We found that this shift was very reproducible and reversible, i.e., when the sample annealed at lower temperature than 700°C the subthreshold curve was shifted to positive gate bias side again and vice versa. At present, the exact reason for the behavior of subthreshold curve shift is unclear and further study is required. Fig. 4 (b) shows the back interface D_{it} of pseudo-MOSFETs. It is found that back interface D_{it} generated during the RTA process decreased by CTA process. When the annealing temperature is lower than 500°C, the effect of CTA was insignificant. Meanwhile, the improvement of D_{it} was almost saturated at 500°C. Particularly, the acceptor-type traps above the midgap energy were significantly reduced by CTA process. These results suggest that the CTA is very effective process for improving the interface-states at the Si/BOX interface generated by RTA process.

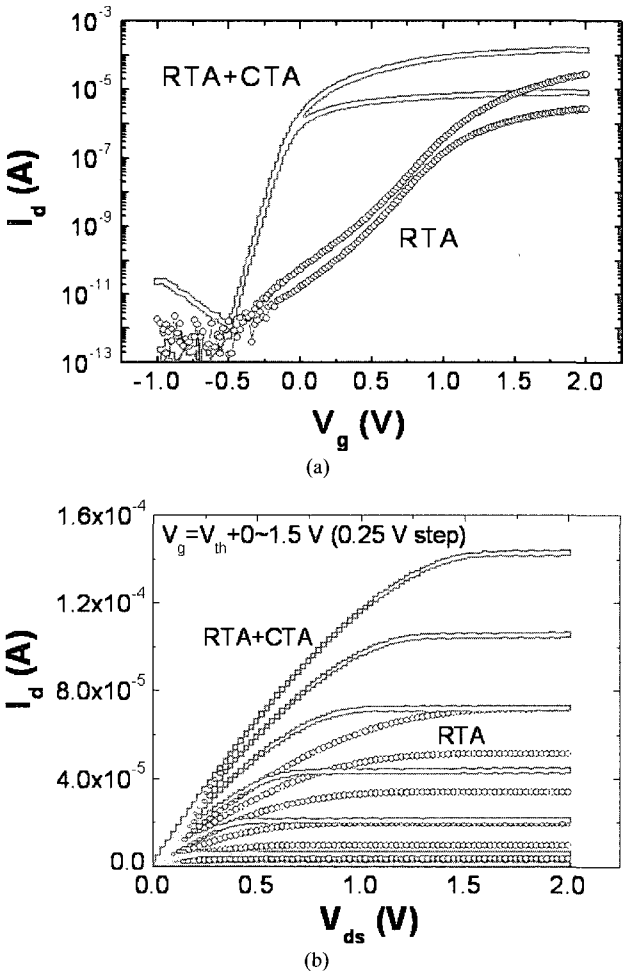


Fig. 5. Current-voltage characteristics of SOI n-MOSFETs. RTA and CTA were carried out at 950°C for 30s and at 500°C for 30m, respectively

Figure 5 shows the I-V characteristics of conventional SOI MOSFETs with a diffused source/drain region, which was measured to correlate the effects of back interface-state and thermal annealing processes on the operation characteristics of pseudo-MOSFETs and conventional SOI MOSFETs.

Similar to the pseudo-MOSFETs, a considerable degradation of subthreshold swing and a hump at low gate electrical field were observed in RTA processed sample as shown in Fig. 5(a). We also confirmed that the hump was observed only in the n-channel MOSFETs, which is the same result of pseudo-MOSFETs. On the other hand, the subthreshold characteristics of CTA processed sample after RTA showed an excellent subthreshold swing, approximately 65 mV/decade. Fig.5 (b) shows the characteristic of drain current against the drain voltage (I_d-V_{ds}). The saturation current of CTA processed sample was much larger than that of the RTA processed sample. These results suggest that the optimization of thermal process is required to fabricate electrically reliable SOI substrate and high performance SOI electronic devices.

IV. Conclusions

A study on the interface-states at the top Si/BOX interface and the effects of annealing processes of nano-SOI substrate has been presented. The distributions of interface-states at the top silicon/buried oxide interface were evaluated by the pseudo-MOSFETs. We found that the RTA process introduced the back interface-states and high temperature RTA process increased the back interface-states. Especially, the back interface-states above the midgap of energy band, which act as acceptor-type traps and resulted in the considerable degradation of n-channel operation, were strongly affected by the thermal processes. On the other hand, the increased trap density by

RTA process was remarkably decreased by relatively low temperature CTA process for the first time. Also, we confirmed that the electrical characteristics of conventional SOI MOSFETs with source/drain regions as well as pseudo-MOSFETs strongly depend on the thermal processes. Therefore, we can conclude that the control of interface-states at the Si/BOX interface by optimization of thermal process is very important for fabricating high performance SOI MOSFETs.

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