Characteristics of Schottky Diode and Schottky Barrier Metal-Oxide-Semiconductor Field-Effect Transistors

Moongyu Jang, Yarkyeon Kim, Myungsim Jun and Seongjae Lee

Abstract—**Interface-trap density, lifetime and Schottky barrier height of erbium-silicided Schottky diode are evaluated using equivalent circuit method. The extracted interface trap density, lifetime and Schottky barrier height for hole are determined as 1.5×10^{13} traps/cm^2, 3.75 ms and 0.76 eV, respectively. The interface traps are efficiently cured by N$_2$ annealing. Based on the diode characteristics, various sizes of erbium- silicided/platinum-silicided *n/p*-type Schottky barrier metal-oxide- semiconductor field effect transistors (SB-MOSFETs) are manufactured from 20 μm to 35nm. The manufactured SB-MOSFETs show excellent drain induced barrier lowering (DIBL) characteristics due to the existence of Schottky barrier between source and channel. DIBL and subthreshold swing characteristics are compatible with the ultimate scaling limit of double gate MOSFETs which shows the possible application of SB-MOSFETs in nanoscale regime.**

Index Terms—**SB-MOSFETs, Schottky diode, interface trap, scaling**

I. INTRODUCTION

Recently, silicide metallic junction-based electronic devices are being studied for the applications in nanometer regime as the alternative of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) [1]-[3]. In Schottky barrier MOSFETs (SB-MOSFETs), the source and drain are composed of silicide instead of impurity doped silicon. Thus the parasitic source and drain resistance can be efficiently eliminated and the process temperature can be reduced dramatically lower than 600 °C, giving the opportunity to use metal as gate electrode and high-K dielectric materials as gate insulator [1]. However, in SB-MOSFETs, silicon in channel region reacts with the deposited metals. This reaction can cause the generation of trap states, causing microscopic inhomogeneity of Schottky barrier height [4]. Thus, for the improvement of the device performance, the interface of Schottky diode should be carefully analyzed. Until now, current-voltage (*I-V*) measurement method has been widely used to explore the trap states in Schottky diode by evaluating diode ideality factor [4], [5]. However, there has been no established method on the quantitative evaluation of trap density in the Schottky diode, although it is well established in the metal-insulator-semiconductor system [6].

In SB-MOSFETs, most of the works are done in *p*-type transistors, using platinum-silicide because of its low Schottky barrier height (0.24 eV) for hole [3]. Recently, erbium-silicide is being considered as the candidate for the *n*-type SB-MOSFETs [2, 3]. But there have been no studies on the erbium-silicided Schottky diode characteristics, incorporating trap states with Schottky barrier height and their effects on the electrical characteristics of SB-MOSFETs.

In this paper, erbium-silicided Schottky diode is fabricated on the *p*-type silicon and the interface of Schottky diode is analyzed using the current-voltage and capacitance-voltage (*C-V*) measurement methods.

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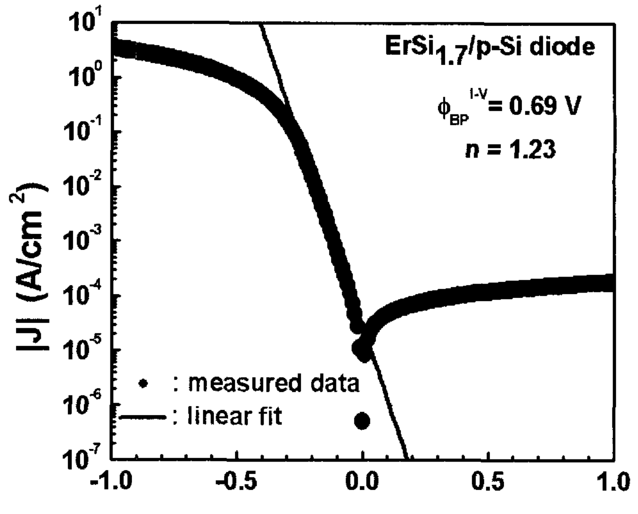
Moreover, by incorporating equivalent circuit model with the *C-V* measurement method, trap density, lifetime and Schottky barrier height are extracted in erbium-silicided Schottky diode. Also, short channel characteristics of SB-MOSFETs are analyzed using drain induced barrier lowering (DIBL) and subthreshold swing (SS) characteristics. Also, the simple DIBL model of SB-MOSFETs is proposed and compared with the scaling theory of double gate (DG) MOSFETs.

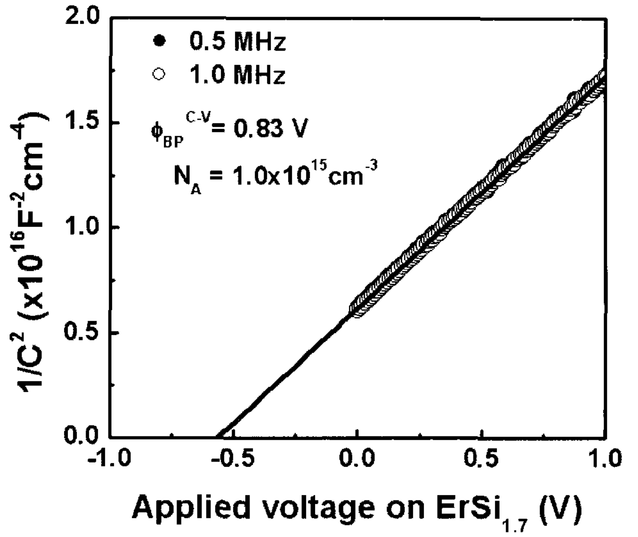
II. EXPERIMENTAL

1. Fabrication of Erbium-Silicided Schottky Diode

In conventional MOSFETs, Titanium, Cobalt and Nickel are widely being used for the silicidation process to minimize the parasitic resistance of impurity doped source and drain. But in this work, erbium is chosen as source and drain metal of *n*-type SB-MOSFETs, because of its low Schottky barrier height (0.28 eV) for electrons [2, 3]. The boron doped (100) *p*-type bulk silicon wafer is used for the erbium-silicided Schottky diode. The resistivity is 13.5-22.5 Ω·cm and the corresponding doping concentration is about 1.0×10^{15} cm^{-3}. After wafer cleaning, 100 nm thick SiO_2 layer is grown on the wafers using thermal oxidation method at 1000 °C and the 250 μm×250 μm region is opened using lithography and 30:1 BOE (buffered oxide etchant) etching. After erbium sputtering, erbium-silicide is formed by using rapid thermal annealing (RTA) technique. Annealing temperature and time and pressure are 500 °C, 5 min and 1.0×10^{-6} torr, respectively. The non reacted erbium is removed by using the mixture of H_2SO_4 and H_2O_2 (Sulfuric Peroxide mixture: SPM) SPM for 10 min. The volume ratio of H_2SO_4 and H_2O_2 is 1:1. The thickness of $ErSi_{1.7}$ is about 55 nm which is confirmed by Transmission Electron Microscopy. Platinum-silicide is formed on the boron heavily doped backside of *p*-type silicon wafers for ohmic contact for the accuracy of the measurements.



(a)



(b)

Fig. 1. Room -temperature *I-V* and *C-V* curves of $ErSi_{1.7}$/p-Si diode. The extracted Schottky barrier height for hole is 0.69 and 0.83 V from *I-V* and *C-V* method, respectively.

2. Fabrication of SB-MOSFETs

As starting material, (100) *p*-type silicon-on-insulator (SOI) wafer is used. SOI wafer is boron doped with a resistivity of 13.5~22.5 Ω·cm and the corresponding doping concentration is about 1.0×10^{15} cm^{-3}. The thickness of the SOI and buried oxide (BOX) layer is 100 nm and 200 nm, respectively. The gate oxide is 5 nm thick SiO_2, grown by thermal oxidation and the gate electrode is highly phosphorus doped *n*-type polycrystalline silicon. Electron-beam lithography is employed to define gate pattern. After gate etching, 30 nm thick gate sidewall spacer is formed by using thermal oxidation method. After blanket dry etching of gate sidewall spacer, 100 nm thick erbium and platinum are sputtered for *n*-type and *p*-type

SB-MOSFETs, respectively. Erbium-silicide and platinum-silicide are formed by using rapid thermal annealing (RTA) technique. Annealing temperature and time is 500 °C and 5 min, respectively. The non-reacted erbium and platinum are removed by using SPM and aqua regia for 10 min, respectively. The formation of $ErSi_{1.7}$ and PtSi phase are confirmed by x-ray diffraction (XRD) and Auger electron spectroscopy (AES) analysis. The sheet resistance are less than 30 Ω/□ and 10 Ω/□ for erbium-silicide and platinum-silicide, even if the line width is less than 100 nm. Thus, erbium and platinum are applicable in sub-100 nm regime SB-MOSFETs manufacturing.

III. RERULTS AND DISCUSSIONS

1. Analysis of Erbium-Silicided Schottky Diode

For the erbium-silicide/*p*-type silicon contact, Schottky barrier heights for hole are extracted as 0.69 and 0.83 eV from *I-V* (Fig. 1a) and *C-V* measurement (Fig. 1b), respectively. The barrier heights determined by two methods give big difference, which causes the difficulty in the determination of Schottky barrier height. On the other hand, from the *I-V* measurement, the extracted ideality factor is 1.23 which implies the possible existence of traps within the depletion region of erbium-silicided Schottky diode. The existence of traps causes the microscopic inhomogeneity of Schottky barrier, which will in turn degrade the ideality factor, thus change the Schottky barrier height [4], [5]. Forwardly biased current transport at inhomogeneous Schottky barrier is dominated by low Schottky barrier patches, leading to the deduction of barrier height. Since, under usual circumstances, the *C-V* method yields an average Schottky barrier height for the whole diode [4]. To analyze the leakage current (I_R) conduction mechanisms in reversely biased Schottky diode, Frenkel-Poole and Schottky emission models are considered [6], [7]. The plot of $\ln(I_R/E)$ and $\ln(I_R/T^2)$ versus $E^{1/2}$ gives the linear curve for the Frenkel-Poole and Schottky emission and the slope can be expressed as [7]

$$S = \frac{q}{nkT}\sqrt{\frac{q}{\pi\varepsilon}} \tag{1}$$

where, n = 1, 2 for the case of Frenkel-Poole and Schottky emission, respectively. Here, q is the electron charge quantity, k Boltzmann's constant, ε permittivity, and E the maximum electric field in Schottky diode. The theoretically calculated slopes at 27°C for Frenkel-Poole and Schottky emission is 0.0087 and 0.0043 $(V/cm)^{-1/2}$, respectively.

Fig. 2 shows $\ln(I_R/E)$ and $\ln(I_R/T^2)$ versus $E^{1/2}$ curves obtained with the use of *I-V* data shown for the erbium-silicided Schottky diode in Fig. 1a. The slopes as determined from the fit to the data are extracted as 0.013 and 0.027 $(V/cm)^{-1/2}$, for Frenkel-Poole and Schottky emission, respectively. The experimentally determined

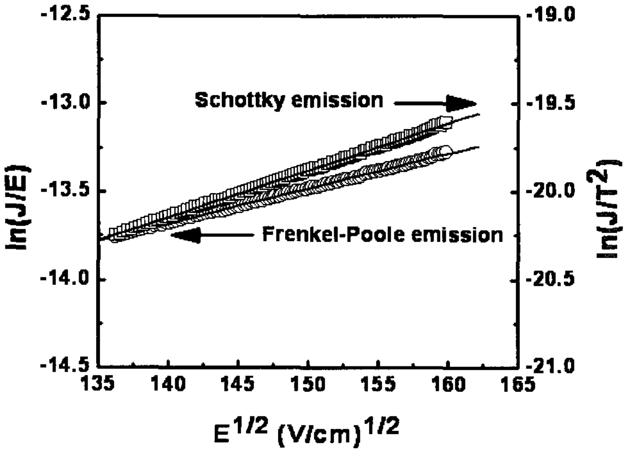


Fig. 2. Electric field dependence of $ErSi_{1.7}$/p-Si diode in the reverse bias region at 27 °C. The circle and square symbol correspond to the Frenkel-Poole and Schottky emission, respectively

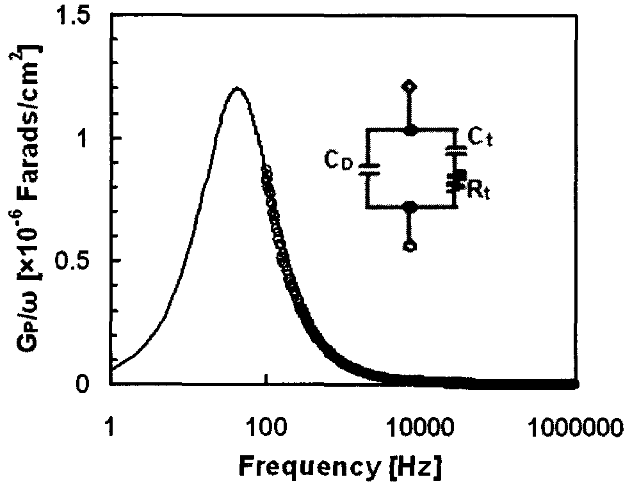


Fig. 3. Frequency versus conductance loss plot. From this plot, the trap density (D_t) and lifetime (τ) can be extracted. The reversely biased voltage is 0.2 V. Inset shows equivalent circuit of Schottky diode including trap states

slope is slightly larger than the theoretical value for Frenkel-Poole case, but is much larger than the theoretical value for Schottky emission. Thus, the result is more consistent with Frenkel-Poole emission which implies the existence of deep trap level within depletion region of erbium-silicided Schottky diode.

The equivalent circuit of Schottky diode, including the trap states can be modeled as shown as inset of Fig. 3 [6]. In the figure, C_D, C_t and R_t are the semiconductor depletion-layer capacitance, traps associated capacitance and resistance, respectively. The product C_tR_t is defined as the trap lifetimeτ. The parallel branch of the equivalent circuit in Fig. 3 can be converted into a frequency-dependent C_p in parallel with a frequency-dependent conductance G_p and can be expressed as following.

$$\frac{G_p}{\omega} = \frac{C_t\omega\tau}{1+\omega^2\tau^2}, \quad C_p = C_D + \frac{C_t}{1+\omega^2\tau^2} \qquad (2)$$

where, ω is the angular frequency.

In (2), the plot of G_p/ω versus $\omega\tau$ goes through maximum when $\omega\tau = 1$, and gives τ directly. The value of G_p/ω at the maximum is $C_t/2$. Thus, equivalent parallel conductance, divided by angular frequency gives C_t and τ directly from the measured conductance. The trap density is obtained by using the relation $D_t = C_t/qA$, where A is the diode area. By using the extracted value C_t in G_p/ω relation, C_D can be extracted directly by using C_p. Also, C_t andτ can be evaluated by using C_p relation. But in this case, inaccuracy of extracted values can exist because of the sensitive dependence of C_p to measured frequency, ω. For the consideration of external resistance including substrate and contact resistance, serial connection of additional resistor can be added.

Fig. 3 shows the plot of G_p/ω versus frequency with the 0.2 V reverse bias condition. The conductance and capacitance are measured using HP4285A impedance analyzer. In figure, the circle and solid line represent measured and fitted data, respectively. From the curve fitting, the extracted C_t, D_t and τ value are 2.4×10^{-6} Farads/cm^2, 1.5×10^{13} traps/cm2 and 3.75 ms, respectively. The extracted C_D value is 10.6×10^{-9} Farads/cm^2. The extracted interface-trap density is higher compared with the typical values in SiO_2 interface [8]. This interface-trap can be cured using hydrogen annealing.

By using the aforementioned method, depletion

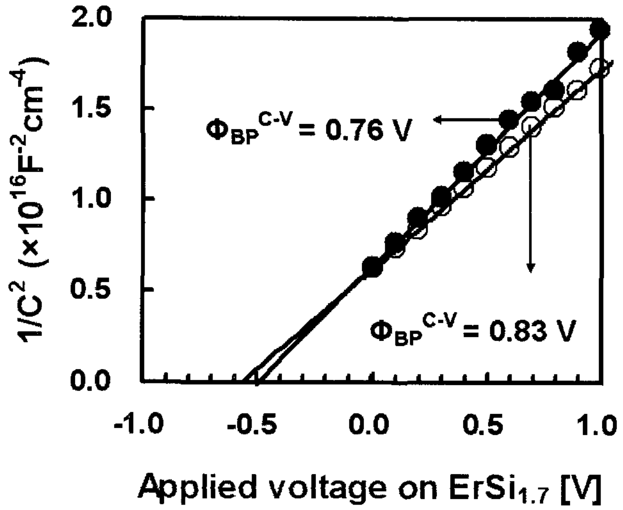
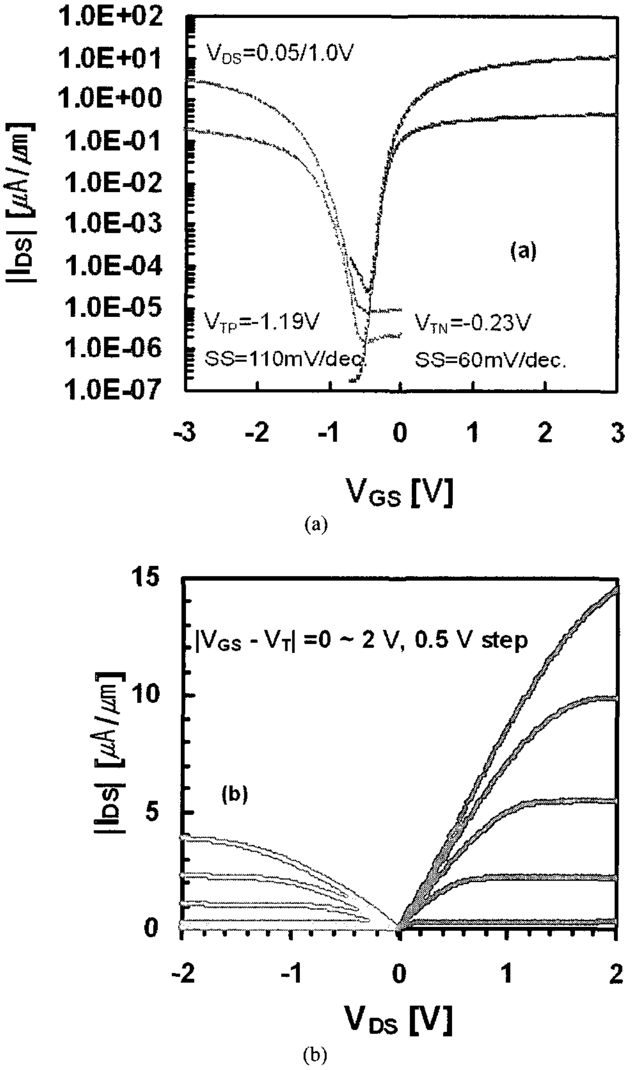


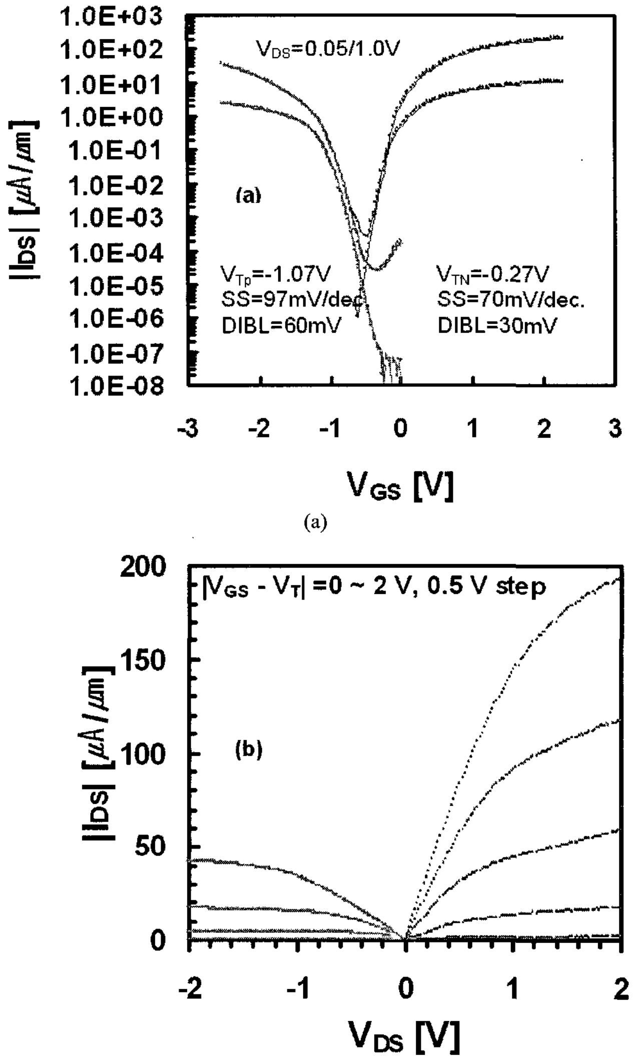
Fig. 4. Re-extraction of Schottky barrier height by eliminating the capacitance associated with trap



(a)

(b)

Fig. 5. I_{DS}-V_{GS} (a) and I_{DS}-V_{DS} (b) characteristics of 20 μm long channel *n*/*p*-type SB-MOSFET



(a)

(b)

Fig. 6. I_{DS}-V_{GS} (a) and I_{DS}-V_{DS} (b) characteristics of 100 nm gate length *n/p*-type SB-MOSFET

capacitance (C_D) values are extracted for the various reverse bias conditions. Fig. 4 shows the plot of $1/C_D^2$ versus reverse voltage and open and closed circles represent the as-measured (C_P) and corrected depletion capacitance (C_D) data, respectively. C_P includes C_I, giving the wrong Schottky barrier height in the plot of $1/C^2$ versus reverse voltage. The slope of corrected data has higher values than that of as-measured data because C_I is eliminated from C_P. From Fig. 4, the re-extracted Schottky barrier height is 0.76 eV for hole and 0.36 eV for electron. The extracted value is consistent with reported photoemission method, which shows the validity of newly developed method [11]. The extracted Schottky barrier height of erbium-silicide is higher compared with the value extracted in SB-MOSFETs results (0.28 eV) [3]. In SB-MOSFETs, image force induced Schottky barrier height lowering is severe due to the electrically induced inversion carriers. At strong inversion condition, the estimated barrier lowering value is almost 0.1 eV [2]. Thus, in SB-MOSFETs, the effective Schottky barrier height can be lower than the value extracted by Schottky diode measurement.

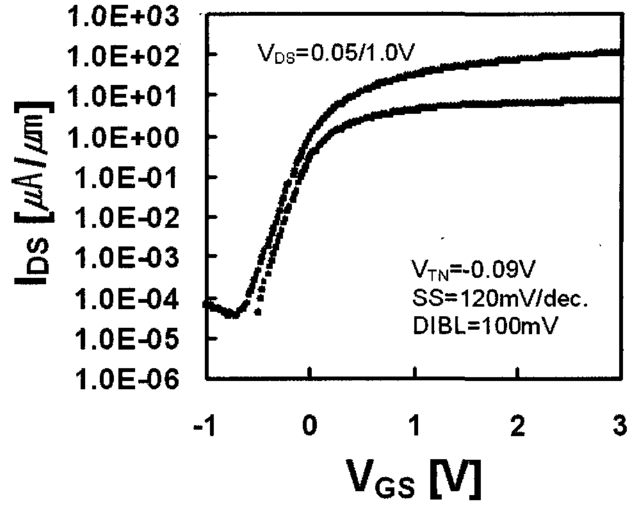


Fig. 7. I_{DS}-V_{GS} characteristics of 23 nm *n*-type SB-MOSFET

2. Scalability of SB-MOSFETs

Fig. 5 shows I_{DS}-V_{GS} characteristics of the 20μm long channel *n/p*-type SB-MOSFETs. The gate oxide and spacer thickness is 5nm and 15nm, respectively. Both the *n/p*-type SB-MOSFETs show high on/off current ratio, larger than $I_{on}/I_{off}>10^5$ with low leakage current ($I_{LKG}<100$ pA/μm). The on/off ratio and the leakage current level is the highest and lowest values compared with previously published data in *n*-type SB-MOSFETs [3]. Also, DIBL is almost suppressed in both *n/p*-type SB-MOSFETs and the SS value is 60mV/decade in *n*-type SB-MOSFETs.

Fig. 6 shows the I_{DS}-V_{GS} characteristics of erbium-silicided 100nm gate length *n/p*-type SB-MOSFETs. Also, this 100nm gate length *n/p*-type SB-MOSFET shows excellent short channel characteristics. The measured SS and DIBL values are 70mV/decade and 30mV, respectively, for *n*-type SB-MOSFETs.

Fig. 7 shows the I_{DS}-V_{GS} characteristics of 23nm gate length *n*-type SB-MOSFETs. Although the substrate boron doping concentration is 10^{15}cm^{-3}, short channel effect is

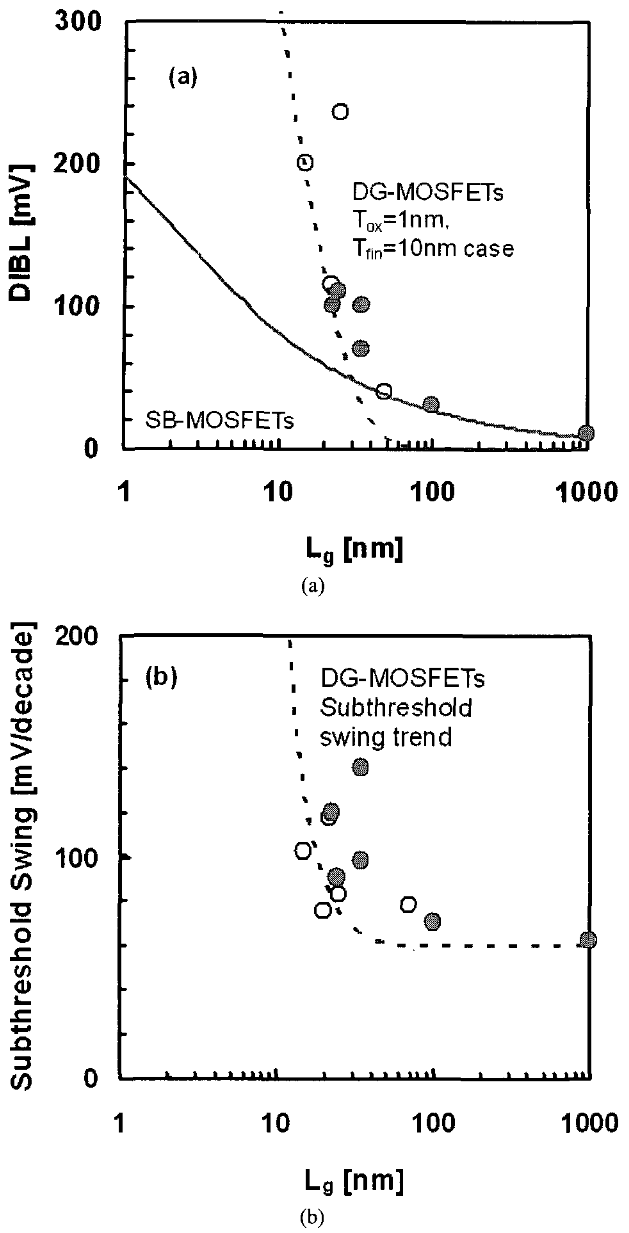


Fig. 8. DIBL (a) and Subthreshold Swing (b) characteristics of SB-MOSFETs

sufficiently suppressed due to the existence of Schottky barrier between source and channel. The existence of interface traps can severely affect the short channel characteristics in SB-MOSFETs, especially for the low doped substrate case due to the severe penetration of drain field into the source/channel interface. The penetration of drain field can cause the interface trap mediated leakage current, giving the degradation of SS value and leakage current characteristics.

Fig. 8 shows the DIBL (a) and SS (b) characteristics of SB-MOSFETs with the variation of gate length. In Fig. 8(a), solid and dotted line represents theoretical DIBL characteristics of SB-MOSFETs and DG-MOSFETs, respectively and the open circles are plotted from the published data [3] and the closed circles are the data from this work. The scaling theory of DG-MOSFETs can be found in [12]. In the calculations of DIBL in DG-MOSFETs, gate oxide and body thickness are assumed as 1nm and 10nm, respectively. Note that these assumed values correspond to the ultimate minimum values in device technology. The DIBL characteristics of SB-MOSFETs are better than DG-MOSFETs. The reason for this is due to the existence of the Schottky barrier between source and channel. This is explained in Fig.9. In DG-MOSFETs, the subthreshold characteristics, including DIBL and SS, are mainly determined by the built-in potential. In short channel device, as the drain voltage increases, built-in potential between source and channel decreases, giving DIBL effect. But in SB-MOSFETs, the subthreshold characteristics are mainly determined by the Schottky barrier. Thus DIBL characteristics of SB-MOSFETs can be described by the Schottky barrier lowering due to the drain voltage. In SB-MOSFETs, the decrease of threshold voltage with the increase of drain voltage, due to the Schottky barrier lowering, can be

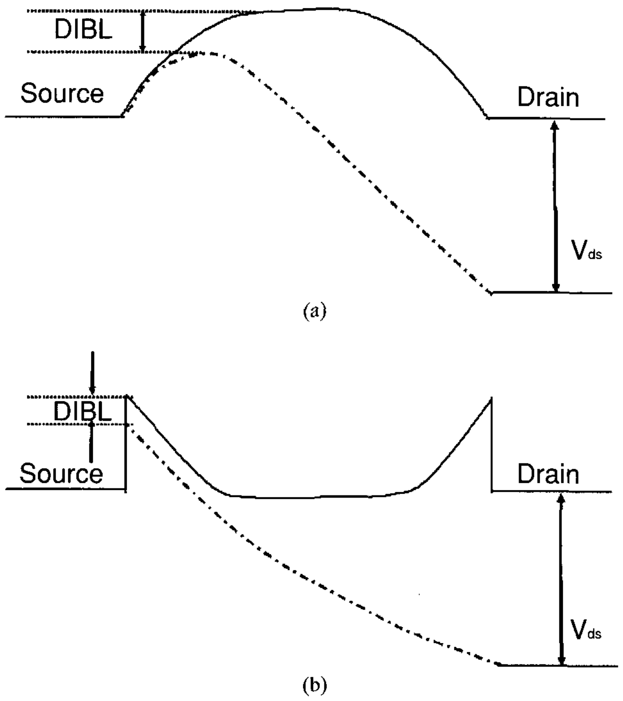


Fig. 9. Different DIBL mechanisms in MOSFETs (a) and SB-MOSFETs (b)

expressed as following.

$$\Delta V_T = \sqrt{\frac{q}{4\pi\varepsilon}}\left[\sqrt{\frac{V_{DS}^{\ H}}{L_{eff}}} - \sqrt{\frac{V_{DS}^{\ L}}{L_{eff}}}\right] \qquad (3)$$

where, L_{eff} means the effective gate length and V_{DS}^H and V_{DS}^L means high and low drain voltage, respectively.

In Fig. 8(b), dotted line represents theoretical SS characteristics of DG-MOSFETs, with 1nm gate oxide and 10nm body thickness. As shown, the SS characteristics of SB-MOSFETs are almost compatible with ultimately scaled DG-MOSFETs.

IV. CONCLUSIONS

Erbium-silicided Schottky diode is fabricated on the p-type silicon and the electrical characteristics is analyzed using the *I-V* and *C-V* measurement methods. From *I-V* analysis, the major leakage current conduction mechanism of reversely biased Schottky diode is due to the Frenkel-Poole emission originating from the existence of deep trap level in the depletion region of erbium-silicided Schottky diode. The trap density and lifetime are evaluated using equivalent circuit modeling method and the extracted trap density and lifetime are 1.5×10^{13} traps/cm^2 and 3.75 ms, respectively. The corrected Schottky barrier height (0.76 eV) is extracted by eliminating the parallel connected capacitance associated with trap using equivalent circuit modeling method. Also, SB-MOSFETs are manufactured and the electrical characteristics are analyzed. In SB-MOSFETs, DIBL is strongly suppressed due to the existence of Schottky barrier between source and channel. DIBL and SS characteristics of SB-MOSFETs are compatible with the ultimately scaled DG-MOSFETs which shows the possible application of SB-MOSFETs in nanoscale regime as the alternative to the MOSFETs.

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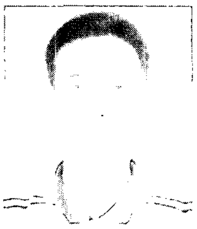

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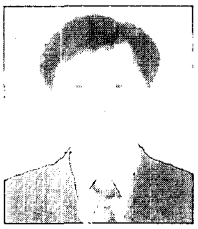

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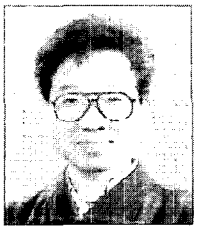

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