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Design and Analysis of Current Mode Low Temperature Polysilicon TFT Inverter/Buffer

Joon-Chang Lee[**] **and Ju Young Jeong**[*]

Abstract

We propose a current mode logic circuit design method for LTPS TFT for enhancing circuit operating speed. Current mode inverter/buffers with passive resistive load had been designed and fabricated. Measurement results indicated that the smaller logic swing of the current mode allowed significantly faster operation than the static CMOS. In order to reduce the chip size, both all pTFT and all nTFT active load current mode inverter/buffer had been designed and analyzed by HSPICE simulation. Even though the active load current mode circuits were inferior to the passive load circuits, it was superior to static CMOS gates.

Keywords : digital circuits, current mode, thin film transistor, simulation

1. Introduction

With the advancement of low temperature poly-silicon (LTPS) quality, thin film transistor (TFT) can be used to implement not only pixel switching function but also display drivers and digital logic blocks [1]. In addition, the system-on-glass, (SOG), which contains LTPS TFT-based microcontroller, memory, and graphic controller, is an acknowledged concept for next generation flat panel displays [2]. The advantages of SOG displays include lower cost, higher reliability, and higher design flexibility [3]. However, since the LTPS TFT's use lower quality silicon than bulk MOSFET's, device dimension and driving voltage are much higher than those of bulk MOSFET's. The latest development on SOG is the 8 MHz micro-processor built with 1um LTPS TFT process technology [4].

For bulk MOSFET, device scaling and other circuit techniques have been used to achieve circuit performance improvements but have provided only little improvement or non at all. But due to polycrystalline nature of the substrate, it is not easy to apply device scaling toLTPS TFTs.

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* Member, KIDS; ** Student Member, KIDS.
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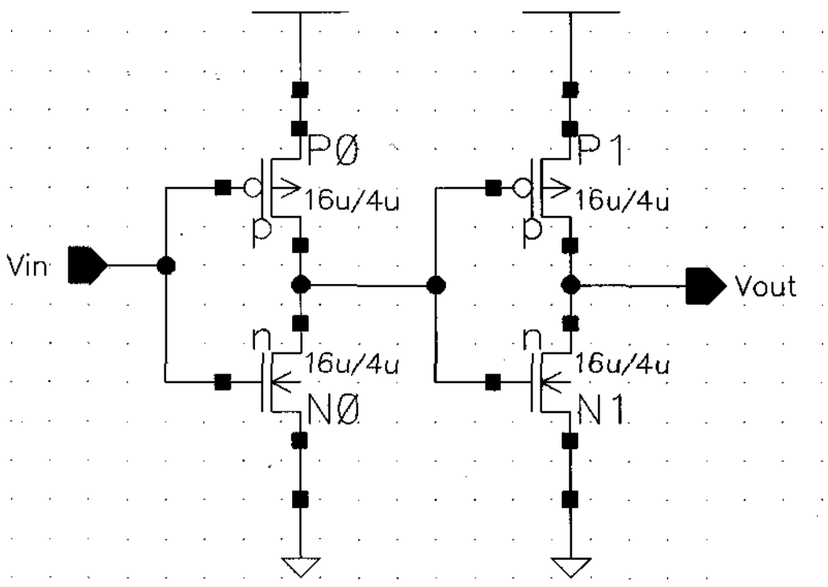
Corresponding Author : Ju-Young Jeong
Department of Electronic Engineering, The University of Suwon, Kyongki-do, 445-743, Korea.
E-mail : jyjeong@suwon.ac.kr **Tel** : +031 220-2168 **Fax** : +031 220-2494

So far, all digital blocks integrated in the SOG adopted CMOS design technique. Even though this is well established, it is more suited for bulk MOSFET circuits than LTPS TFT circuits. More specifically, LTPS TFT circuits needed to use higher Vdd and therefore, CMOS design style inevitably requires a high power consumption because of large logic swing. Furthermore, CMOS design style requires a large device width to achieve required current driving capability and speed.

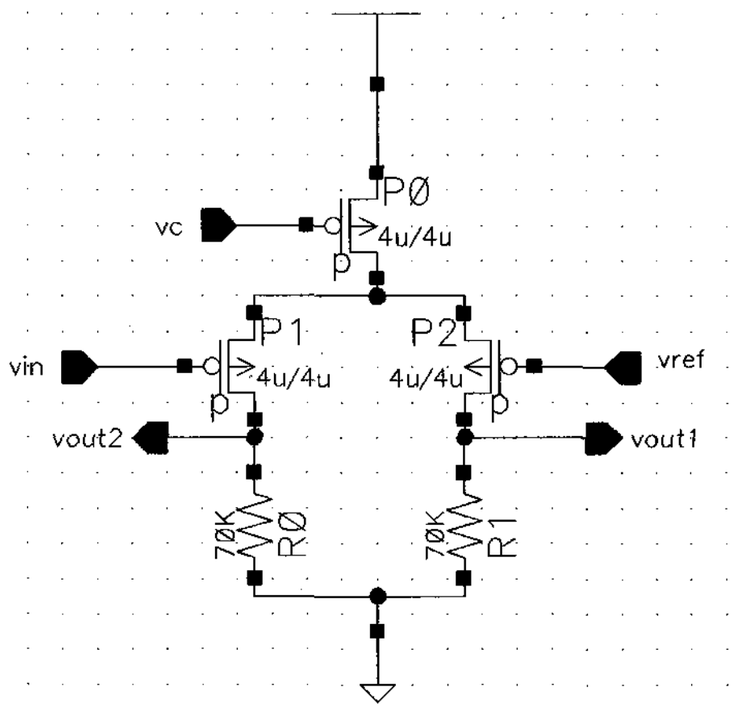
In this work, we report about the current mode LTPS TFT circuit design technique which can reduce chip area as well as logic swing. We have designed inverter/buffer with only p channel TFT's for process simplicity and hot carrier immunity.

2. Experiments

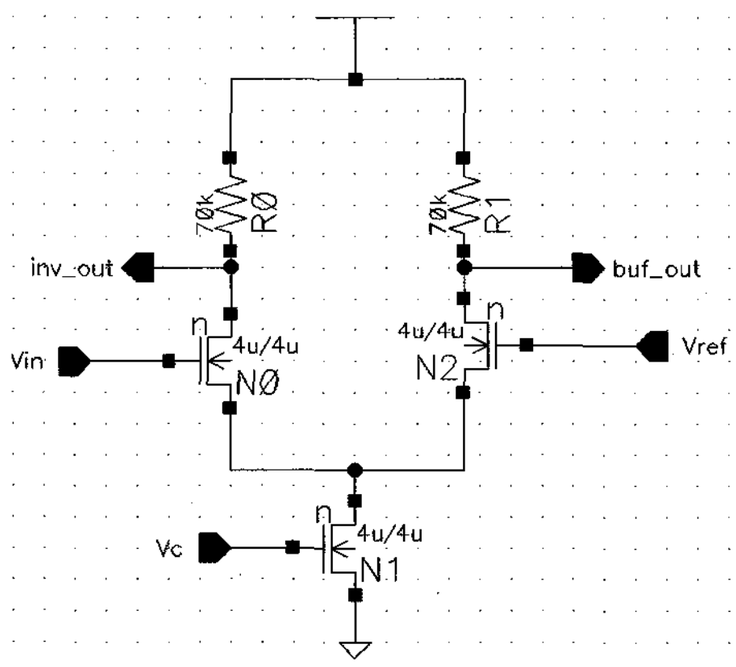
Fig. 1 shows typical inverters designed in CMOS and current mode logic. Current mode logic (CML) resembles the emitter coupled logic (ECL) in operation principle and are commonly used in high speed applications [5,6]. In ECL circuits, in order to minimize storage time, transistors are usually not allowed to operate in hard saturation. Similarly, we made MOSFET's in our CML circuits to stay on and steer the current through a path with lower resistance. In CML circuits, constant current source is important but since LTPS TFT's have severe threshold voltage fluctuation, device matching is difficult and



(a)



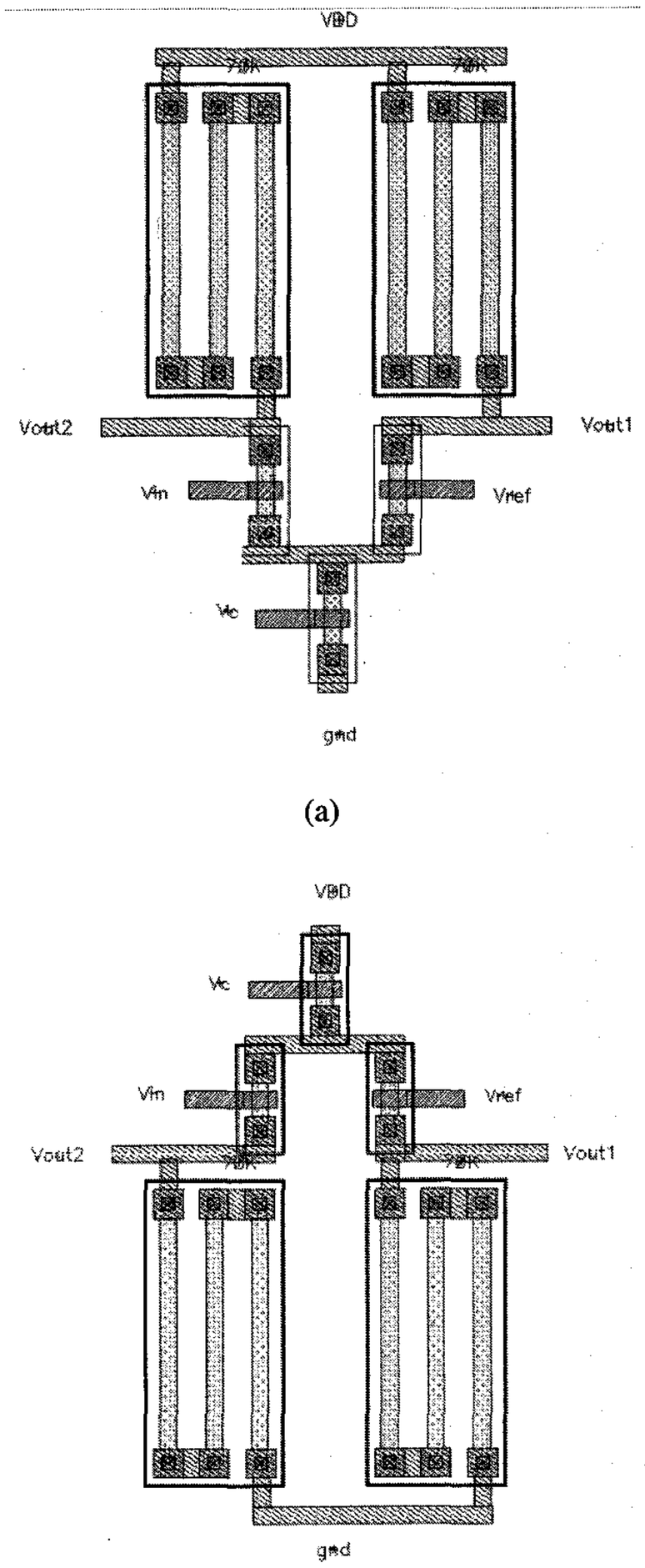
(b)



(c)

Fig. 1. Inverter/buffer structures. (a) Static CMOS, (b) pTFT CML, and (c) nTFT CML.

therefore, high quality current mirror is difficult to design. Instead, since input resistance of a TFT is infinite, we used single TFT as a current source in Figs. 1 (b) and (c). Note that we used only pTFT's in order to reduce the short



(a)

(b)

Fig. 2. Test panel layouts of CML inverters/buffer with resistors. (a) all nTFT case (b) all pTFT case.

channel effect and the floating body effect in Fig. 1 (b). Current source P0 in Fig. 1 (b) maintains a constant current through the branches of the circuit at all times. There are two current paths, as follows : 1) through P1 and R0, 2) through P2 and R1. Vc is constant DC Voltage and the reference voltage (Vref) is set to middle voltage of input signal (Vin) swing. When Vin is low, most of the current flow through path 1) because P1 turns on more strongly than P2. Output node (output_inv) increases due to voltage drop across the resistor R0. When Vin is high, most of

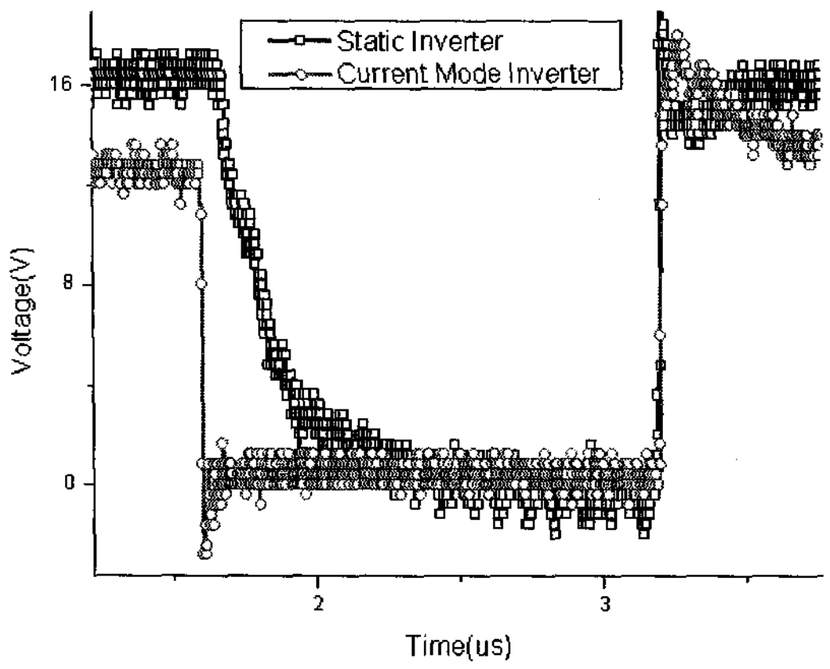


Fig. 3. Test panel measurement result of static CMOS TFT inverter and all pTFT current mode inverter/buffer. Current mode inverter data had been magnified by 3 for direct comparison.

Table 1. Test panel measurement result summary

	CMOS Logic	Current Mode Logic
Falling Propagation Delay (ns)	244	24
Falling Time (ns)	216	8
Rising Propagation Delay (ns)	30	34
Rising Time (ns)	20	10

current flow through path 2) and the output node becomes logic 0.

The output node voltage swing can be determined by the resistance of R0 and R1. With 70 Kohm resistors, we obtained reduced logic swing between 3 and 6 volts. It is also possible to design CML buffer/inverter with only n channel TFT's as shown in Fig. 1 (c). From this figure, note that the locations of the load and the current mirror are switched.

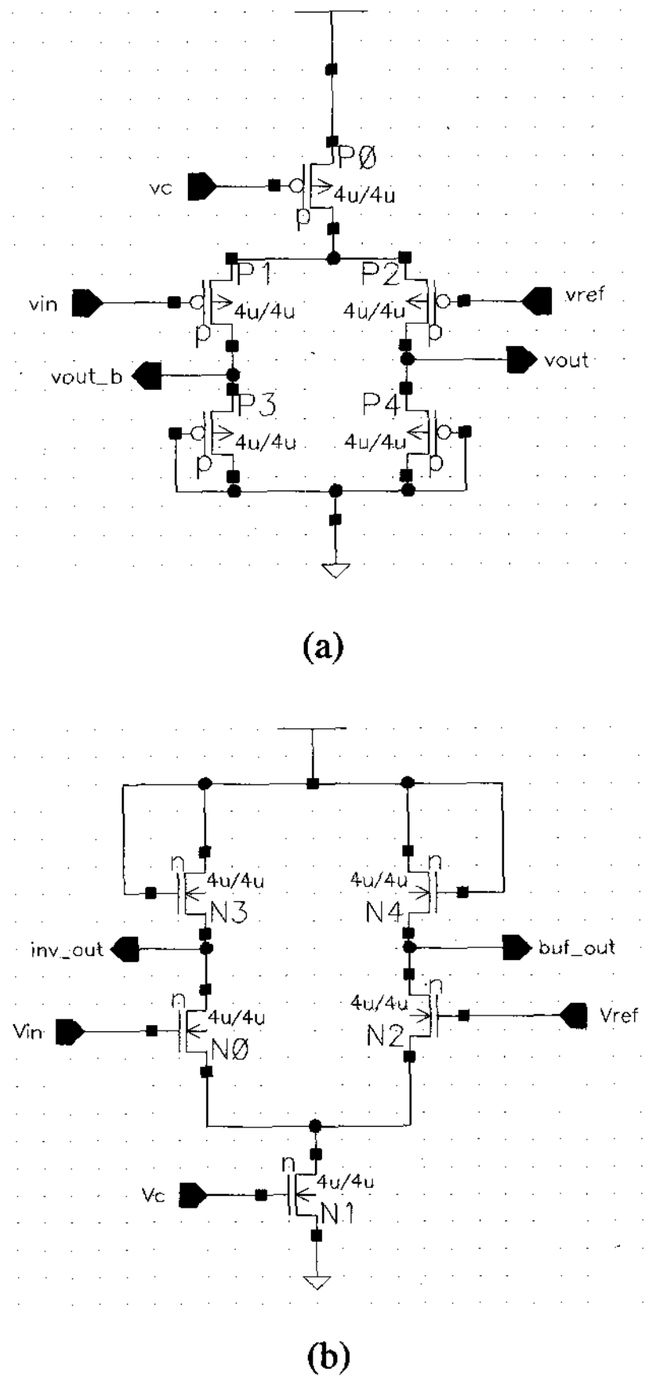
To confirm the circuit performance, we have designed and fabricated the logic circuits as shown in Fig. 1. Fig. 2 shows the layout of the current mode inverter/buffers. We have measured the switching behavior of both static CMOS and current mode TFT inverters as shown in Fig. 3 and the results are summarized in Table 1. Note that the current mode inverter data in Fig. 3 have been magnified by 3 for direct comparison. It is clear that the current mode inverter had superior delay characteristics especially in the falling edge.

3. Aanlysis

In order to examine the potential of the current mode logic, we used HSPICE to simulate the circuits tested and we used device parameters extracted from the TFT process which we used to make the test panel. Some key device parameters are summarized in Table 2. Furthermore, we designed current mode inverter/buffer with active loads for smaller chip area. Fig. 4 shows schematics of the gates in which we replaced the passive resistors with diode connected TFT's.

Table 2. Selected Device Parameters Extracted from 4um LTPS Process

Device Parameter	n-channel TFT	p-channel TFT
Mobility (cm^2/Vsec)	78	75
Threshold Voltage (V)	0.3	-1.0
Kink Voltage (V)	5.0	3.0
Gate Oxide Thickness (nm)	100	100



(a)

(b)

Fig. 4. CML inverter/buffer with active loads. (a) all pTFT, (b) all nTFT.

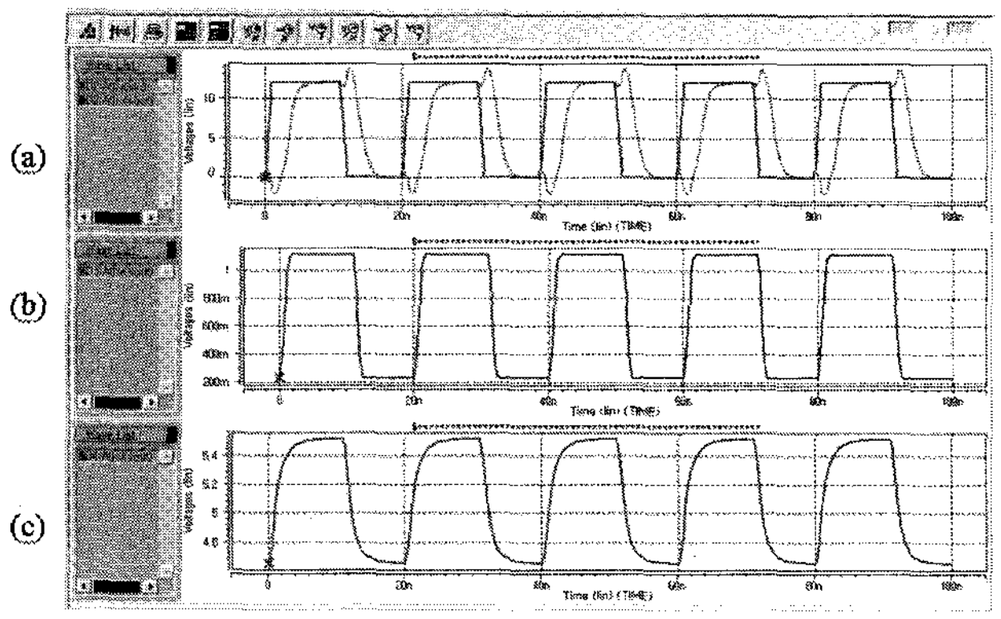


Fig. 5. Buffer outputs of (a) static CMOS (solid line: input, dotted line: output), (b) pTFT CML with resistors, (c) pTFT CML with active load.

Fig. 5 shows the simulation results of pTFT current mode inverter/buffer while Fig. 6 shows those of nTFT current mode inverter/buffer. For comparison, static CMOS buffer output is also included. From these results, first of all, it should be noted that the magnitude difference of the logic swing. In contrast to static CMOS which had 12 V logic swing, the current mode gates were able to operate with merely 1 volt logic swing. Secondly, the static CMOS case showed sudden voltage overshoot at the beginning of switching due to the kink effect in TFT. On the other hand, the current mode case had no undesirable transients since drain to source potential difference is small enough. Thirdly, the static CMOS charging/discharging rounded off at the end of the switching. Similar round offs were observed in the current mode inverter/buffers with active loads. This is inevitable since the current driving capabilities of the active loads drop significantly due to smaller Vds and Vgs at the end of switching.

Table 3 summarizes the simulation results. Since the static CMOS buffer was made of two inverter stages, propagation delay of each stage should be about 1.6 nsec. Rising and falling time a more direct measure of switching characteristics. For the static CMOS buffer, rising and falling time are 2.1 and 2.2 nsec, respectively. On the other hand, these values were around 1.2 and 0.9 nsec for nTFT and pTFT CML gate with passive loads, respectively. For active load CML gates, improvements in delay time were less obvious. But active load CML can be seen to consume much less area than both the CML with passive load and static CMOS. The sum of the gate area for the static CMOS buffer is 256 um^2 while that of the active load CML buffer

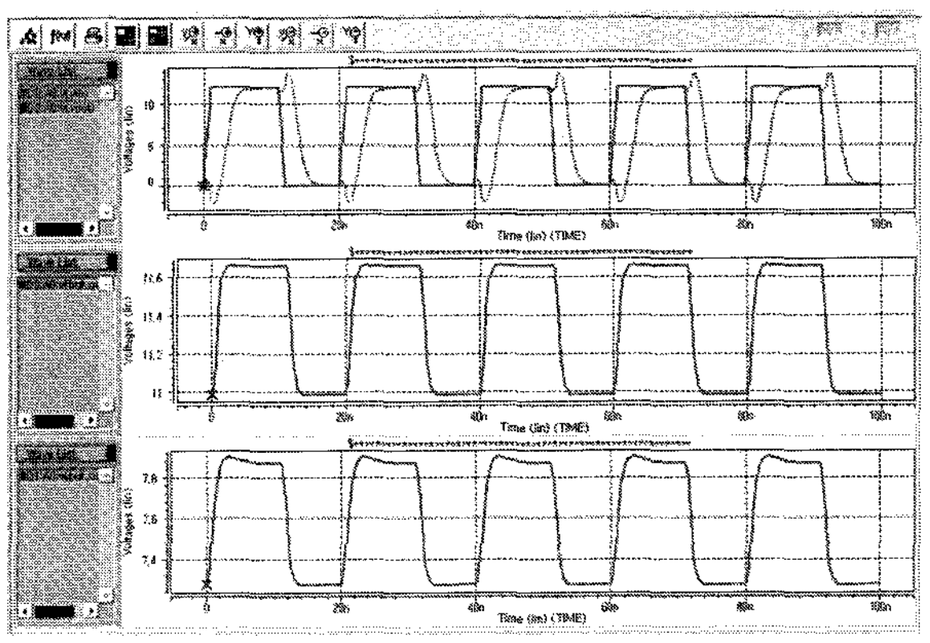


Fig. 6. Buffer outputs of (a) static CMOS (solid line: input, dotted line: output), (b) nTFT CML with resistors, (c) nTFT CML with active load.

Table 3. Performance Comparison between inverter/buffer structures (buffer output)

	Average Power (uW)	Propagation Delay Rising (ns)	Propagation Delay Falling (ns)	Rising Time (ns)	Falling Time (ns)
Static CMOS Circuit	1119	3.1	3.4	2.1	2.2
nTFT CML with resistors	432	0.32	0.38	1.2	1.23
nTFT CML with active loads	355	0.5	0.46	1.46	1.44
pTFT CML with resistors	535	0.3	0.16	0.9	0.91
pTFT CML with active loads	458	0.7	0.6	2.6	2.2

is 80 um^2. In summary, it is clear that the CML has a strong advantage in terms of speed and area while power consumption is comparable to the static CMOS. The comparable power consumption data was obtained according to device size and current level optimization.

4. Conculsion

In this study, we were able to demonstrate the usefulness of the current mode logic in TFT digital circuits and verified that one can improve operation speed by reducing the logic swing. Even though the current mode

operation consumes a significant amount of static current, the total power consumption can be made comparable to the static CMOS case through circuit optimization. We further showed that the current mode logic can be implemented with active loads and chip area can be reduced to a smaller size than that of the static CMOS. Lastly, we found that the current mode logic is kink free due to smaller potential differences between drain and source terminals.

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