

Hysteresis Characteristics in Low Temperature Poly-Si Thin Film Transistors

Hoon-Ju Chung[*a], Dae-Hwan Kim[b], and Byeong-Koo Kim[*b]

Abstract

The dependence of hysteresis characteristics in low temperature poly-Si (LTPS) thin film transistors (TFTs) on the gate-source voltage (Vgs) or the drain-source voltage (Vds) bias is investigated and discussed. The hysteresis levels in both p-type and n-type LTPS TFTs are independent of Vds bias but increase as the sweep range of Vgs increases. It has been found that the hysteresis in both p-type and n-type LTPS TFTs originated from charge trapping and de-trapping in the channel region rather than at the source/drain edges.

Keywords : thin film transistor, poly-Si, hysteresis, AMOLED, residual image

1. Introduction

Active matrix organic light emitting diode (AMOLED) displays have many advantages, such as wide viewing angle, fast response time, low cost, and thin thickness [1]. Recently, many companies have been trying to penetrate into the small-sized application market for mobile phones, personal digital assistances and digital still cameras.

However, there are still some critical issues that need to be resolved in order for AMOLED displays to be competitive in the display market. Such problems include reliability of OLED materials and TFTs and uniformity in electrical characteristics of driving TFTs. The non-uniformity in brightness of AMOLED display is induced by non-uniformity in electrical characteristics of driving TFTs. This is due to the fact that the luminance of pixels is too sensitive to the electrical characteristics of driving TFTs with the conventional pixel structure of two transistors and one capacitor. The degradation of OLED materials and driving TFTs causes the residual image, the variation of panel brightness, and color change in display panels. The residual image is classified into two types. One is irrecoverable residual image which is caused by the degradation of the OLEDs or driving TFTs with emitting time. The other is the recoverable residual image, which is related to the hysteresis of driving TFTs [4]. As a result, it is very important to understand the origin of the hysteresis in order to improve the recoverable residual image of AMOLED display.

In this paper, we investigate the hysteresis characteristics of p-type and n-type poly-Si TFTs with Vgs and Vds.

2. Fabrication

Poly-Si TFTs with a top coplanar structure were fabricated using excimer laser annealing method. SiO_2 buffer (3,000 Å) and a-Si:H (500 Å) were deposited on a glass substrate by plasma-enhanced chemical vapor deposition (PECVD). The a-Si:H film was crystallized by excimer laser annealing after dehydrogenation. Following the active layer patterning, the gate oxide (1,500 Å) and the gate metal (Mo) were deposited by PECVD and sputtering, respectively. After patterning the gate metal, n^- doping was performed to form a lightly doped drain (LDD) region and n+ and p+ doping were carried out using a PR mask to produce source and drain electrodes of complementary metal oxide semiconductor (CMOS) TFTs. Then, rapid thermal annealing was performed to activate the dopant. The interlayer was depostited by PECVD and contact holes

Manuscript received November 1, 2005; accepted for publication December 13, 2005.

* Member, KIDS.

This paper was supported by Research Fund, Kumoh National Institute of Technology.

Corresponding Author : Hoon-Ju Chung

[a] School of Electronic Engineering, Kumoh National Institute ofTech-nology, 1, Yangho-dong, Gumi, Gyeongbuk, 730-701, Korea.

[b] P-Si Process Integration Team, LG. Philips LCD Co., Ltd., Gumi, Gyeong buk, 730-726, Korea.

E-mail : hjchung@kumoh.ac.kr **Tel** : +054 478-7433 **Fax** : +054 478-7449

were formed using a buffered oxide etchant (BOE). The source/drain metals (Mo/AlNd/Mo) were deposited using sputtering. Then, the SiNx film was deposited for passivation. After contact holes were formed in the passivation layer, the indium thin oxide (ITO) was deposited and patterned for pixel electrodes. The electrical properties were measured using a HP 4155A parameter analyzer.

3. Hysteresis Characteristics

Fig. 1 shows the Ids-Vgs transfer characteristics for forward gate voltage sweep (Vgs sweep from 15 V to –20 V) and reverse gate voltage sweep (Vgs sweep from -20 V to 15 V) in p-type poly-Si TFT. As shown in Fig. 1, the difference in the threshold voltage (Vth) is indicated by the gate voltage sweep direction. The figure shows that the |Vth| of reverse gate voltage sweep is larger than that of forward gate voltage sweep.

In MOS structure, the potential balance equation can be expressed as follows,

$$V_{GB} = \psi_{ox} + \psi_s + \phi_{MS}$$

where, V_{GB} is the externally applied voltage between the gate and the silicon, ψ_{ox} is the potential drop across the oxide, ψ_s is the surface potential, and ϕ_{MS} is the difference in the work function of the metal and the silicon, respectively. Because ϕ_{MS} is a known constant, any change in V_{GB} must be balanced by changes in ψ_{ox} and ψ_s:

$$\Delta V_{GB} = \Delta\psi_{ox} + \Delta\psi_s$$

The charges in MOS structure must be balanced for the overall charge neutrality as follows,

$$Q_G' + Q_O' + Q_C' = 0$$

where, Q_G' is the charge per unit area on the gate, Q_O' is the effective interface charge per unit area, and Q_C' is the charge per unit area in the semiconductor under the oxide, respectively. If the charges per unit area in the semiconductor have the same value for the same drain current, the charge balance equation can be written as [5]

$$\Delta Q_G' + \Delta Q_O' = 0.$$

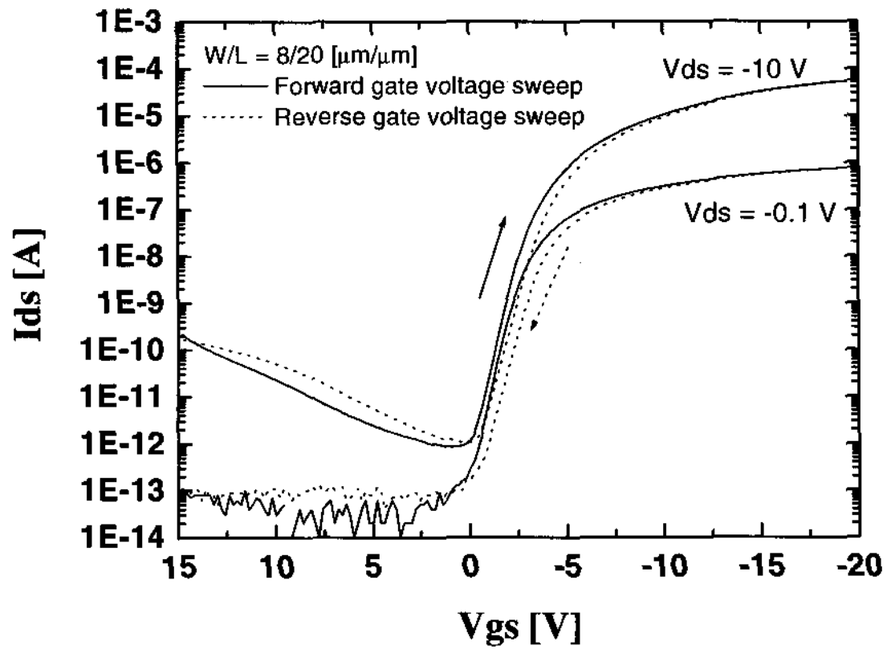
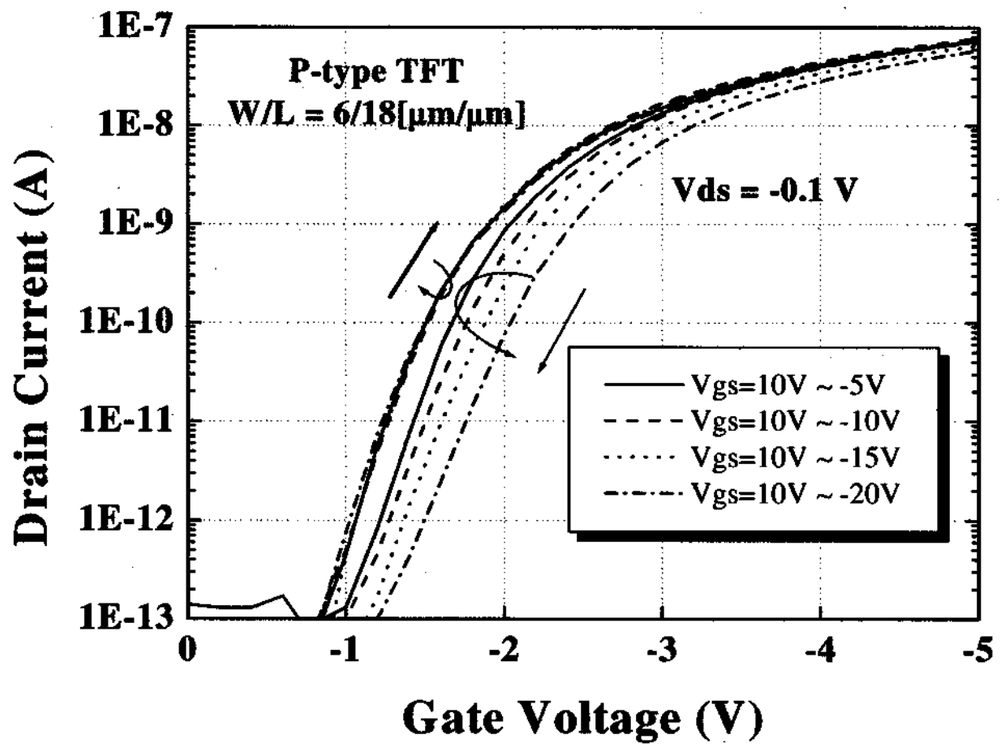


Fig. 1. Ids-Vgs transfer characteristics for changing the sweep direction of Vgs in p-type poly-Si TFT.

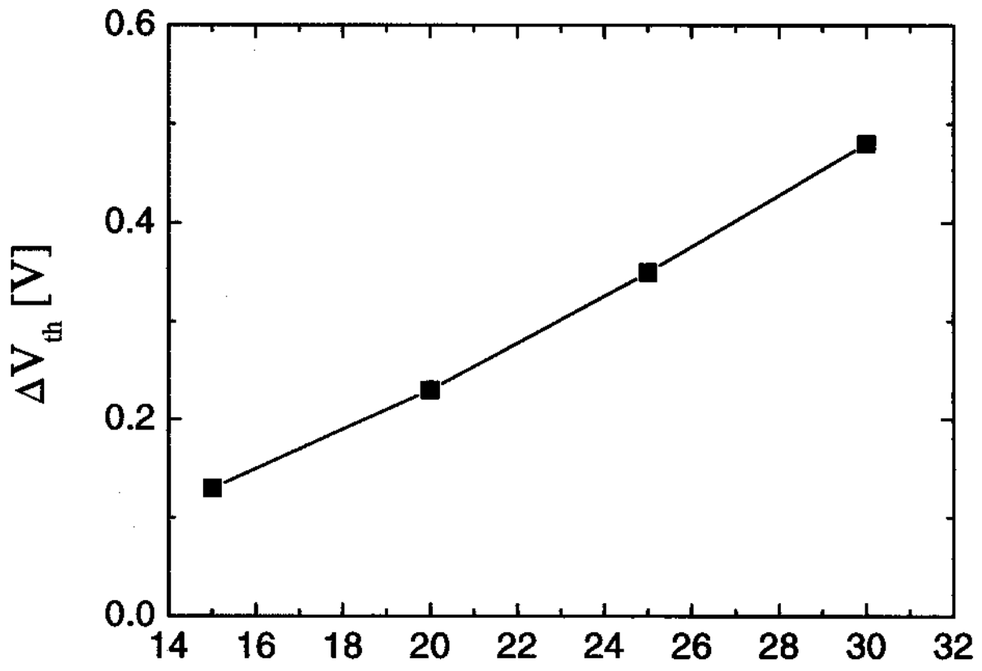
The difference in the threshold voltage according to the gate voltage sweep direction, can be explained by the effective interface charge. The hysteresis of p-type poly-Si TFT is induced by hole trapping in the oxide trap states and interface trap states between the poly-Si layer and gate insulator [6, 7]. Holes can be trapped and de-trapped repeatedly depending on the applied voltage. As hole trapping occurs at the negative starting gate voltage under a condition, so called a reverse gate voltage sweep, the transfer characteristics exhibit a parallel shift toward the negative voltage. This causes, the |Vth| to increase and the channel current to decrease in proportion to the quality of the trapped charge. For positive starting voltage in the forward gate voltage, the trapped charge should be de-trapped, which would cause the |Vth| to decrease and the channel current increase.

In order to investigate the dependence of hysteresis level on Vgs, the negative voltage of forward and reverse gate voltage sweeps was changed from –5 V to –20 V in steps of -5 V. Hysteresis level is defined as the difference in the threshold voltage measured for changing the gate voltage sweep direction.

Fig. 2 shows the Ids-Vgs transfer characteristics and hysteresis levels for various sweep ranges of Vgs in p-type poly-Si TFTs. The transfer characteristics for the forward gate voltage sweep conditions have the same shapes because they have the same starting voltage of the forward gate voltage sweep. However, the transfer characteristics for reverse gate voltage sweep conditions show a parallel shift toward the negative voltage due to hole trapping increment as the negative voltage of reverse Vgs sweep decreases. This causes, the hysteresis level increases as the sweep range of Vgs to increase.



(a)

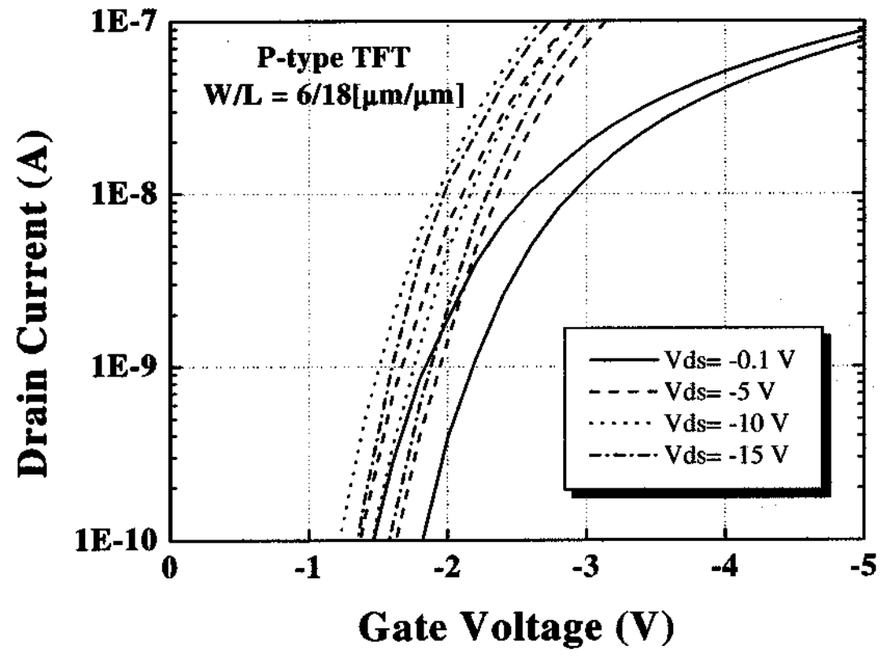


(b)

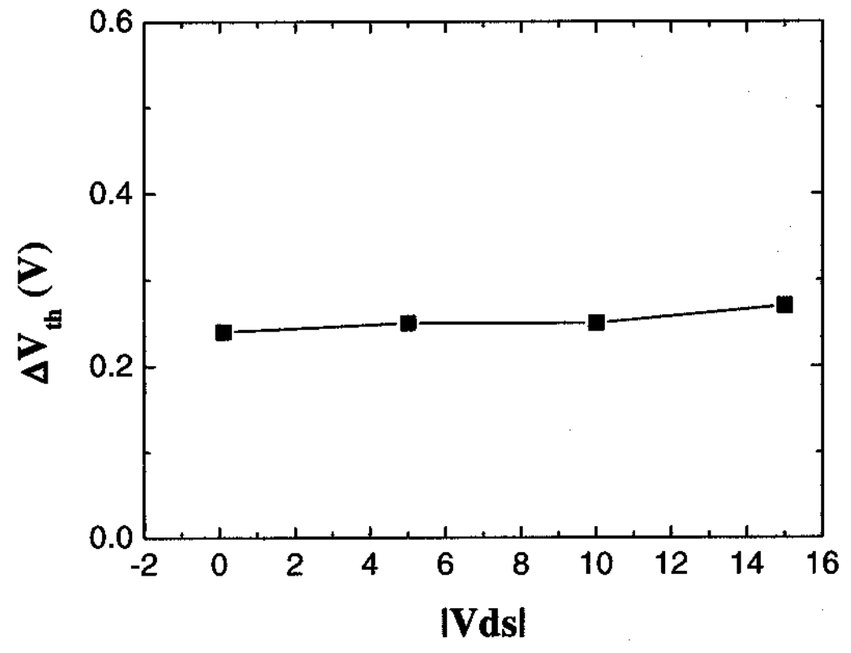
Fig. 2. Ids-Vgs characteristics (a) and Hysteresis levels (b) for various sweep range of Vgs in p-type Poly-Si TFT.

Fig. 3 shows the Ids-Vgs characteristics and hysteresis levels for various Vds conditions in p-type poly-Si TFTs. As |Vds| bias increases, both transfer characteristics for forward and reverse Vgs sweeps show a shift toward positive voltage and the hysteresis level remains unchanged.

Fig. 4 shows the Ids-Vgs transfer characteristics and hysteresis levels for various sweep ranges of Vgs in n-type poly-Si TFTs. The threshold voltage of forward gate voltage sweep (Vgs sweep from negative voltage to positive voltage) is smaller than that of reverse gate voltage sweep (Vgs sweep from positive voltage to negative voltage) in n-type poly-Si TFT. As electron trapping occurs at positive starting gate voltage in the reverse gate voltage sweep, the transfer characteristics exhibit a parallel shift



(a)

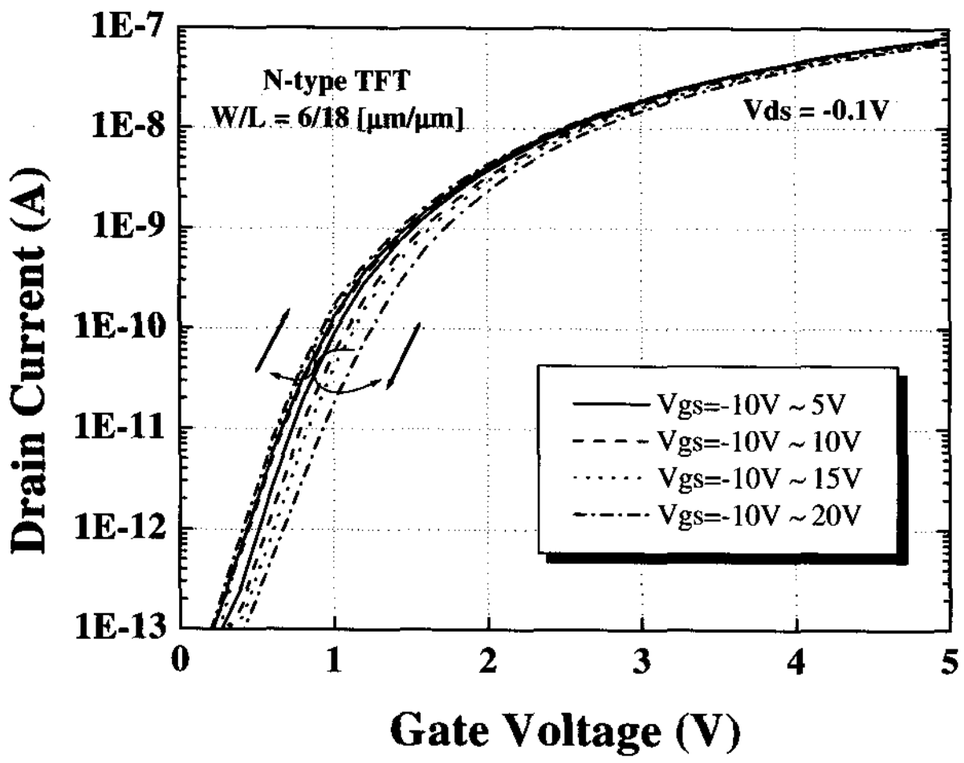


(b)

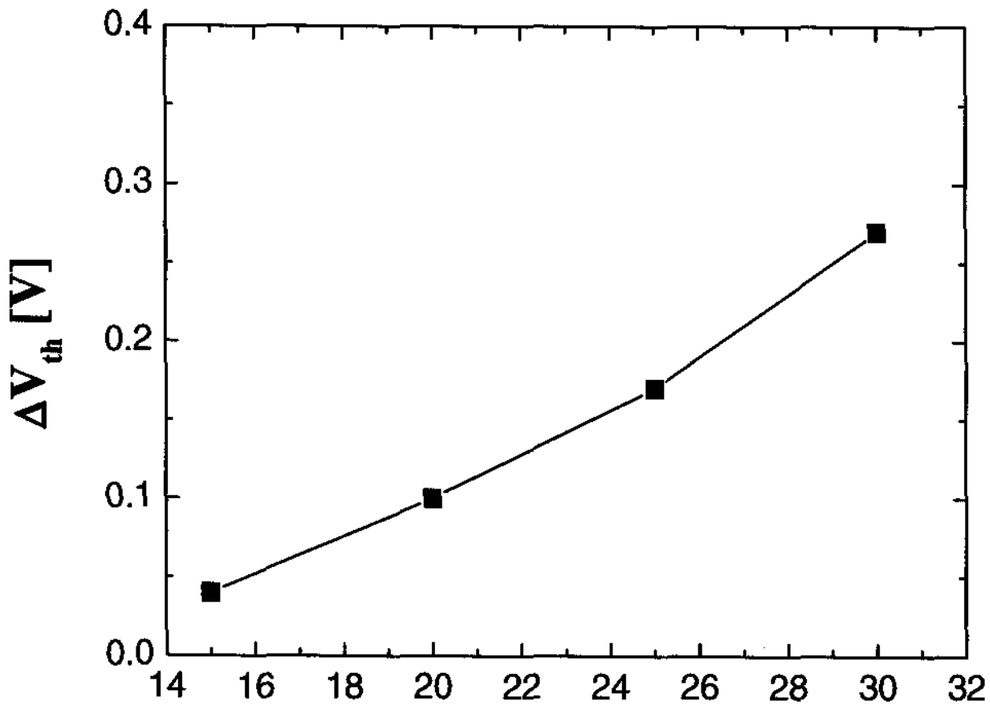
Fig. 3. Ids-Vgs characteristics (a) and Hysteresis levels (b) for various Vds conditions in p-type poly-Si TFT.

toward the positive voltage. Therefore, the threshold voltage increases and the channel current decreases in proportion to the quality of the trapped charge. For negative starting voltage in the forward gate voltage, the trapped charge is de-trapped and the threshold voltage decreases and the channel current increases. The transfer characteristics for the forward Vgs sweep conditions have the same shapes due to the same starting voltage of the forward gate voltage sweep. However, the transfer characteristics for reverse gate voltage sweep conditions show a parallel shift toward positive voltage due to the increase in the electron trapping as the positive voltage of reverse Vgs sweep increases. Therefore, the hysteresis level increases as the sweep range of Vgs increases.

Fig. 5 shows the Ids-Vgs characteristics and hysteresis levels for various Vds conditions in n-type poly-Si TFTs. As Vds bias increases, both transfer characteristics for

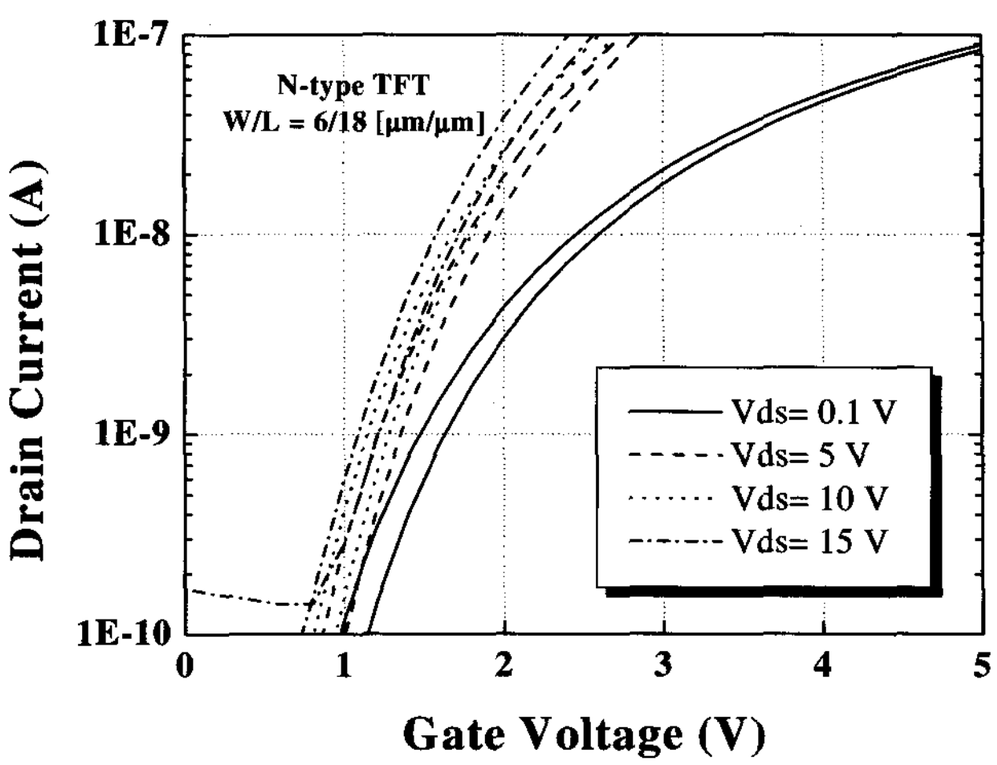


(a)

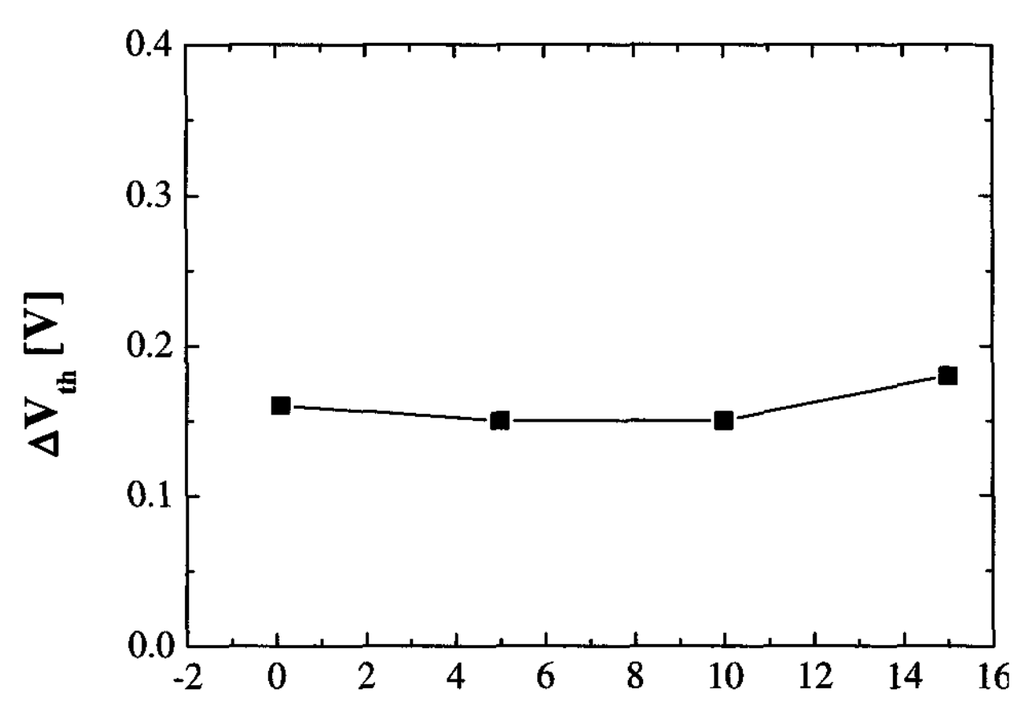


(b)

Fig. 4. Ids-Vgs characteristics (a) and Hysteresis levels (b) for various sweep range of Vgs in n-type Poly-Si TFT.



(a)



(b)

Fig. 5. Ids-Vgs characteristics (a) and Hysteresis levels (b) for various Vds conditions in n-type poly-Si TFT.

forward and reverse Vgs sweeps show a shift toward negative voltage and the hysteresis level is not changed.

In summary, the hysteresis in n-type and p-type LTPS TFTs are dependent on the applied Vgs sweep ranges but independent of the applied Vds bias values. The hysteresis in p-type and n-type poly-Si TFTs are induced by the charge trapping in the channel region rather than by that at source/drain edges. In order to solve the recoverable residual image problem in AMOLED displays, the hysteresis of driving TFTs should be reduced or a pixel structure, which can compensate the dependence of threshold voltage on Vgs bias, including the current mirror pixel structure, the current copy pixel structure, and the self-compensated voltage programmed pixel structure, should be applied.

4. Conclusions

We investigated the dependence of hysteresis characteristics of driving TFTs on Vgs or Vds. The hysteresis for forward and reverse gate voltage sweep was found to be caused by the changes in effective fixed oxide charge concentration induced by the trapping and de-trapping of carrier charges. The hysteresis level was found to increase as the sweep range of Vgs increased. However,

it was also found that the hysteresis level is independent of the applied Vds values. This means that the recoverable residual image problem can be resolved by adopting the pixel structures that can compensate the dependence of threshold voltage on Vgs bias.

References

[1] N. C. van der Vaart, H. Lifka, F. Budzelaar, J. Rubingh, J. Hoppenbrouwers, J. F. Dijksman, R. Verbeek, R. van Woudenberg, F. J. Vossen, M. Hiddink, J. Rosink, T. Bernards, and A. Giraldo, N. D. Young, D. A. Fish, M. J. Childs, W. A. Steer, D. Lee, and D. S. George, in *SID '04 Digest* (2004), p. 1284. R. Dawson, Z. Shen, D. A. Furst, S. Connor, J. Hsu, M. G. Kane, R. G. Stewart, A. Ipri, C. N. King, P. J. Green, R. T. Flegal, S. Pearson,W. A. Barrow, E. Dickley, K. Ping, S. Robinson, C. W. Tang, S. Van Slyke, F. Chen, J. Shi, J. C. Sturm, and M. H. Lu, in *SID '98 Digest* (1998), p. 11.

[2] T. Sasaoka, M. Sekiya, A. Yumoto, J. Yamada, T. Hirano, Y. Iwase, T. Yamada, T. Ishibashi, T. Mori, M. Asano, S. Tamura, and T. Urabe, in *SID '01 Digest* (2001), p. 384.

[3] B. K. Kim, O. Kim, H. J. Chung, J. W. Chang, and Y. M. Ha, *Jpn. J. Appl. Phys.* **43**, L4892, (2004).

[4] Y. Tsividis, *Operation and Modeling of the MOS Transistor* (McGRAW-Hill, Singapore, 1999) 2nd Ed., p. 56.

[5] K. Chatty, S. Banerjee, T. P. Chow, and R. J. Gutmann, *IEEE Electron Device Lett.* **23,** 330, (2002).

[6] K. N. Manjularani, V. R. Rao, and J. Vasi, *IEEE Trans. Electron Devices* **50,** 973, (2003).