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Pentacene-based Thin Film Transistors with Improved Mobility Characteristics using Hybrid Gate Insulator

Chang-Bum Park[**], Keum-Dong Jung[**], Sung Hun Jin[**], Byung-Gook Park[*], and Jong Duk Lee[*]

Abstract

Hybrid insulator pentacene thin film transistors (TFTs) are fabricated with thermally grown oxide and cross-linked polyvinylalcohol (PVA) including surface treatment by dilute ploymethylmethacrylate (PMMA) layer on n^+ doped silicon wafer. Through the optimization of SiO_2 layer thickness in hybrid insulator structure, carrier mobility is increased to more than 35 times than that of the TFT which has only a gate insulator of SiO_2 at the same electric field. The carrier mobility of 1.80 cm^2/V-s, subthreshold swing of 1.81 V/decade, and I_{on}/I_{off} current ratio > 1.10×10^5 are obtained less than -30 V bias condition. The result is one of the best reported performances of pentacene TFTs with hybrid insulator including cross-linked PVA layer as a gate insulator at relatively low voltage operation.

Keywords : pentacene, organic thin film transistors (TFTs), hybrid gate insulator, PMMA, PVA

1. Introduction

In recent years, extensive efforts have been put into enhancing the performances of organic thin film transistors (OTFTs) [1,2] for various applications such as flexible circuits [3], radio-frequency identification tags [4] and sensors [5]. Accordingly, there is great demand for high carrier mobility of devices for these applications. One of the most effective method to enhance the electrical characteristics of OTFTs is to select gate dielectric layer with various materials [6].

In this paper, we propose the hybrid insulator structure with cross-linked PVA, SiO_2 and PMMA layer for the transistors to increase carrier mobility of TFTs and merge the influences of each insulator.

Among the various gate insulator materials, cross-linked PVA was adopted as a polymer gate insulator because of its high-k characteristics [7], photosensitivity [8] and good surface alignment effect [8]. Additionally, the surface treatment of cross-linked PVA was performed by using dilute PMMA solution to modify the surface state of gate dielectric layer. This method provides a similar termination to silicon single crystals on which hydrocarbons are chemisorbed [9] to reduce heterogeneous nucleation facilitating grain growth [9]. In addition, SiO_2 was adopted as a barrier layer to reduce carrier injection from gate electrodes and enhance the saturation characteristics in hybrid structure.

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[*] Member, KIDS ; [**] Student Member, KIDS.
Corresponding Author : Chang Bum Park
Inter-University Semiconductor Research Center and School of Electrical Engineering, Seoul Natinal University San 56-1, Shinlim-dong, Kwanak-gu, Seoul, 151-742, Korea
E-mail : bum319@snu.ac.kr **Tel** : +2 880-7282 **Fax** : +2 882-4658

2. Device Fabrication

The top contact transistors were fabricated on n^+ doped silicon wafers, which were used as gate electrodes. Silicon wafers were thermally oxidized to obtain to be 8 nm, 40 nm, and 100 nm thickness of SiO_2 which serve as the inorganic gate dielectrics. The PVA solution with ammonium dichromate photosensitizer was spin-coated on the SiO_2 layers to serve as a 500 nm thick polymer gate dielectric layer also. The coated PVA was exposed with UV light and heated at 110 ℃ for 5 hours in a convection oven to define gate insulator and make cross-linking PVA's molecules, respectively. The dielectric constant of cross-linked PVA was measured to be ε=5.1 at 10 kHz frequency in our capacitors.

For the surface modification, a 8 nm thick PMMA layer was formed onto the cross-linked PVA layer by spin-coating process and it was baked at 110 ℃ for 30 minutes. In a final step, a 50 nm thick pentacene film was deposited

using a thermal evaporation system, keeping the substrate temperature as 80 ℃ and deposition rates within the range of 0.5-1.0 Å/s. Afterward, gold was thermally evaporated on top of the pentacene layer using shadow masks giving transistors with 25 μm channel length and 1000 μm width. The cross-section of the device is sche-matically shown in Fig. 1.

3. Electrical Characteristics and Discussion

Fig. 2 shows the transfer characteristics of our hybrid insulator pentacene TFTs under three different gate dielectric conditions. During the gate bias sweeping from +5 V to -30 V, the drain voltage was held constant at -30 V to keep the devices in saturation. The carrier mobility and threshold voltage were calculated from the slope of the plot of $|I_D|^{1/2}$ versus V_{GS} at -30 V of gate voltage in Fig. 2. The extracted values of electrical parameters for the devices are summarized in Table 1. As shown in the insets of Fig. 2 and

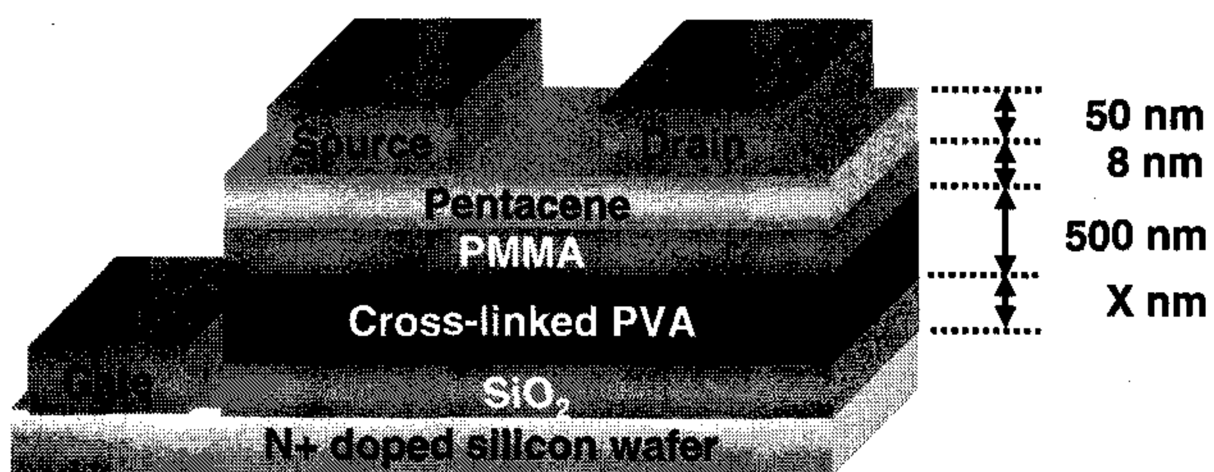

Fig. 1. Device structure of hybrid insulator OTFTs with SiO_2, cross-linked PVA and PMMA layers. W/L = 1000/25 (μm).

Table 1. Summary of the electrical parameters for the three hybrid insulator OTFTs according to the different SiO_2 thickness in hybrid insulator (X nm SiO_2/500 nm cross-linked PVA/8 nm PMMA). The first column stands for the thickness ratio of cross-linked PVA versus SiO_2 layer thickness in hybrid structure

Ratio of cross-linked PVA vs. SiO_2	T_{ox} (nm)	μ_{eff} (cm^2/V-s)	V_{th} (V)	I_{on}/I_{off} ratio	SS (V/dec)
5:1	100	0.25	- 15.2	6.9×10^4	2.92
12.5:1	40	0.53	- 15.0	8.0×10^4	2.28
62.5:1	8	1.80	- 14.9	1.1×10^5	1.81

Table 1, the noticeably improved drain current and carrier mobility was inspected according to the reduction of SiO_2 layer thickness in hybrid insulator.

For the case of less than -30V bias condition, a pronounced result was extracted from the sample A (8 nm SiO_2 + 500 nm cross-linked PVA + 8 nm PMMA): the carrier mobility of 1.80 cm^2/V-s, sub-threshold swing of 1.81 V/decade, and I_{on}/I_{off} current ratio > 1.10×10^5 were obtained. Since the carrier mobility of OTFTs is influenced by gate bias [10], the result is one of the best results ever

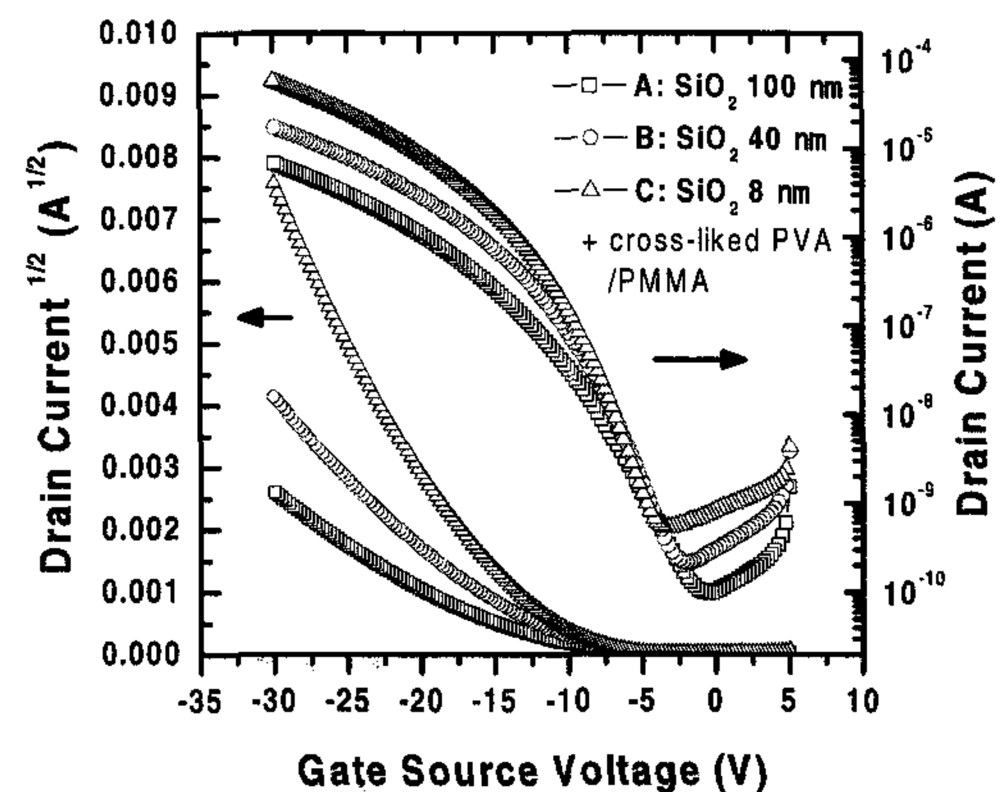

Fig. 2. Electrical transfer characteristics of split hybrid insulator OTFTs. sample A: SiO_2 (100 nm)/PVA (500 nm)/PMMA (8 nm), sample B: SiO_2 (40 nm)/PVA (500 nm)/PMMA (8 nm), and sample C: SiO_2 (8 nm)/PVA (500 nm)/PMMA (8 nm).

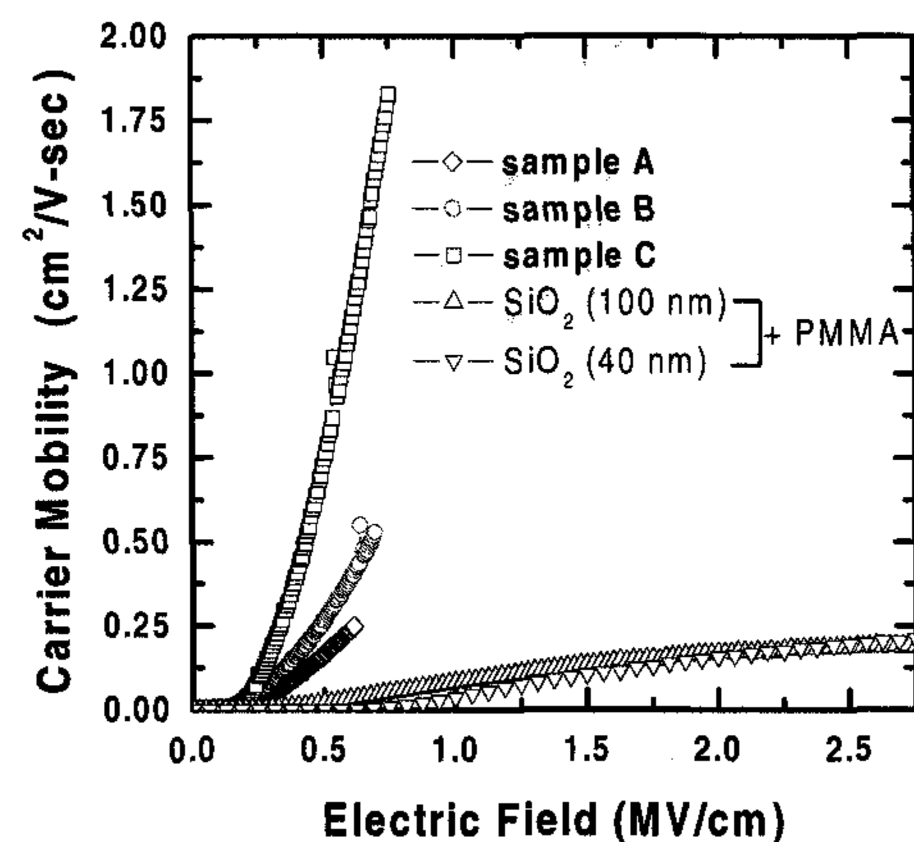

Fig. 3. Carrier mobility versus gate electric field for sample A, B and C using split hybrid insulator structures (SiO_2 (X nm)/PVA (500 nm)/PMMA (8 nm)) and PMMA treated SiO_2 insulator devices (40 nm and 100 nm). The thickness ratio of cross-linked PVA vs. SiO_2 in hybrid insulator devices: sample A = 5:1, B = 12.5:1, and C = 62.5:1 for 100 nm, 40 nm, and 8 nm thick SiO_2 layer, respectively.

reported of hybrid insulator pentacene TFTs including cross-linked PVA gate dielectric material at relatively low voltage operation.

To further investigate the cross-linked PVA effect and equivalent comparison between the gate dielectric condition and carrier mobility, we investigated the correlation between carrier mobility and gate electric field for the same structured samples shown in Table. 1 and the two kinds of devices with PMMA treated 40 ㎚, and 100 ㎚ thick SiO_2 gate dielectric layers. The result of the comparison is shown in Fig. 3.

From this figure, we can see that the carrier mobilities of 0.238, 0.402 and 1.139 cm^2/V-sec were extracted at 0.6 MV/cm gate electric field in hybrid insulator devices which correspond to the thickness ratio of cross-linked PVA vs. SiO_2 of 5:1 (sample A), 12.5:1 (sample B), and 62.5:1 (sample C) in hybrid insulator, respectively. The optimum-device sample C shows mobility that is 35 times greater than that of the TFTs only with PMMA treated 100 nm thick SiO_2 gate insulator at the same gate electrical field by using the hybrid insulator which has 62.5 times larger cross-linked PVA portion than SiO_2 thickness. Meanwhile, a slight mobility change is observed in the devices using PMMA treated SiO_2 insulator (40 ㎚ and 100 ㎚) only. These results prove a the cross-linked PVA is an effective gate dielectric layer that greatly enhances carrier mobility at the same electric field condition in hybrid insulator OTFTs.

4. Conclusion

In this paper, we proposed a new hybrid insulator structure with thermally grown oxide and cross-linked PVA layer including PMMA treatment to increase carrier mobility of pentacene TFTs. Through the optimization of hybrid insulator by the reduction of SiO_2 layer thickness, we enhanced the carrier mobility of devices to more than 35 times of the magnitude than that of SiO_2 insulator devices. Additionally, the effect of cross-linked PVA in terms of increasing carrier mobility was fairly proven by comparing the carrier mobility with gate electric field for the devices with different thickness ratios of cross-linked PVA and SiO_2 layer in hybrid insulator.

From the optimum devices with SiO_2 (8 ㎚) + cross-linked PVA (500 ㎚) + PMMA (8 ㎚) hybrid insulator structure, the carrier mobility of 1.80 cm^2/V- s, subthreshold swing of 1.81 V/decade, and I_{on}/ I_{off} current ratio > 1.10×10^5 were obtained at relatively low bias (less than -30 V) condition.

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