A Low Jitter and Fast Locking Phase-Lock Loop with Adaptive Bandwidth Controller

Youn-Gui Song, Young-Shig Choi, *Member, KIMICS*

Abstract—This paper presents the analog adaptive phase-locked loop (PLL) architecture with a new adaptive bandwidth controller to reduce locking time and minimize jitter in PLL output for wireless communication. It adaptively controls the loop bandwidth according to the locking status. When the phase error is large, the PLL increases the loop bandwidth and reduces locking time. When the phase error is small, the PLL decreases the loop bandwidth and minimizes output jitters. The adaptive bandwidth control is implemented by controlling charge pump current depending on the locking status. A 1.28-GHz CMOS phase-locked loop with adaptive bandwidth control is designed with 0.35 μ m CMOS technology. It is simulated by HSPICE and achieves the primary reference sidebands at the output of the VCO are approximately -80dBc.

Index Terms— Phase Locked Loop, Fast Locking, Adaptive Bandwidth, Low Jitter,

I. INTRODUCTION

In order to meet the growing demand for wireless communication, it is preferable to implement PLL in CMOS process with other transceiver circuits. Due to the close separation between the channels in wireless communication systems, phase-locked loops (PLL's) are required to generate low-noise or low-jitter frequency and at the same time needed to achieve fast locking [1].

Conventional analog PLL's use various methods such as a gear shifting or a lock detection scheme to achieve low jitter and fast locking [2], [3]. These PLL's can not respond properly to unpredictable phase fluctuation because it is operated with a pre-stored charge-pump current. An analog PLL with adaptive bandwidth control was proposed to be used under a time-varying noise environment. But it still requires a complicated analog adaptive controller with a reference voltage circuit [1].

The design of PLL's must generally deal with a tight trade off between the locking time and the amplitude of the ripple on the oscillator control line [4]. This paper presents the analog adaptive phase-locked loop architecture capable of varying loop bandwidth to reduce locking time and minimize jitter which is caused by the the VCO control line for wireless communication.

A new adaptive bandwidth controller adaptively controls the loop bandwidth according to the locking status. When the phase error is large, the PLL increases the loop bandwidth and reduces locking time. When the phase error is small, the PLL decreases the loop bandwidth and minimizes output jitters. Section II of the paper, the jitter of PLL output is discussed. Section III describes the proposed charge pump PLL. The simulation results and conclusion are described in section IV and section V.

II. THE JITTERS IN CHARGE PUMP PLL

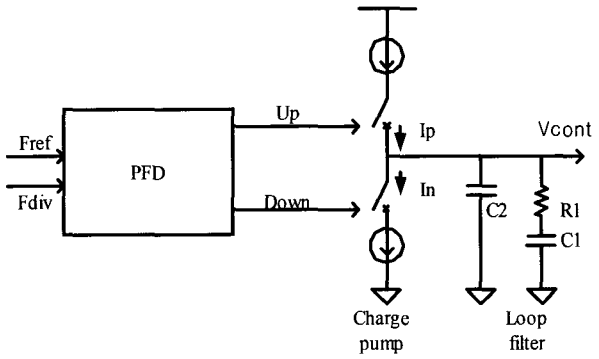


Fig. 1 Basic concept of charge pump PLL

Fig. 1 shows the charge pump and loop filter circuits used in PLL's. The combination of a phase-frequency detector and a charge pump is widely used in PLL's, because of its frequency-sensitive error signal, that can aid acquisition when the loop is out of the lock. The Up and Down pulses are used to switch the currents sources in the charge pump. When Up is active, a current with magnitude of I_p is sourced by the charge pump; conversely, when Down is active, a current with magnitude of I_n is sunk into the charge pump. When both Up and Down pulses are inactive, no current flows into or out of the output node of the charge pump. The output is high impedance node, under all circumstances. Resistor R_1 provides the stabilizing zero and capacitance C_2 suppresses the jitters generated by charge pump at every phase comparison instant.

The jitters arise from: 1) the mismatch between the

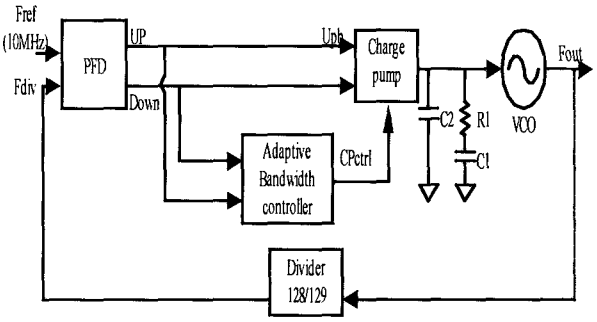
Manuscript received March 14, 2005.

Youn-Gui Song is Ph.D. course student in Pukyong National University, Busan, Korea.
(e-mail : neojack@mail1.pknu.ac.kr)
Young-Shig Choi is with Dept. of Electronics and Telecommunication Engineering, Pukyong National University, Busan. Korea. (e-mail : choivs@pknu.ac.kr)

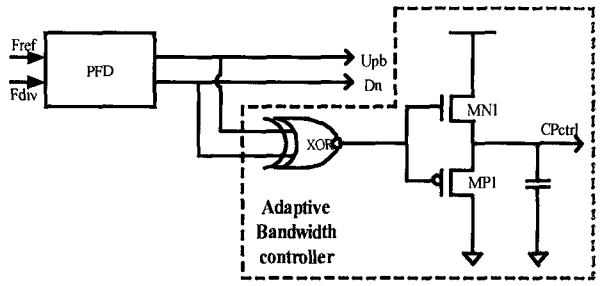
arrival times of the Up and Down pulses; 2) the mismatch between rising and falling time of switching transistors due to different gate capacitance; the mismatch between the width of the Up and Down pulses; 3) the mismatch between the charge pump current sources (both random and due to channel-length modulation); 4) the charge injection and clock feedthrough of switching transistors in the charge pump [4]. These factors cause an AC component on the tuning line of the VCO, which causes the output of the VCO to be FM modulated. It becomes the factor to raise the jitter in time domain.

III. LOW JITTER CHARGE PUMP PLL ARCHITECTURE

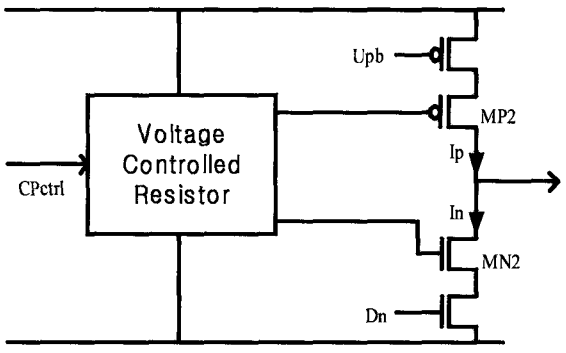
A. Proposed charge pump PLL



(a) The block diagram of the proposed PLL.



(b) The circuit of adaptive bandwidth controller.



(c) A simplified charge pump circuit.

Fig. 2 The proposed low jitter PLL based on a new adaptive bandwidth controller.

Fig. 2. (a) shows the proposed low jitter phase-locked loop based on a new adaptive bandwidth controller. It adaptively controls the loop bandwidth according to the locking status. When the phase error is large, the PLL increases the loop bandwidth and reduces locking time. When the phase error is small, the PLL decreases the loop bandwidth and minimizes output jitters. The loop bandwidth is controlled by changing the magnitude of charge pump current using the charge pump current controller shown on Fig. 2 (b). The magnitude of charge pump current on Fig. 2 (c) is proportional to CPctrl voltage.

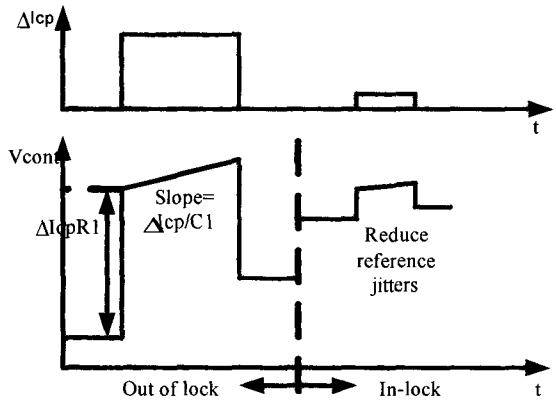


Fig. 3 Concept of reducing reference jitters

Up and Down pulses obtained from phase frequency detector (PFD) through XOR determines the status of transistors, MN1 and MP1. When the PLL is out of lock, MN1 turns on and MP1 turns off. The voltage (CPctrl) on the capacitor increases. The voltage (CPctrl) increases the current of MN3 and MN4, and subsequently, the currents (I_p and I_n) of charge pump. When the PLL is in-lock, on the other side, MP1 turns on and MN1 turns off. The voltage (CPctrl) on the capacitor decreases. And then, the currents of charge pump decreases.

When the PLL is out of lock, the loop bandwidth is wide with the large charge pump current. When the PLL is in-lock, the loop bandwidth is narrow with the small charge pump current. Therefore, the proposed PLL can achieve fast locking with low jitter characteristic because it controls the magnitude of charge pump current depending on the locking status. When the PLL is out of lock, XOR generates an output proportional to the difference between Up and Down pulses. When the PLL is in-lock, the width of Up and Down pulses is same. Then, XOR generates no signal.

The effect of those mismatches described in the previous section can be minimized by reducing the charge pump current at the lock state. Therefore, low jitter PLL can be designed while keeping fast locking. Fig. 3 shows modulating VCO input voltages that cause reference jitters. The magnitude of modulating VCO input voltage depends on the charge pump current. Small charge pump current decreases the magnitude of modulating VCO input voltage and lowers phase noise on the PLL output signal.

B. Design model of charge pump PLL

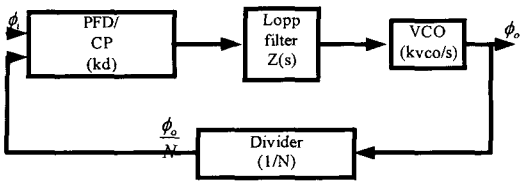


Fig. 4 Block diagram of a conventional PLL.

Fig. 4 shows a block diagram of type2 third order PLL. The PLL transfer functions are as follow,

$$G(s) = \frac{\phi_o}{\phi_i} = \frac{k_d Z(s) k_{vco}}{s} \quad (1)$$

$$H(s) = \frac{1}{N} \quad (2)$$

where, $G(s)$ is forward loop gain, $Z(s)$ is the impedance of loop filter, and $H(s)$ is reverse loop gain in PLL. $k_d = \frac{I_p}{2\pi}$ [Ampere/radian] is the combined phase frequency detector/charge pump gain, I_p is charge pump current, k_v [hertz/volt] is the VCO gain and N is divider ratio. This transfer function may be rewritten, in which use ω_n-the natural frequency of the loop, and ξ-the damping factor [5]. Therefore, open loop gain [$F(s)_{open}$], and close loop gain [$F(s)_{close}$] are as follow,

$$F(s)_{open} = H(s)G(s) = \frac{k_d Z(s) k_{vco}}{Ns} \quad (3)$$

$$F(s)_{close} = \frac{G(s)}{[1 + H(s)G(s)]} \quad (4)$$

At the type-2 third order PLL (at Fig. 1.), the impedance of loop filter would be,

$$Z(s) = \frac{1 + s\tau_2}{s(C_1 + C_2)(1 + s\tau_1)} \quad (5)$$

where τ is the time constant of loop filter as follows

$$\tau_1 = \frac{C_1 C_2}{C_1 + C_2} R_1 \quad \text{and} \quad \tau_2 = R_1 C_1 \quad (6)$$

The value of τ may be rewritten [6], for a given desired loop bandwidth (ω_p) and phase margin (ϕ_p), the loop filter design would be

$$\tau_1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \quad (7\text{-a})$$

$$\tau_2 = \frac{1}{\omega_p^2 \tau_1} \quad (7\text{-b})$$

$$\omega_p = \frac{1}{\sqrt{\tau_1 \tau_2}} \quad (7\text{-c})$$

with Eq. 7, the values of loop filter can be expressed as follow.

$$C_2 = \frac{k_d k_{vco}}{\omega_p^2 N} \frac{\tau_1}{\tau_2} \sqrt{\frac{1 + (\omega_p \tau_2)^2}{1 + (\omega_p \tau_1)^2}} \quad (8\text{-a})$$

$$C_1 = C_2 \left(\frac{\tau_2}{\tau_1} - 1\right) \quad (8\text{-b})$$

$$R_1 = \frac{\tau_2}{C_1} \quad (8\text{-c})$$

With those equations, the values of resistance and capacitances are obtained to make PLL stable both at out of lock and in-lock. The placements of the pole and zero are a trade-off between the necessary spurious tone and noise suppression, and the dynamic behavior of the loop. The pole and zero are located at 26.5KHz and 557.3KHz in the PLL, respectively. The cut-off frequencies depending on the magnitude of charge pump current are located at 229KHz (out of the lock) and 52KHz (in-lock), respectively.

IV. SIMULATION RESULTS

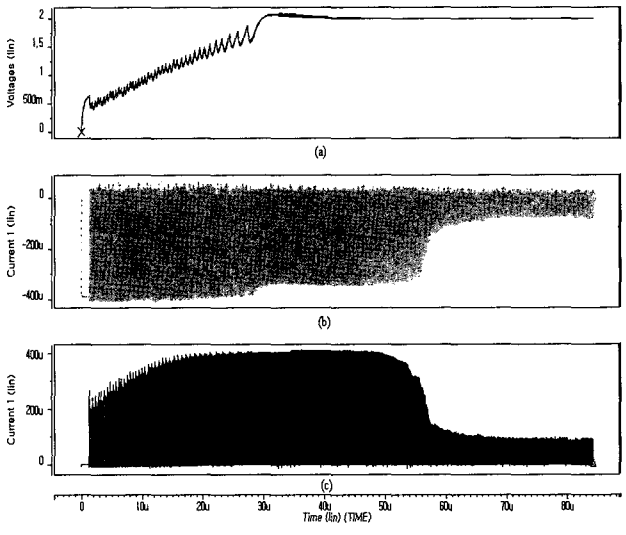


Fig. 5 (a) VCO control voltage(Vcont). The variations of I_p (b) and I_n (c) depending on the locking status.

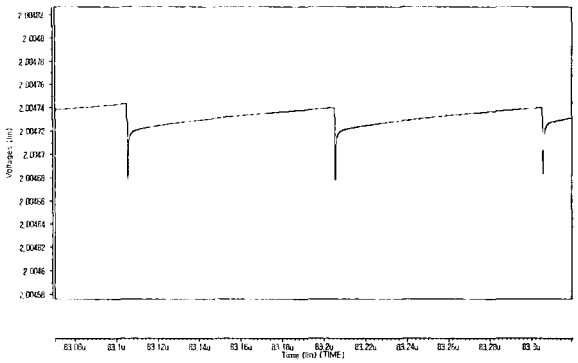
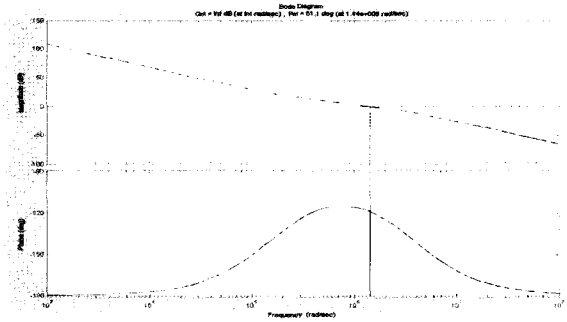
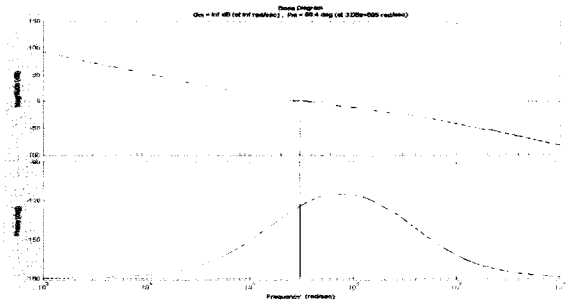


Fig. 6 The AC components of Vcont of the PLL (peak to peak voltage is approximately 60 μ volts).



(a)



(b)

Fig. 7 (a) Phase margin at out of lock (61.1deg. @ 229KH) when the current is 400 μ A.
(b) Phase margin at lock state(57.5deg. @ 52kHz) when the current is 75 μ A.

Fig. 5 shows voltage of Vcont, currents I_p and I_n of charge pump in Fig. 2. When PLL is out of lock, the currents, I_p and I_n, are maximum at 400 μ A. When PLL is in-lock, these are minimum at 75 μ A. Fig. 6 shows the fluctuations on the VCO input node when PLL is in-lock. The relative magnitude of the primary sidebands at the output of the VCO is given by [4],

$$\beta = \frac{A_m k_{vco}}{2\omega_{ref}} \tag{9}$$

where β is a value of modulation index, A_m [volt] is the peak amplitude of the first harmonic of the ripple, k_{vco} [rad/volt] is the gain of the VCO, and ω_{ref} is the synthesizer reference frequency. By using Eq. (9), -80dBc of the relative magnitude of the primary sidebands at the output of VCO can be obtained.

Fig. 7 shows the phase margin and loop bandwidth of proposed PLL as predicted by MATLAB. It has sufficient phase margin both at out of the lock and in-lock. The loop bandwidth becomes wide when the PLL is out of lock, and it becomes narrow when the PLL is in-lock. The simulation results are measured by MATLAB program using Eq. (1), (2) and (3). Fig. 7. (a) and (b) show phase margin and loop bandwidth when the magnitudes of charge pump current are 400 μ A and 75 μ A, respectively.

V. CONCLUSIONS

This paper presents an analog adaptive phase-locked loop(PLL) architecture with a new adaptive bandwidth controller to achieve fast locking and minimize jitter on PLL output. It adaptively controls the loop bandwidth according to the locking status. Therefore, the PLL can achieve fast locking with low jitter characteristic.

A 1.28-GHz CMOS phase-locked loop with a new adaptive bandwidth controller is designed with 0.35 μ m CMOS technology. It has the primary reference sidebands that are at approximately -80dBc.

REFERENCES

[1] Joonsuk Lee, and Beomsup Kim, "A low-noise fast lock phase-locked loop with adaptive bandwidth con ntrol," IEEE J, Solid-State Circuits, vol. 35, Aug. 2000, pp.1137-1145.

[2] M. Mizuno et al., "A 0.18 μ m CMOS hot-stand by phase-locked loop using a noise immune adaptive gain voltage-controlled oscillator," ISSCC Dig. Tech. Papers, Feb. 1995, pp. 268-269.

[3] G. Roh, Y. lee, and B. Kim, "An optimum phase-acq uisition technique for charge-pump phase-locked loops," IEEE Trans. Circuit Syst. II, vol. 44, Sept. 1997, pp. 729-740.

[4] Tai-Cheng Lee and Behzad Razavi, "A stabilization technique for phase-locked frequency synthesizers," IEEE J, Solid-State Circuits., vol. 38, NO. 6, June 2003, pp. 888-894.

[5] F.M GARDNER, Phaselock techniques, John Wiley &Sons, New York, 1979.

[6] Dean Banerjee, " An Analysis and Performance Evaluation of a Passive Filter Design Techniques for charge pump PLL's," Application Note 1001, National Semiconductor Corporation, July 2001

Youn-Gui Song
He received B.S. degree in Physics from Dongeui University in 2000, M.S degree in Electronic Engineering from Pukyong National University in 2002. Since 2002 to now, he has been Ph.D. course student in Electronic Engineering, Pukyong National University, Busan, Korea. The areas of interest are PLL, DLL, Fractional Frequency Synthesizer and CDRC design.

Young-Shig Choi
He received B.S. degree in Electronics Engineering from Kyungpook National University in 1982, M.S. degree from Texas A&M University in 1986 and Ph.D from Arizona State University in Electrical Engineering in 1993. From 1987 to 1989 and 1993 to 1999, he was with Hyundai Electronics as a Senior Development Engineer where he has been involved in the development of SRAM and communication chips. From 1999 to 2003, he was with Dongeui University. He joined Pukyong National University in 2003. His current interests include PLL and DLL circuit design.