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A Single Carrier Multi-Modulation Method In Multilevel Inverters

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ABSTRACT

A novel variant of full multi-modulation applications to diode-clamped and cascade multilevel inverter-termed single carrier multi-modulation is presented. The proposed PWM-technique is advantageous for its simple implementation. The correlation between multi-carrier and single-carrier multi-modulations is deduced. For the PWM methods, a mathematical model of voltage source inverter and general algorithm for the multi-modulating modulator are proposed. The theory is demonstrated by simulation results

Keywords: Multilevel inverter, Single carrier, Multi-modulation

1. Introduction

The multi-modulation derived based on the SVPWM-CPWM correlation presents a full capability in the vector redundancy and phase redundancy control in multilevel inverter[1]. Further study shows that multi-carrier multi-modulation can be equivalently implemented using only a single carrier waveform. In this continued theory, the correlation between these multi-modulations will be deduced. Carrier PWM methods can be described by a unified algorithm. For voltage source multilevel inverter, the effective zero sequence function can represent the SVPWM attributes and become a proper reference input.

For simplicity, several basic terminologies and definitions, which have been introduced in the related papers [1],[2] will not be defined again.

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2. The correlation between multi-carrier multi- modulation and single-carrier multi-modulation

From the mathematical formulation of a full multi-carrier multi-modulation (MMM) described in [1], each modulating signal is modulated within one carrier wave. The switching time diagram will be unchanged if all carrier waves and modulating signals are vertically shifted to the position of the standard carrier wave (0,1). Every new reference modulating signal will be modulated within the range of (0,1). The deduced PWM method is termed single carrier multi-modulation(SMM). To deduce the PWM equation of SMM, firstly the reference modulating signals of the MMM with p- modulating signal sets can be described as follows [1]:

$$\begin{aligned} [v_r] &= \sum_{j=1}^{3} K_j \left(\xi_{j0}[Q_{j0}] + \xi_{j1}[Q_{j1}] + ... + \xi_{j,lrj}[Q_{j,lrj}] \right) \\ K_1 &+ K_2 + K_3 = 1 \\ \xi_{j0} &+ \xi_{j1} + ... + \xi_{j,lrj} = 1 \end{aligned} \quad (1)$$

where (K_1, K_2, K_3) and (l_{r1}, l_{r2}, l_{r3}) are switching time duties and levels of redundancy defined in[1]. The reference modulating signals and multi-modulating pattern(MMP) are described in matrix forms as

$$[v_r] = \begin{bmatrix} v_{ra1}, v_{ra2}, \ldots, v_{rap} \\ v_{rb1}, v_{rb2}, \ldots, v_{rbp} \\ v_{rc1}, v_{rc2}, \ldots, v_{rcp} \end{bmatrix}$$

$$[Q_{jk}] = \begin{bmatrix} Q_{ajk1}, Q_{ajk2}, \ldots, Q_{ajkp} \\ Q_{bjk1}, Q_{bjk2}, \ldots, Q_{bjkp} \\ Q_{cjk1}, Q_{cjk2}, \ldots, Q_{cjkp} \end{bmatrix}$$

$$j = 1,2,3; \quad k = 0,1,2,.., l_{rj}; p = (n-1) \tag{2}$$

Let's rewrite the MMP $[Q_{jk}]$ in a summation form as

$$[Q_{jk}] = [Q_0] + [S_{jk}]$$

where

$$[Q_0] = \begin{bmatrix} Q_{10}, Q_{20}, .. Q_{p0} \\ Q_{10}, Q_{20}, .. Q_{p0} \\ Q_{10}, Q_{20}, .. Q_{p0} \end{bmatrix} \tag{3}$$

$$[S_{jk}] = \begin{bmatrix} S_{ajk1}, S_{ajk2}, .. S_{ajkp} \\ S_{bjk1}, S_{bjk2}, .. S_{bjkp} \\ S_{cjk1}, S_{cjk2}, .. S_{cjkp} \end{bmatrix}$$

$$j = 1,2,3; k = 0,1,2,.., l_{rj}$$

The matrix $[Q_0]$, termed as transforming matrix, characterizes the relation between the multi- and single-carrier multi-modulation methods. Its element is constant and described as:

$$Q_{t0} = P_{\min} + n - 1 - t \;\; ; \;\; t = 1,2,.., p,$$

where $P_{\min} = -(n-1)/2$ for odd level inverter. Then (3) can be rewritten as:

$$[Q_0] = \begin{bmatrix} P_{\max} - 1, P_{\max} - 2, \ldots, P_{\min} + 1, P_{\min} \\ P_{\max} - 1, P_{\max} - 2, \ldots, P_{\min} + 1, P_{\min} \\ P_{\max} - 1, P_{\max} - 2, \ldots, P_{\min} + 1, P_{\min} \end{bmatrix} \tag{4}$$

where

$$\begin{aligned} P_{\max} &= n - 1 + P_{\min} \\ Q_{10} + Q_{20} + .. + Q_{p0} &= P_{\min} \end{aligned} \tag{5}$$

The matrix $[S_{jk}]$, termed switching state pattern matrix, presents the ON/OFF states of all switching pairs for generating corresponding voltage vector. Its element $S_{xjkt}, x = a,b,c$ can obtain a value from 0 and 1. From (1a,b) and (3), the CPWM equation can be deduced and simplified as follows:

$$[v_r'] = [v_r] - [Q_0] \tag{6a}$$

$$[v_r'] = \sum_{j=1}^{3} K_j \left(\xi_{j0}[S_{j0}] + \xi_{j1}[S_{j1}] + \xi_{j2}[S_{j2}] + ... + \xi_{j,lrj}[S_{j,lrj}] \right) \tag{6b}$$

where $0 \le v_{rat}' \le 1$, $0 \le v_{rbt}' \le 1$ and $0 \le v_{rct}' \le 1$, $t = 1,2,..., p$.

Example 1: From the example of five-level inverter[1], the matrix $[Q_0]$ is determined as

$$[Q_0] = \begin{bmatrix} Q_{10}, Q_{20}, Q_{30}, Q_{40} \\ Q_{10}, Q_{20}, Q_{30}, Q_{40} \\ Q_{10}, Q_{20}, Q_{30}, Q_{40} \end{bmatrix} = \begin{bmatrix} 1, 0, -1, -2 \\ 1, 0, -1, -2 \\ 1, 0, -1, -2 \end{bmatrix}$$

For diode-clamped inverters, the *PMMP* elements can be mathematically expressed using PMMP sets in Table 1a, as follows:

$$S_{xjkt} = \begin{cases} 1 & if \quad P_{xjk} \ge \left(\frac{n+1}{2} - t\right) \\ 0 & if \quad else \end{cases} \tag{7}$$

$$j = 1,2,3; x = a,b,c; t = 1,2,.., p; k = 0,1,2,.., l_{rj}$$

For cascade inverters, each new PMMP set can be derived from (7) by moving $t-$ elements between *PMMP* sets. For example, we consider set 1 and set 2, where the 1st element of set 1 is equal to 4th element of set 2, 2nd element of set 1 is equal to 3rd element of set 2, etc. As a result, there are totally (n-1)! (factorial) PMMP sets

in Table 1b. Since any PMMP is described from a sequence of 0 and 1, then generating *PMMP* sets using digital circuits will be quite simple in comparison to the full MMM.

Table 1 *PMMP* sets of five-level inverter –Single carrier multi-modulation

a) For diode clamped inverter					
PMP	-2	-1	0	1	2
PMMP set	0,0,0,0	0,0,0,1	0,0,1,1	0,1,1,1	1,1,1,1
b) For cascade inverter					
PMMP	0,0,0,0	1,0,0,0 0,1,0,0 0,0,1,0 0,0,0,1	0,1,0,1 1,0,1,0 1,0,0,1 1,1,0,0 0,1,1,0 0,0,1,1	1,0,1,1 1,1,0,1 1,1,1,0 0,1,1,1	1,1,1,1
Set 1	0,0,0,0	0,0,0,1	0,0,1,1	0,1,1,1	1,1,1,1
Set 2	0,0,0,0	1,0,0,0	1,1,0,0	1,1,1,0	1,1,1,1
Set 3	0,0,0,0	1,0,0,0	1,0,1,0	1,1,1,0	1,1,1,1

Characteristics of the SMM

Notice (2),(4) and (5), the relation between MP component[1] and corresponding MMP p-component set in SMM can be expressed as

$$P_{xjk}=\sum_{t=1}^{p}Q_{xjkt}=\sum_{t=1}^{p}(Q_{t0}+S_{xjkt})=P_{\min}+\sum_{t=1}^{p}S_{xjkt} \qquad (8)$$
$$x=a,b,c$$

The MP common mode, related to switching matrix can be determined as

$$P_{jkCM}=\sum_{x=a,b,c}P_{xjk}=\sum_{x=a,b,c}\sum_{t=1}^{p}(Q_{t0}+S_{xjkt})= \qquad (9)$$
$$=\sum_{x=a,b,c}(P_{\min}+\sum_{t=1}^{p}S_{xjkt})=3P_{\min}+\sum_{x=a,b,c}\sum_{t=1}^{p}S_{xjkt}$$

In the MMM, the effective modulating signals v_{rxe}, proportional to phase to dc-neutral point voltage, can be expressed using modulating references v_{rxt} as

$$v_{rxe}=(v_{rx1}+v_{rx2}+..+v_{rxp})=\sum_{t=1}^{p}v_{rxt} \qquad (10)$$

For the SMM, it can be deduced from references v'_{rxt} as

$$v_{rxe}=\sum_{t=1}^{p}(Q_{t0}+v'_{rxt})=P_{\min}+\sum_{t=1}^{p}v'_{rxt}.$$

Verifying the generalized multi-modulation formulation

The matrix MMP $[S_{jk}]$ describes the ON/OFF states of switching pairs. The corresponding MP presents the address for switching state data. If some states in (6) disappear, their corresponding time duties will be zero ($K_j\xi_{jk}=0$), $k=0,1,2,..,l_{rj}$. The reference modulating signal v'_{rxt} of switching pair SW_{xt} can be determined as a time integration of switching states as:

$$v'_{rxt}=\sum_{j=1}^{3}\sum_{k=0}^{lrj}\frac{T_{jk}}{T_S}S_{xjkt} \qquad (11)$$
$$T_{jk}=K_j\xi_{jk}T_S$$

where during the jk-switching state, parameters S_{xjkt} and T_{jk} present the ON/OFF state of switching pair SW_{xt} and corresponding time duration, respectively. The logic function S_{xjkt} varies depending on the PMP values (P_{xjk}) and selected PMMP set. For diode-clamped inverter, S_{xjkt} can be determined by (7). For cascade inverter, S_{xjkt} can be derived by moving conditions (7) between elements. From PMMP sets and by noticing the increase of phase MP values in switching sequence, the state of switching pair will change from 0 to 1 in sampling period T_S. Equation (11) can be rewritten in relation to the on-time duration T_{ON} of switching pair SW_{xt} as:

$$v'_{rxt}=\frac{T_{ON}}{T_S} \qquad (12)$$

Each modulating signal v'_{rxt} is proportional to the on-time duration T_{ON} of the corresponding switching pair.

The rightness of (12) has verified the accuracy of the generalized carrier PWM approach using multi-modulating patterns.

3. Voltage model of voltage source inverter, multi-modulation modulator

a) Voltage model of voltage source inverter

From the previous investigation, the voltage source inverter can be considered as a complex source, consisting of active voltages in series with zero sequence component –Fig.1b. The active voltage components can be determined from vector location in the hexagonal diagram and zero sequence component from the values of redundant coefficients.

Active and fundamental voltages influence on the PWM performance by representing the parameters K_1, K_2 ,and K_3 in the effective zero sequence function .

Effective zero sequence function: For unipolar PWM, the zero sequence function is given as a function of redundant factors η_1, η_2, η_3 as:

$$v_{r0} = v_{r0\min} + \eta_1 K_1 + \eta_2 K_2 + \eta_3 K_3 \qquad (13)$$

In the MMM, the effective zero sequence function v_{r0e} , which is related to zero sequence voltage of $v_0 = v_{r0e} V_{dc} /(n-1)$, can be derived as follows:

$$v_{r0e} = v_{r0\min} + \sum_{j=1}^{3} K_j \left(\xi_{j1} + 2\xi_{j2} + ... + l_{rj}\xi_{j,lrj}\right) \qquad (14)$$

The maximum and minimum zero sequence voltage in discontinuous PWM can be determined by corresponding setting of $\xi_{j,lrj} = 1$ and $\xi_{j0} = 1$, $j = 1,2,3$, respectively as follows:

$$v_{0\max} = V_{dc}/2 - V_{dc} Max/(n-1) \qquad (15)$$

$$v_{0\min} = -V_{dc}/2 - V_{dc} Min/(n-1) \qquad (16)$$

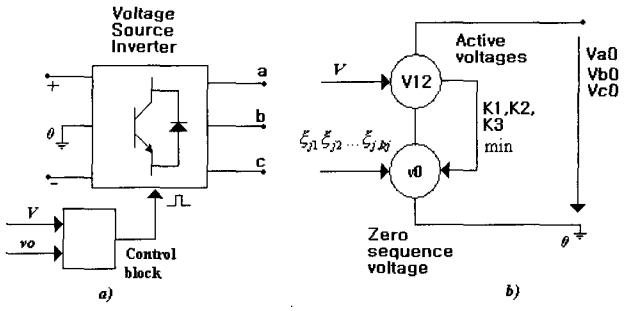

Fig. 1 Voltage source inverter and its equivalent voltage model with fundamental voltages and vector redundancy (zero sequence) controllable

where Max and Min are the largest and the smallest values from three fundamental modulating signals.

b) Multi-modulation methods

Every unipolar/multi-modulation can be represented by redundant parameters of corresponding(effective) zero sequence function. Redundant coefficients can be determined either by direct setting ξ_{jk} (redundancy controlled multi-modulation) or indirectly from required zero sequence voltage(zero sequence controlled multi-modulation).

Direct method is advantageous if functions of redundant parameters are known. The DPWM and SVPWM with extreme zero sequence functions are among its simple cases.

Indirect method can be implemented for obtaining zero sequence voltage closest to some optimum function. The methods related to common mode have been introduced in [2]. As a result, for given reference zero sequence voltage, redundant parameters and corresponding MP can be derived. Using the $\vec{P}_{jk} \leftrightarrow [S_{jk}]$ transformation and substituting them in the PWM equation, reference modulating signal set can be generated. Let $v_{r0e,ref}$ be reference effective zero sequence, the SVPWM multi-modulation with its effective zero sequence approximate to $v_{r0e,ref}$ can be derived as follows:

1) $n_0 = Int(v_{r0e,ref} - v_{r0\min})$ (17)

$$v_{r1} = v_{r0e,ref} - v_{r0\min} - n_0 \tag{18}$$

2) Determination of MPs [2]

$$\vec{P}_{jk} = \vec{P}_{j0} + k\vec{l};\ j = 1,2,3 \quad k = n_0, (n_0 + 1) \tag{19}$$

3) Transformation $\vec{P}_{jk} \rightarrow [S_{jk}]$ using Table 1.

4) Determination of reference modulating signals by (20) as:

$$[v_r^{'}] = \begin{cases} 0.5K_1([S_{1,n0}] + [S_{1,(n0+1)}]) + K_2[S_{2,n0}] + K_3[S_{3,n0}] & if \quad 0 \le v_{r1} \le K_1 \\ K_1[S_{1,(n0+1)}] + 0.5K_2([S_{2,n0}] + [S_{2,(n0+1)}]) + K_3[S_{3,n0}] & if \quad K_1 < v_{r1} \le K_1 + K_2 \\ K_1[S_{1,(n0+1)}] + K_2[S_{2,(n0+1)}] + 0.5K_3([S_{3,n0}] + [S_{3,(n0+1)}]) & if \quad K_1 + K_2 < v_{r1} < 1 \end{cases} \tag{20}$$

The main operator is summation, whose augmenter will be selected if related switching state S_{xjkt} is 1.

c) Multi-modulation modulator can be described as shown in Fig.2:

The parameters K_1, K_2, K_3 are calculated in the fundamental control block. The redundant coefficients ξ_{jk} and corresponding MP $\vec{P}_{jk}$ are performed in the redundancy control block, depending on the required zero sequence and PWM conditions. The selection of PMMP sets $[S_{jk}]$ and the following transformation $\vec{P}_{jk} \rightarrow [S_{jk}]$ are implemented in the phase redundancy control block, using look-up Table or deduced algorithm. Finally, reference modulating signals are generated at the output.

For unipolar PWM and MMM, whose reference modulating signals are generated based on the CPWM-SVPWM correlation, the SVPWM mode for obtaining a low ripple current and the DPWM mode for reducing the number of switches can be obtained by proper setting of redundant parameters[2]. The capability of easy achieving these two modes while to reduce common mode to the required value, which is not available in the other PWM methods, introduces their advantage. In the diode clamped inverter, this could be utilized, if the deduced zero sequence is set as active signal for reducing dc neutral point variation or properly distributing the switching loss among switching devices, particularly in a low modulation index..

For cascade inverters, multi-modulations can become more preferable than unipolar PWM since balancing of switching loss among switching pairs can always be achieved independently from modulation index and reference waveforms. This can be done by subsequently alternating PMMP sets in the related carrier PWM equation for several fundamental periods. Since the corresponding MMP sets in the sequences of 0 and 1 can

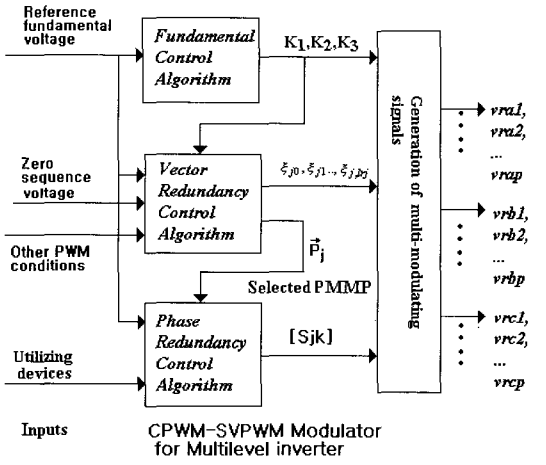

Fig. 2 The general block diagram of CPWM-SVPWM modulator for multilevel inverter

be implemented by digital EPLD circuits and simple summation and comparison operators are required in PWM modulator, the SMM presents a perspective solution of multi-modulation. For diode clamped multilevel inverters, from numerous switching states corresponding to pivot vectors, more possible redundant variants can be selected for dc neutral point balancing. Hence, the SMM method attains the desired states in corresponding time duties, or in this case, SMM presents a direct access to time duty of individual redundant states. The problem of balancing dc-neutral point in SMM for certain current circumstances by proper states and time duty will be investigated in further detail.

4. Examples

Example 2: It is required (by a direct method) to determine reference modulating signals of SMM, which implement SVPWM with the lowest effective zero sequence for five-level inverter.

The required SVPWM can be implemented by sequence of four switching states, corresponding to $\vec{U}_{10},\vec{U}_{20},\vec{U}_{30}$ and $\vec{U}_{11}$ ($(\xi_{10}=\xi_{11}=0.5)$ and $(\xi_{20}=\xi_{30}=1)$). The corresponding equation of reference signals is described as follows:

$$\lfloor v_r^{'} \rfloor = 0.5K_1([S_{10}]+[S_{11}])+K_2[S_{20}]+K_3[S_{30}]. \qquad (21)$$

The diagrams of modulating signal sets are drawn in Fig.3.

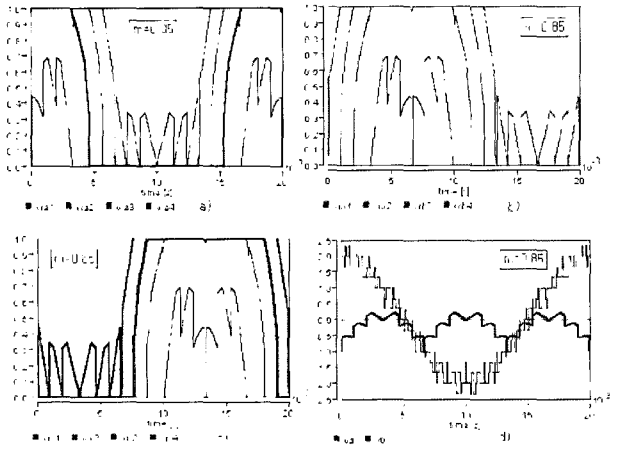

Fig. 3 Five-level inverter: The SVPWM in SMM with the lowest zero sequence: a),b),c) the modulating signal sets of A-,B- and C- phases and d)the A-phase voltage and effective zero sequence.

Example 3: The described multi-modulation theory for obtaining a large number of switching states can be illustrated for three-level inverter. In full MMM, the parameter p is equal 2. A single carrier multi-modulation is required with the assumptions as follows:

a) to obtain the medium zero sequence voltage, then

$$v_{r0,mid}=\frac{v_{r0\max}+v_{r0\min}}{2}=v_{r0\min}+\frac{l_{r1}}{2}K_1+\frac{l_{r2}}{2}K_2+\frac{l_{r3}}{2}K_3$$

b) to have all middle redundant vectors active and equally-centered at the dashed circles as shown in Fig.4a. There are 5/4/5 switching states for corresponding areas 1/2 (or 4)/ 3, respectively.

Solution

The redundant parameters are derived as follows:

Area 1: For $l_{r1}=2$ and $l_{r2}=l_{r3}=1$:

$v_{r0,mid}=v_{r0\min}+K_1+0.5K_2+0.5K_3$

$\Rightarrow \xi_{10}=0$, $\xi_{11}=1$, $\xi_{20}=\xi_{21}=0.5$ and $\xi_{30}=\xi_{31}=0.5$

$\lfloor v_r^{'} \rfloor = K_1[S_{11}]+0.5K_2([S_{20}]+[S_{21}])+0.5K_3([S_{30}]+[S_{31}])$

Similarly, redundant parameters and MP can be determined for other areas as described below.

Areas 2, 4: For $l_{r1}=1$ and $l_{r2}=l_{r3}=0$:

$\lfloor v_r^{'} \rfloor = 0.5K_1([S_{10}]+[S_{11}])+K_2[S_{20}]+K_3[S_{30}]$

Area 3: For $l_{r3}=0$, $l_{r1}=l_{r2}=1$ and

$\lfloor v_r^{'} \rfloor = K_1([S_{10}]+[S_{11}])+0.5K_2([S_{20}]+[S_{21}])+K_3[S_{30}]$

Determination of the MP:

For instance, in area 1 (x=a,b,c):

$P_{x11}=P_{x10}+1; P_{x21}=P_{x20}+1; P_{x31}=P_{x30}+1$

Determination of the MMP: The relation between MP and corresponding MMP can be derived from the Table 2.

Table 2 Single multi-modulation: Phase multi-modulating pattern($PMMP$) for a three-level inverter

PMP	-1	0	1
($PMMP$)- set 1	(0,0)	(0,1)	(1,1)
($PMMP$) - set 2 (cascade type only)	(0,0)	(1,0)	(1,1)

If set 1 is selected then

$$S_{x1}=\begin{cases}1 & if \quad P_x=1\\ 0 & else\end{cases}$$

$$S_{x2}=\begin{cases}1 & if \quad P_x\geq 0\\ 0 & else\end{cases}$$

If set 2 is selected (cascade type only) then

$$S_{x1} = \begin{cases} 1 & if \quad P_x \geq 0 \\ 0 & else \end{cases}$$

$$S_{x2} = \begin{cases} 1 & if \quad P_x = 1 \\ 0 & else \end{cases}$$

In simulation, using two PMMP sets from Table 2, the diagrams of the A-,B- and C-phase modulating signal sets $v_{ra1}, v_{ra2}, v_{rb1}, v_{rb2}$ and v_{rc1}, v_{rc2}, and effective zero sequence are drawn in Fig.4b for set 1 and Fig.4c for set 2.

Example 4: This example demonstrates the zero sequence controlled SVPWM method with minimum common mode using previously described algorithm (17),(18),(19) and (20). In Fig.5, the diagrams are drawn for m=0.75 ($v_{r0ref} = 0$).

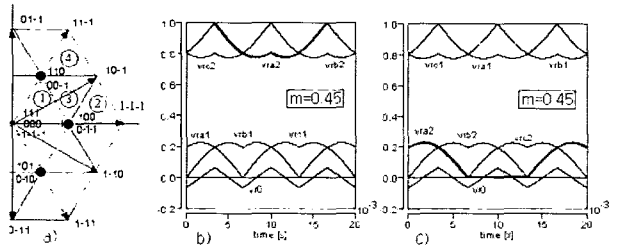

Fig. 4 Three-level inverter: a) the MP diagram, b),c) the diagrams of three phase modulating signals and effective zero sequence for b) PMMP set 1 and c) PMMP set 2

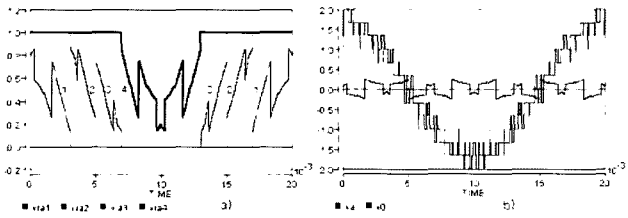

Fig. 5 Five-level inverter: Minimum CM SVPWM, m=0.75 a) the diagrams of v_{ra1} (1), v_{ra2} (2), v_{ra3} (3) and v_{ra4} (4) and b) A-phase voltage and effective zero sequence

5. Conclusions

In the paper, the single-multi-modulation has been presented. The algorithm for generating the reference signals in the SMM has been drastically simplified in comparing to multi-carrier approach. For generating numerous reference signals, summing and comparing operators can be properly designed with digital technique. The proposed voltage model of inverter with redundant control of effective zero sequence is useful for circuit analysis in the other applications such as in four-leg multilevel inverter. By modifying MMP, the algorithm is also applicable for partial multi-modulation.

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