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A High Efficiency ZVS PWM Asymmetrical Half Bridge Converter for Plasma Display Panel Sustaining Power Modules

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ABSTRACT

A high efficiency ZVS PWM asymmetrical half bridge converter for a plasma display panel (PDP) sustaining power modules is proposed in this paper. To achieve the ZVS of power switches for the wide load range, a small additional inductor L_{lkg}, which also acts as an output filter inductor, is serially inserted into the transformer's primary side. At that point, to solve the problem of ringing in the secondary rectifier caused by L_{lkg}, the proposed circuit employs a structure without the output filter inductor, which helps the voltages across rectifier diodes to be clamped at the output voltage. Therefore, no dissipative RC (resistor capacitor) snubber for rectifier diodes is needed and a high efficiency as well as low noise output voltage can be realized. In addition, since it has no large output inductor filter, the asymmetrical half bridge converter features a simpler structure, lower cost, less mass, and lighter weight. In addition, since all energy stored in L_{lkg} is transferred to the output side, the circulating energy problem can be effectively solved. The operational principle, theoretical analysis, and design considerations are presented. To confirm the operation, validity, and features of the proposed circuit, experimental results from a 425W, 385Vdc/170Vdc prototype are presented.

Keywords: switch mode power supply, zero voltage switching, and plasma display panel.

1. Introduction

A plasma display panel(PDP) is now expected as the leading candidate for large area wall-hanging color TVs, since it has advantages over conventional display devices by its large 40 plus-inch screen, wide view angle, lightness, thin width, long life time, and high contrast [1-3].

The operation of the PDP is divided into three periods of resetting, addressing, and sustaining periods. During the resetting period, all PDP cells are erased in preparation to carry out addressing. Selective, write-discharges form required image and are ignited by applying the data and scanning pulses to the addressing and scanning electrodes, respectively. Since the addressing discharge itself emits an insufficient visible light, high voltage AC square pulses are continuously applied between sustaining and scanning electrodes for the strong light emission of selective cells during the sustaining period. Therefore, to carry out these operations successfully, the PDP must be equipped with the various kinds of power modules for sustaining, erasing, addressing, and scanning operations, etc[1-3].

Since most of the power required to drive the PDP is consumed during the sustaining period, sustaining operations among the above-mentioned power modules are mainly responsible for the overall system efficiency

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and size. In addition, since the recent wall hanging PDP color TV tends to require the smaller size, lighter weight, and fan-less system for the lower levels of acoustic noise and vibration, the high power density, high performance, and high efficiency become a hot issue of the PDP power module[1-3].

Among various ZVS-PWM DC/DC converters hitherto developed, a half bridge converter suitable for the mid power level (about 400W~500W) application like the PDP power module has been proposed to reduce the component current/voltage stress and switching losses as shown in Fig. 1 (a). However, since this converter is required to have the large leakage inductor to achieve the ZVS of power switches for the wide load range, it has several serious problems such as a large circulating energy, low system efficiency, serious parasitic ringing in the secondary rectifier, considerable heating, bulky cooling system, and noisy output voltage. Specifically, in the case of the high output voltage applications like the PDP sustaining power module, the resistor-capacitor (RC) snubber absorbs the serious ringing voltage across the secondary rectifier which degrades the overall system efficiency, because the energy stored in the snubber capacitor is not only very large but also dissipated through the snubber resistor. Moreover, since the leakage inductor is the parasitic component, which cannot be tuned arbitrarily, the additional large inductor, enough to achieve the ZVS of power switches, would be required [4-7]. Therefore, a new high efficiency ZVS-PWM asymmetrical half bridge converter well suited to the PDP Sustaining Power Module (PSPM) is proposed in this paper as shown in Fig. 1 (b). It can effectively overcome the above-mentioned problems of the prior circuit and realize high power density, higher performance, and higher efficiency.

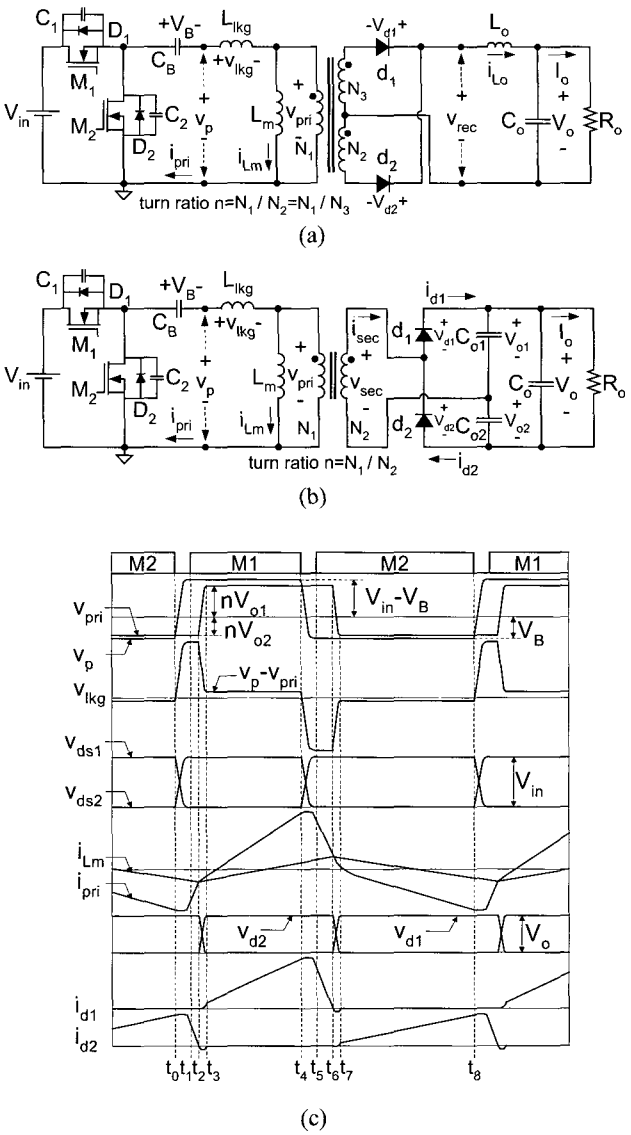

Fig. 1 Proposed converter (a) Conventional ZVS PWM half bridge converter (b) Schematic diagram of the proposed circuit (c) Key waveforms

2. Features of the proposed converter

To achieve the ZVS of power switches for the wide load range, an additional inductor is inserted into the transformer primary side as seen in the prior approach of Fig. 1 (b), where C_1, C_2, D_1 and D_2 are not additional components but parasitic capacitors. Anti-parallel diodes of MOSFETs and L_{lkg} represent the additional inductor including the transformer leakage component.

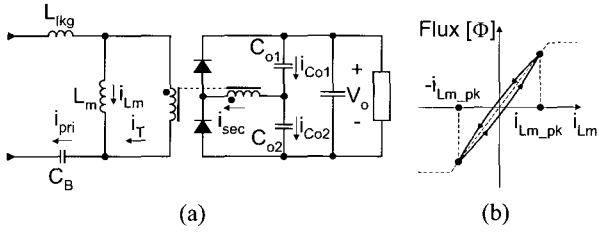

Fig. 2 Zero DC offsets of the transformer magnetizing current and flux (a) transformer magnetizing current (b) B-H curve of the magnetic core

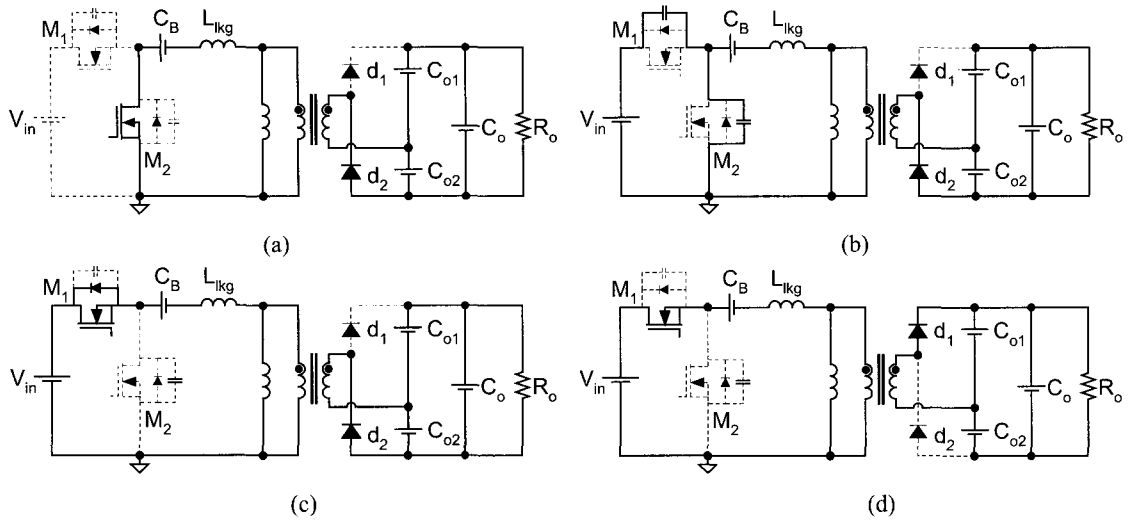

Fig. 3 Operational modes of the proposed converter, (a) Before t_0 (b) Mode 1 (t_0~t_1) (c) Mode 2 (t_1~t_2) (d) Mode 3 (t_2~t_3)

However, the same abovementioned problems as the prior circuit caused by the additional inductor are inevitable. To solve the problem related to the ringing in the secondary rectifier, the voltages across output rectifier diodes have to be clamped at any voltage source, which can be effectively accomplished by removing the output filter inductor. Therefore, a RC snubber to absorb the ringing voltage is not necessary and the high efficiency as well as low noise output voltage can be realized. In addition, since it has no large output filter inductor but also employs only a small additional leakage inductor in the primary side, it features a simpler structure, lower cost, less mass, and lighter weight. Although the output filter inductor does not exist, L_{lkg} can function as a filter inductor as well as for ZVS operation, which counts for nothing in high-voltage and low-current applications such as a PDP sustaining power module. Moreover, since all energy stored in L_{lkg} is transferred to the output side until the current flowing through L_{lkg} becomes 0A, the circulating energy problem can be effectively solved.

Fig. 2 shows that the proposed converter features the zero DC offsets of the transformer magnetizing current and magnetic flux. From the fact that the DC value of the current through the capacitor is 0A in steady state, the DC values of i_{pri}, i_{Co1}, and i_{Co2} (i. e. $<i_{pri}>$, $<i_{Co1}>$, and $<i_{Co2}>$, respectively) are all 0A, where $<\bullet>$ means the DC value of '•'. As can be seen in Fig. 2 (a), since i_{sec} is equal to i_{Co1}-i_{Co2}, $<i_{sec}>=<i_{Co1}>-<i_{Co2}>=0$A. Since i_T is equal to i_{sec}/n, $<i_T>=<i_{sec}/n>=0$A. And, since i_{Lm} is equal to i_{pri}-i_T, $<i_{Lm}>=<i_{pri}>-<i_T>=0$A, which means that the DC offsets of the transformer magnetizing current and magnetic flux can be completely blocked. Therefore, the transformer magnetic core can be fully utilized as shown in Fig. 2 (b), and thus, its power density can be considerably increased and the heat generation of the transformer greatly reduced.

3. Circuit operation

Figs. 1 (b) and (c) shows the proposed circuit and its key waveforms, respectively. One cycle period of a proposed circuit is divided into two half cycles, t_0~t_4 and t_4~t_8. Since the operation principles of two half cycles are symmetric, only the first half cycle is explained. The driving method of the proposed circuit is the same as those of the conventional circuit. The switches M_1 and M_2 are turned on and off in a complementary method offset against each other. M_1 is driven with the duty ratio D, which is less than 0.5. To illustrate the steady-state operation, all parasitic components except for those specified in Fig. 1(b) are assumed to be neglected. The switch M_2 is assumed to be initially in turn-on states before t_0. Therefore, the energy stored in C_B is powered to the output stage as shown in Fig. 3 (a) and at the same time, the primary current is linearly decreased with the slope of $-(V_B-nV_{o2})/L_{lkg}$. The analysis of the proposed circuit begins when the switch M_2 is turned off.

Mode 1 (t_0~t_1): When M_2 is turned off at t_0, mode 1 begins as shown in Fig. 3 (b). With the initial conditions of $i_{pri}(t_0)=I_{t0}$, $v_{ds1}(t_0)=V_{in}$, and $v_{ds2}(t_0)=0$, the current i_{pri} flowing through L_{lkg} charges C_2 and discharges C_1 as $v_{ds1}(t)=V_{in}-I_{to}/(2C_{oss})(t-t_0)$ and $v_{ds2}(t)=I_{to}/(2C_{oss})(t-t_0)$ where C_1 and C_2 are equal to C_{oss} and L_{lkg} acts as a current source with the value of I_{t0} during this interval. After the voltage across C_1 is decreased to 0V, D_1 starts conducting. Therefore, the voltage across M_1 is maintained to 0V.

Mode 2 (t_1~t_2): Since D_1 is conducting before t_1, M_1 can be turned on with the ZVS at t_1. Since the primary current i_{pri} is larger than the magnetizing current i_{Lm}, the secondary current i_{sec} is still flowing in the same direction as that of the previous mode and output rectifier diode d_2 is also on the conductive state as shown in Fig. 3 (c). At the same time, the primary current is linearly increased with the slope of $(V_{in}-V_B+nV_{o2})/L_{lkg}$.

Mode 3 (t_2~t_3): When the primary current i_{pri} becomes equal to the magnetizing current i_{Lm}, mode 3 begins as shown in Fig. 3 (d). Since the primary current i_{pri} becomes smaller than the magnetizing current i_{Lm}, the direction of the secondary current i_{sec} is reversed and the commutation between d_1 and d_2 begins.

Mode 4 (t_3~t_4): After the commutation of output rectifier diodes, d_1 is conducting and d_2 blocked. Therefore, the input source energy is powered to the output stage and at the same time, the primary current is linearly increased with the slope of $(V_{in}-V_B-nV_{o1})/L_{lkg}$.

The circuit operation of t_4~t_8 is similar to that of t_0~t_4. Subsequently, the operation from t_0 to t_8 is repeated.

4. Analysis of the proposed converter

4.1 Voltage conversion ratios

For the convenience of the analysis of the steady-state operation, several assumptions are made as follows:

- All parasitic components except for the leakage inductor are neglected
- The dead time between M_1 and M_2 is discarded.
- The conductive period DT_s of M_1 is less than $0.5T_s$.
- The commutation time between two pairs of output diodes is discarded.
- The blocking capacitors C_B, C_{o1}, C_{o2} and output capacitor C_o are large enough to be considered as a constant voltage source V_B, V_{o1}, V_{o2}, and V_o, respectively.
- Since time intervals t_1~t_2 and t_5~t_6 (as shown in Fig. 1 (c)) are much smaller than the switching period T_s, they can be discarded for the simplicity of the analysis.
- The magnetizing inductor L_m is so large that $i_{Lm}=0$.

By imposing the volt-second balance rule on the leakage inductor L_{lkg}, the steady state equation can be obtained as:

$$D(V_{in}-nV_{o1}-V_B)=(1-D)(V_B-nV_{o2}) \tag{1}$$

From equation (1), the voltage V_B across C_B can be expressed as:

$$V_B=DV_{in} \tag{2}$$

By imposing the volt-second balance rule on the magnetizing inductor L_m, the steady state equation can be obtained as:

$$D(V_o-V_{o2})=(1-D)V_{o2} \tag{3}$$

From equation (3), the voltage V_{o2} across C_{o2} can be expressed as:

$$V_{o2}=DV_o \tag{4}$$

Since V_{o1} is equal to V_o-V_{o2}, the voltage V_{o1} across C_{o1} can be easily obtained as:

$$V_{o1}=V_o-V_{o2}=(1-D)V_o \tag{5}$$

Fig. 4 shows that simplified current waveforms and the half of the average value of the sum of i_{d1} and i_{d2} is equal to the load current I_o. Therefore, the following steady state equation is satisfied:

$$I_o=\frac{V_o}{R_o}=\frac{1}{2}avg\langle i_{d1}+i_{d2}\rangle =\frac{n}{2T_s}\left[\frac{V_{in}-nV_{o1}-V_B}{2L_{lkg}}D^2T_s^2+\frac{V_B-nV_{o2}}{2L_{lkg}}(1-D)^2T_s^2\right] \tag{6}$$

where avg<•> means the average value of '•'. From equations (2), (4), (5), and (6), the steady state voltage

conversion ratio of the overall system can be derived as follow:

$$M=\frac{V_o}{V_{in}}=\frac{1}{\frac{4L_{lkg}}{nR_oT_sD(1-D)}+n} \quad (7)$$

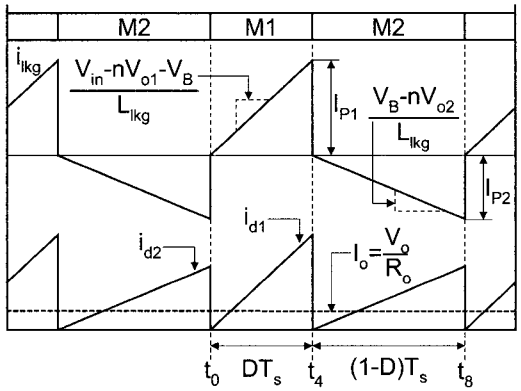

Fig. 4 Simplified current waveforms

4.2 Zero-voltage switching

From Fig. 1 (c), to achieve the ZVS of switches, the energy E_{lkg_t4} stored in the leakage inductor L_{lkg} at t_4 must be large enough to fully charge C_1 and discharge C_2 before the switch M_2 is turned on. Similarly, the energy E_{lkg_t8} stored in the leakage inductor at t_8 must fully charge C_2 and discharge C_1 before the switch M_1 is turned on. Therefore, to assure the ZVS of switches M_1 and M_2, the following equation must be satisfied.

$$E_{lkg\_t_4}=\frac{1}{2}L_{lkg}I_{lkg\_t_4}^2 \geq E_{lkg\_t_8}=\frac{1}{2}L_{lkg}I_{lkg\_t_8}^2 \geq \frac{1}{2}2C_{oss}V_{in}^2 \quad (8)$$

where C_1 and C_2 are assumed to be equal to C_{oss} and I_{lkg_t4} and I_{lkg_t8} are the peak currents through the leakage inductor at t_4 and t_8, respectively. From the simplified current waveforms shown in Fig. 4, I_{lkg_t4} and I_{lkg_t8} are assumed to be equal to I_{p1} and I_{p2}, respectively, which can be also expressed as follows:

$$I_{lkg\_t_4} \cong I_{P1}=\frac{V_{in}-nV_{o1}-V_B}{L_{lkg}}DT_s \quad (9)$$

$$I_{lkg\_t_8} \cong I_{P2}=\frac{V_{in}-nV_{o2}}{L_{lkg}}(1-D)T_s \quad (10)$$

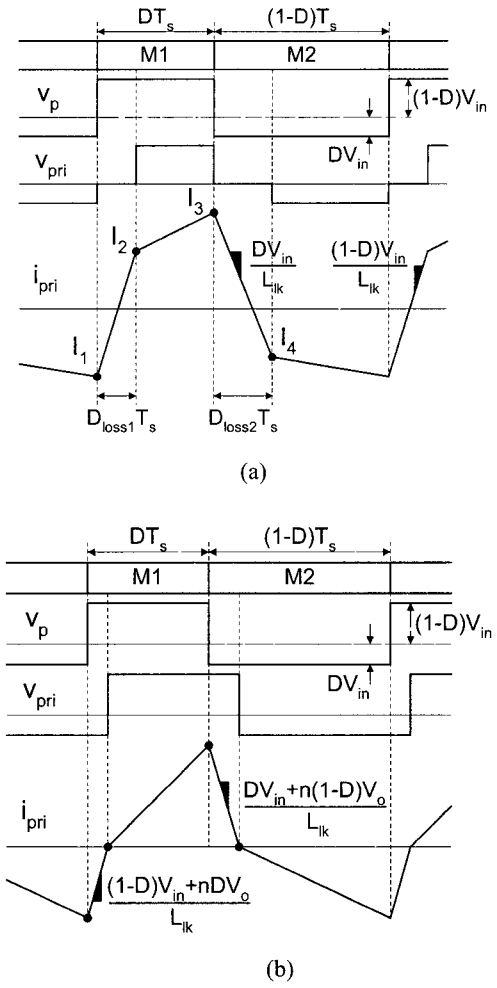

Fig. 5 Comparison of primary voltage and current waveforms
(a) Conventional half bridge converter
(b) Proposed converter

4.3 Duty cycle loss and circulating current

The typical waveforms of the conventional half bridge converter and the proposed converter are compared as shown in Fig. 6. The operating duty cycle of the conventional circuit can be expressed as $D=D_{eff1}+D_{loss1}$ and $1\text{-}D=D_{eff2}+D_{loss2}$, where D_{eff1} and D_{eff2} mean the effective duty cycle and D_{loss1} and D_{loss2} mean the losses of the duty cycle. The D_{loss1} and D_{loss2} can be expressed as where I_1, I_2, I_3, and I_4 are defined in Fig. 6 (a).

$$D_{loss1}=\frac{L_{lk}(I_1+I_2)}{(1-D)T_sV_{in}},\ D_{loss2}=\frac{L_{lk}(I_3+I_4)}{DT_sV_{in}} \quad (11)$$

Table 1 Comparisons of device stress

Part	Conventional circuit	Proposed circuit
Voltage stress of M_1 and M_2	V_{in}	V_{in}
Current stress of M_1 and M_2	$2(1\text{-}D)I_o/n_{con}$, $2DI_o/n_{con}$	$n_{pro}I_o/D$, $n_{pro}I_o/(1\text{-}D)$
Voltage stress of d_1 and d_2	$2DV_{in}/n_{con}+\alpha$, $2(1\text{-}D)V_{in}/n_{con}+\alpha$ (α=voltage ringing)	V_o
Current stress of d_1 and d_2	I_o	$2I_o/D$, $2I_o/(1\text{-}D)$
DC offset current of L_m	$(1\text{-}2D)I_o/n_{con}$	0
Transformer turn ratio	n_{con}	$n_{pro}=2n_{con}$

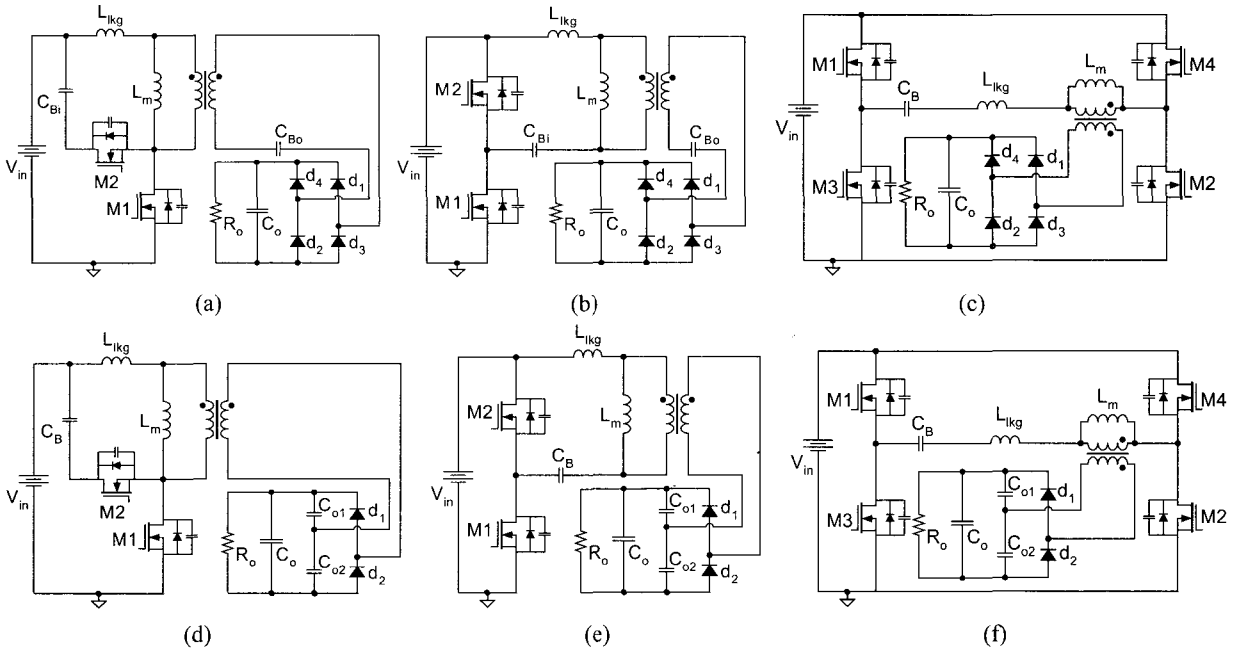

Fig. 6 A family of ZVS PWM bridge type DC/DC converter, (a) Active clamp forward converter with full bridge rectifier (b) Asymmetrical half bridge converter with full bridge rectifier (c) Phase shifted full bridge converter with full bridge rectifier (d) Active clamp forward converter with voltage-doubler rectifier (e) Asymmetrical half bridge converter with voltage-doubler rectifier (f) Phase shifted full bridge converter with voltage doubler rectifier

For the conventional ZVS PWM half bridge converter, the leakage inductance should be large enough to provide a reasonable ZVS range. This means that the loss of the duty cycle D_{loss1} and D_{loss2} are very large from the equation (11) and hence, the effective powering period is decreased as shown in Fig. 6 (a), resulting in the increased circulating current and subsequent serious conduction loss. On the other hand, the proposed converter does not have any duty cycle loss and all energy stored in L_{lkg} is transferred to the output side until the current flowing through L_{lkg} becomes 0A as shown in Fig. 6 (b). Consequently, the circulating energy problem can be effectively solved.

4.4 Comparisons of device stresses

Table 1 shows the comparisons of device stresses between the conventional and proposed circuits. As shown in this table, the voltage stresses of the output diodes d_1 and d_2 in the conventional circuit reach so high as V_{in} at D=0.5 compared with V_o of the proposed circuit. Furthermore, the output diode of the conventional circuit suffers from the serious voltage ringing, which results in the increased voltage rating, forward voltage drop, and cost of the output diode. Therefore, a well-designed RC snubber must be used to protect the output diode from this voltage ringing, which could also generate serious power losses.

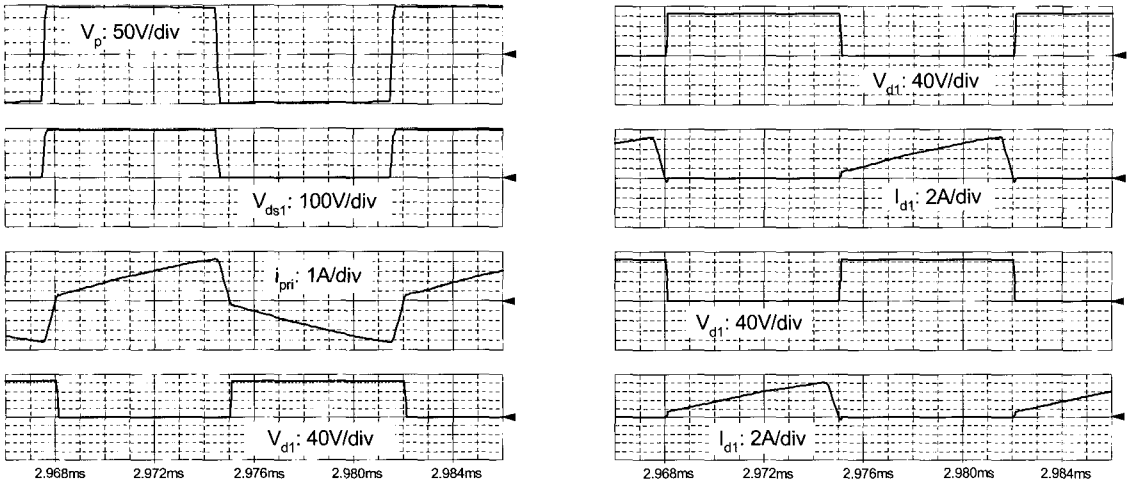

Fig. 7 Simulated results, (a) Key waveforms of v_p, v_{ds1}, i_{pri}, and v_{d1} (b) Key waveforms of v_{d1}, i_{d1}, v_{d2} and i_{d2}

Meanwhile, the current stresses of the output diodes d_1 and d_2 in the proposed circuit are rather large compared with those that in the conventional circuit. This is because the proposed converter employs the output structure of the half bridge configuration, which features the voltage/current doubling effects and simple structure. However, this is not so serious in low current and high voltage applications such as the PDP sustaining power module.

5. Topological extensions of the proposed circuit

The same concept presented to the proposed circuit in the previous section can be extended to any bridge-type DC/DC converter. A family of bridge-type ZVS PWM DC/DC converters is shown in Fig. 5. These converters can be classified into two groups according to their structure of the output stage. One is the full-bridge rectifier type and the other the half-bridge rectifier type. The output voltage of the latter is twice as high as that of the former by its voltage doubling action of the half bridge configuration in the output side under the same condition. On the other side, the current stress of the output rectifier in the latter is twice as high as that in the former.

The operational principles, features, and soft switching procedures of these converters are similar to that of the proposed circuit presented in section III.

6. Simulated and Experimental results

The prototype of the proposed circuit is implemented with specifications of V_{in}=385V, V_o=170V, rated power P_o=425W, L_{lkg}=32uH, C_B=2uF, C_{o1}=C_{o2}=4.4uF, C_o=560uF /250V, transformer turns ratio N_1:N_2=21:11, switching frequency=72kHz, d_1 and d_2=15ETH03, and M_1 and M_2= 2SK2837 (C_{oss}=1.165nF). Fig. 7 (a) and (b) show the simulated key waveforms using Orcad 9.2 at the full load. From these figures, since the voltages across d_1 and d_2 are clamped to the output voltage and turned off under zero current switching (ZCS) conditions, there is no serious voltage ringing in those diodes. Moreover, since all energy stored in L_{lkg} is transferred to the output side, no circulating energy exists. Fig. 8 (a) and (b) shows the experimental key waveforms at the full load. These waveforms exactly coincide with the simulated key waveforms. Fig. Fig. 8 (c) shows that the ZVS of M_1 and M_2 can be achieved at 40% load condition. Fig. 8 (d) shows that while the ZVS of M_2 is obtained at 10% load, M_1 is not. However, since the currents though M_1 are very small at this point, the switching loss is not serious. Fig. 9 shows the measured efficiency. The efficiency along a wide load range is as high as above 95%. Fig. 10 shows an industrial sample of a PDP power module employing the proposed converter.

7. Conclusion

A high efficiency ZVS PWM asymmetrical half bridge converter for PSPM is proposed in this paper. A small additional inductor, which also acts as an output filter inductor, can achieve the ZVS of power switches for the wide load range. The problem related to ringing in the secondary rectifier caused by the additional inductor can also be completely solved by employing a structure without an output filter inductor. In addition, since it has no large output inductor filter, it features a simpler structure, lower cost, less mass, and lighter weight.

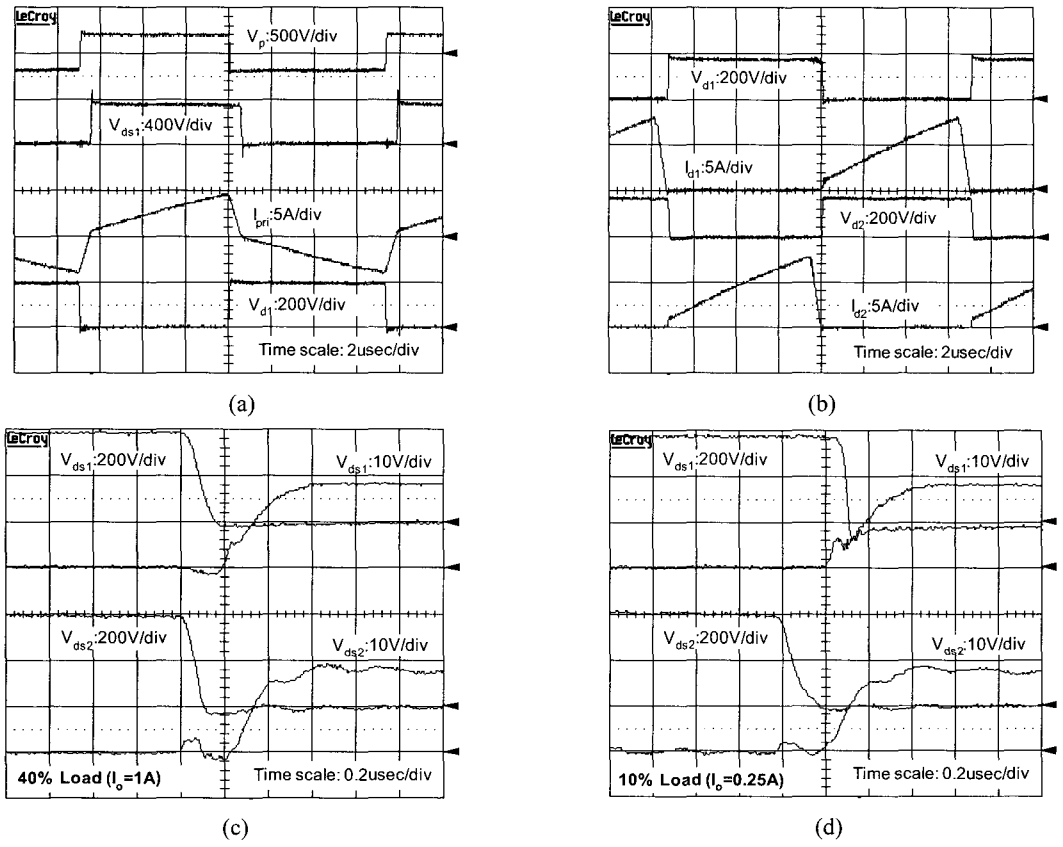

Fig. 8 Experimental waveforms, (a) Key waveforms of v_p, v_{ds1}, i_{pri}, and v_{d1} (b) Key waveforms of v_{d1}, i_{d1}, v_{d2} and i_{d2}, (c) ZVS turn on at 40% load (d) Hard switching and ZVS turn on at 10% load

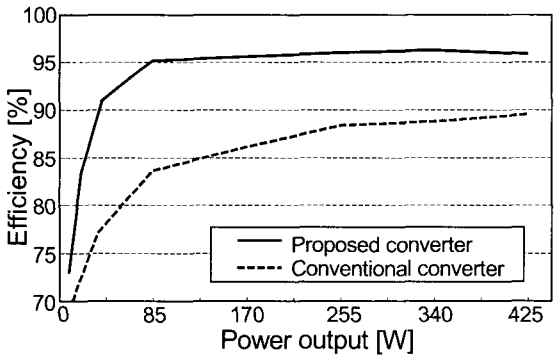

Fig. 9 Measured efficiency

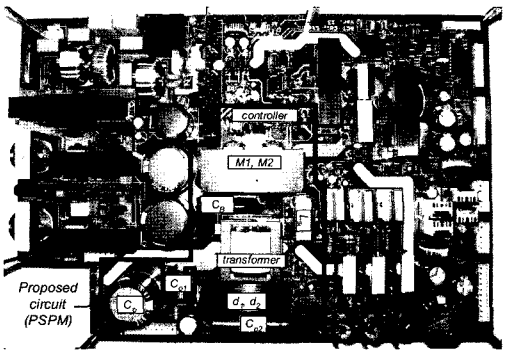

Fig. 10 Industrial sample of a PDP power module employing the proposed converter

Moreover, since all energy stored in the additional inductor is transferred to the output side, the circulating energy problem can be effectively solved and the overall system efficiency along a wide load range is as high as above 95%. The proposed PSPM is expected to be well suited to the wall hanging color PDP TV.

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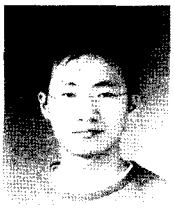

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