# Analysis and Calibration of Transient Enhanced Diffusion for Indium Impurity in Nanoscale Semiconductor Devices

**Jun-Ha Lee† and Hoong-Joo Lee***

**Abstract** - We developed a new systematic calibration procedure and applied it to the calibration of the diffusivity, segregation and TED model of the indium impurity. The TED of the indium impurity was studied under 4 different experimental conditions. Although the indium proved to be susceptible to the TED, the RTA was effective in suppressing the TED effect and in maintaining a steep retrograde profile. Just as in the case of boron, indium demonstrated significant oxidation-enhanced diffusion in silicon and its segregation coefficients at the $Si/SiO_2$ interface were significantly below 1. In contrast, the segregation coefficient of indium decreased as the temperature increased. The accuracy of the proposed technique has been validated by SIMS data and 0.13-㎛ device characteristics such as Vth and Idsat with errors less than 5% between simulation and experiment.

**Keywords**: calibration, indium impurity, nanoscale, transient enhanced diffusion

## 1. Introduction

Accurate and reliable TCAD (technology computer-aided-design) tools play a major role in the development and manufacture of semiconductors [1]. The progress of NSI (nano-scale integrated circuit) technologies to yield higher density DRAM, ultra-high performance and power chips requiring low energy has brought with them the need for use in a wide variety of methods employed by TCAD tools [2-3]. As a result of progress in areas such as process and device physics, utilization of experimental techniques and the power of computing, the TCAD has reached a level that was considered virtual fab, which uses the simulation environment. In silicon microelectronics, the understanding of impurity diffusion is one of the oldest research topics awaiting a satisfactory solution. Over the past few years, considerable progress was made towards the goal of being able to accurately predict doping profiles. In today's advanced and extremely scaled MOS technologies, the formation of shallow junctions is of particular interest. While extremely challenging from a modeling viewpoint, the approach of calibrating the process models to advanced experiments such as secondary ion mass spectroscopy (SIMS) or nano-spreading resistance profiles seems to be quite successful.

Indium, an acceptor dopant in Si, is an alternative of the boron impurity in the channel region for achieving a retrograde channel profile and reduces the SCE (Short Channel Effect) in sub 0.13 ㎛ MOSFETs. This SCE raises the sensitivity of the device electrical behavior to the technological process, via transient effects associated with RTP (Rapid Thermal Processing) [4-5]. Although some results have been published for the behavior of the indium impurity in the inert and oxidizing ambient [6-8], limited data exist for the TED (Transient Enhanced Diffusion) of indium in the RTA (Rapid Thermal Anneal) process [9]. Indium can make a steep channel profile due to its lower diffusivity and strong segregation into the oxide. In this study, the TED phenomena of the indium impurity in silicon are investigated in the range of damage generation from the high energy implantation for the well formation and heavy-dose implantation for the source/drain formation. In addition, the indium profile is systematically calibrated as a newly defined impurity in a process simulator. Finally, we demonstrate the results of 0.13-㎛ logic devices to which the indium impurity has been applied in the channel region to suppress the RSCE (Reverse Short Channel Effect) and enhance the device performance compared to the boron channel device.

## 2. Experiment and Calibration

The process simulator calibration environment based on the TCAD framework [10], as shown in Fig. 1, has been constructed to systematically extract ion-implantation and diffusion model parameters. The TCAD framework operates as manager of the database, the optimizer and runner to control the simulation status on distributed systems. The analytical modeling of ion implantation has

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shown good promise in actual applications. Compared to implantation, accurate and physics-based simulations of thermal annealing steps are considerably more challenging. Impurity diffusion in silicon occurs via a pair diffusion mechanism, which means that the impurity atoms join one or more point defects as an interstitial. These point defects are generated during previous process steps such as an ion implantation. Modern technologies require very shallow junctions below 0.1 μm, which leads to rather short annealing times in the range of a few seconds. Therefore, the diffusion kinetics can be characterized as extremely nonlinear and non-stationary, putting stringent conditions on the numerical methods employed for equation solution. Many aspects of the impurity-defect clustering and de-clustering processes are still unknown. It is for this reason that the calibration methodology should be developed. We analyze the implantation, gate oxidation and annealing process conditions of each process technology generation to make the critical point of the experiment window. Based on this experiment window, we process the short-loop experiment such as is presented in the right-hand box in Fig. 1. The SIMS data is stored as a data-base system for efficient handling [11]. From the target SIMS data, we optimize the parameters that are previously determined for each process condition by the sensitivity analysis. As in the case of the box diagram in the center left of Fig. 1, we sequentially extract the diffusion parameters starting from the intrinsic carrier concentration region with impurity diffusivity to TED (transient enhanced diffusion) parameters. Then the set of extracted parameters is validated by the device simulation in terms of electrical characteristics.

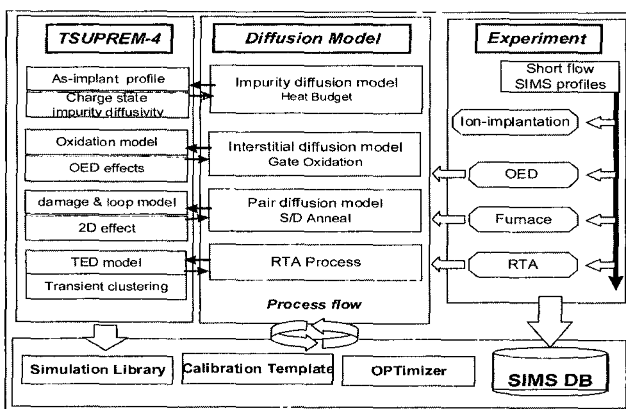


**Fig. 1** A calibration environment for process simulator

The new systematic calibration procedure of a process simulator for the indium impurity is demonstrated in Fig. 2. Unpatterned <100> oriented p-type silicon wafers were implanted with the indium impurity. The implant energy was varied between 120KeV and 180KeV. The dose was varied between 6.0E12 and 1.4E13 $cm^{-2}$.

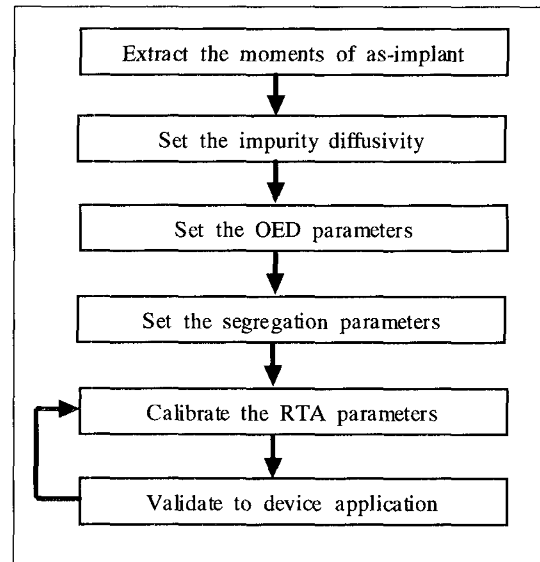


**Fig. 2** The process simulator calibration procedure for indium impurity.

The first was taken from the as-implanted indium SIMS profiles, in which we extracted 9-moments of the dual-Pearson model. The as-implanted calibration results agree well with SIMS data as presented in Fig. 3. The last was taken from previous results of the diffusivity parameters and the enhancement factor with segregation parameters during oxidation for the simulation model [12-13]. It is assumed that the equations governing the diffusion of indium in silicon are identical to those for the other dopants [14]. These results indicate that both indium and boron experience significant oxidation-enhanced diffusion in silicon and have segregation coefficients at the $Si/SiO_2$ interface much less than 1 at temperatures between 800℃ and 1050 ℃.

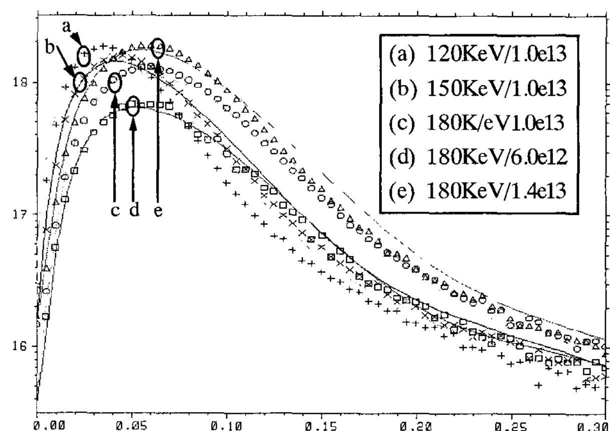


**Fig. 3** The calibration results of the as-implanted indium impurity compared to SIMS data.

## 3. Indium Impurity Simulation

However, the segregation coefficient of indium decreases as the temperature increases. In order to analyze the TED phenomena of the indium, we performed 4 groups of experiments as listed in Table 1.

**Table 1** Four groups of experimental conditions to analyze the TED phenomena of indium and boron in silicon.

| Group | RTA | Oxidation | As-implant | RTA |
|---|---|---|---|---|
| A | X | O | X | O |
| B | O | O | X | O |
| C | O | O | O | O |
| D | X | O | O | O |

The boron impurity was also experimented under the identical conditions for comparison. The purpose of these conditions is to extract the damage effect of the phosphorus high-energy implantation for the well formation and the arsenic heavy-dose implantation for the source/drain formation. The experiment was carried out as follows. Starting from the as-implanted wafers, the first RTA is performed prior to the oxidation on B and C groups only. Then, dry oxidation (850℃/30min.) and inert annealing (900℃/20min.) are applied to all wafers. To monitor how the TED affects the channel impurity redistribution, the damage generation is made on C and D groups by high dose (5.0E15 $cm^{-2}$) arsenic implantation, which is the condition for the source/drain process. Finally, the second RTA (1000℃/30sec) is processed. The SIMS data were obtained after removing the oxide layer. The TED calibrations are carried out with TSUPREM4 using a fully coupled model for dopant diffusion and a scaled "+1" model to account for point defects created by the implant damage [15-16]. The scaled damage factor is approximately 1-1.2 interstitials per implanted ion for phosphorus and 2-2.3 for arsenic. The simulation profiles for the final indium dopant show good agreement with the SIMS profiles as indicated in Fig. 4. The diffusion profiles are also calibrated as accurately as possible, because we analyzed the accuracy of doping profiles according to the variation of threshold voltages in the 0.13-$\mu m$ device, where 1% of channel profile can affect 50% of threshold voltage variation. Thus, if we predict the accuracy of threshold voltage within 10% compared to real data, we should calibrate the channel doping profile within 0.2% error.

The SIMS profiles of Fig. 4 and Fig. 5 have the first peak at 200Å depth. However, the SIMS data seem to be incorrect in this region so that we do not perform the calibration. Compared to the boron TED as shown in Fig. 5, the indium has the lower peak concentration and the surface concentration is much lower than the boron.

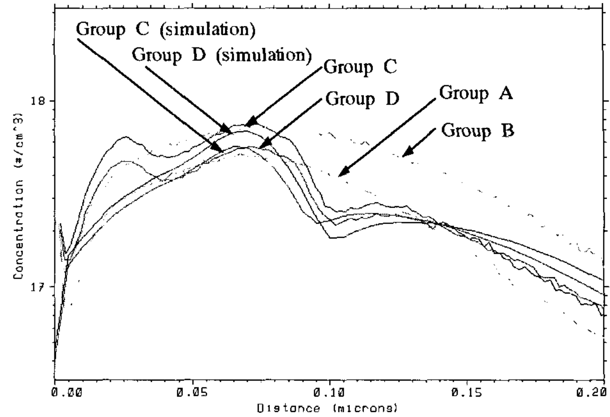


**Fig. 4** The comparison of simulation results to SIMS data for the indium TED effects.

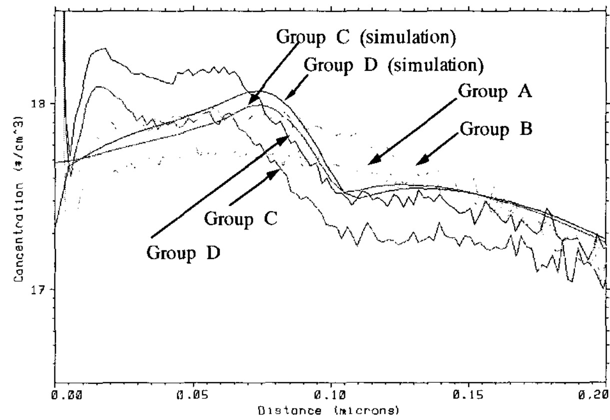


**Fig. 5** The comparison of simulation results to SIMS data of the boron TED effects.

To validate our calibrated RTA model parameters for the indium, we applied the parameters to the 0.13-$\mu m$ logic devices.

In this process, the indium is implanted instead of the boron through a 110Å screen oxide layer to adjust the threshold voltage. Fig. 6 presents the simulated and experimental data of RSCE for both of the indium and the boron implanted devices. If the TED effect is not included in the indium implantation, the RSCE cannot be modeled [17-19]. Using the TED calibration, we can improve the RSCE estimation by about 20%.

The indium profile at the center of the channel becomes broader and the surface concentration increases as the gate length reduces. As the interstitials diffuse laterally from the S/D to the channel region, the channel profile broadens. In addition, the surface concentration pile-up is the result of the gradient in the interstitial concentration produced by recombination at the silicon/oxide interface. The gradient in the interstitial concentration produces the gradient of dopant/interstitial pairs resulting in the diffusion of these pairs towards the $Si/SiO_2$ interface. The gradient of

interstitials towards the surface increases as the channel length decreases; thus, the flux of dopant/defect pairs is augmented. Due to the strong segregation combined with the TED effect of the indium impurity into the gate oxide, the indium pile-up near the surface is reduced, and consequently, the RSCE of an indium-channel device is smaller than that of a boron-channel device. The Vth roll-up is reduced from 70mV to 40mV and the slope of the roll-off is reduced from 150mV to 90mV.

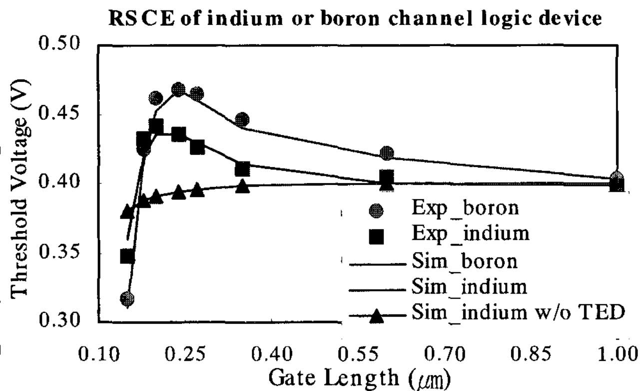


**Fig. 6** The simulation and experimental data of RSCE of a logic device with the indium implanted channel

## 4. Conclusion

We developed a new systematic calibration procedure that was applied to the calibration of the diffusivity and TED model of the indium impurity. The TED of the indium impurity has been studied under 4 different experimental conditions. Although the indium was susceptible to the TED, the RTA was effective in suppressing the TED and maintaining a steep retrograde. The accuracy of the proposed technique was validated by SIMS data and 0.13-μm device characteristics such as Vth and Idsat with errors less than 5% between simulation and experiment. With this calibration tool, we can optimize and integrate the process conditions for developing high performance devices scaled down to the 0.1-μm region by suppressing the RSCE and increasing the driving capability of a device.

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