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A Unified Carrier Based PWM Method In Multilevel Inverters

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ABSTRACT

This paper presents a systematic approach to study the carrier based pulse width modulation (PWM) techniques applied to diode-clamped and cascade multilevel inverters by using multi-modulating patterns. This method is based on the description of controllable redundant parameters in the modulating signals. A unified mathematical formulation is presented for carrier based PWM methods, which obtains outputs similar to the corresponding space vector PWM. A full and separate control of the fundamental voltage, vector redundancies and phase redundancies can be obtained in the carrier based PWM.

In this paper, the proposed PWM method and corresponding algorithm for generating multi-modulating signals will be formulated and demonstrated by our simulations.

Keywords: Multi-carrier, Multilevel inverter, multi-modulating patterns, Multi-modulation

1. Introduction

The two most common multilevel inverter topologies are the diode-clamped and cascade inverters as shown in Fig.1 and Fig.2. For their control, the carrier based unipolar PWM (CPWM) and space vector PWM (SVPWM) methods have been used the most in practice [1]-[3]. The SVPWM is implemented based on a vector diagram and highlighted for its control flexibility. The implementation at higher level inverters still remains sophisticated.

The CPWM technique is implemented using carrier waves and modulating signals. For the diode-clamped inverter, the multi-carrier phase disposition technique (PD) shows a proper solution. For the cascade inverter, the PD discontinuous PWM would give similar performance[4]. Even though the previous PWM methods have been developing in practice for years, the correlation between them has been accepted based on somewhat heuristic investigations[3]. The concept of vector redundancy, which presents a flexible character of the SVPWM technique, has not been presented in the CPWM methods. The modulating pattern(MP) method has appropriately clarified the vector character of the SVPWM-CPWM correlation[5]. The vector redundancy is presented by related redundant factors in the zero sequence function.

Recent studies[6],[7] have shown that if more active redundant vectors in the smallest triangle area are involved in the sampling period (Fig.3c), better regulation of the dc neutral point voltage can be obtained. However, the unipolar PWM is not available for this purpose. The cascade multilevel inverter has its phase redundancies.

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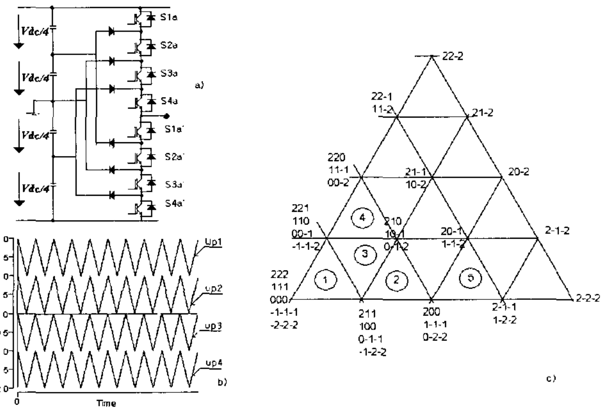

Fig. 1 A-phase leg circuit, carrier waves and modulating pattern diagram of a five-level diode-clamped inverter

The problem is that the phase redundancies are hidden from the vector diagram and the unipolar PWM can not distinguish the phase redundancies. In several methods, to utilize the phase redundancies, modified modulating signals or modified multi carrier wave systems have been introduced[3],[4],[8]. However, a unified mathematical formulation would be needed to represent vector redundancies and phase redundancies in the reference modulating signals.

The previously described problems can be solved by using carrier-based multi-modulation, which has several modulating signals per phase and represents vector and phase redundancies by corresponding multi-modulating patterns(MMP). The proposed multi-modulation is able to implement a maximum number of active redundant vectors and fully control the phase redundancies in cascade multilevel inverters.

This paper describes MMP, multi-modulation equations and introduces an algorithm to generate multi-modulating signals. In a three-phase multilevel inverter the fundamental voltage, vector redundancies and phase redundancies can all be controlled separately in the PWM modulator. This makes the control more flexible.

2. Basic Terminology

The multi-carrier phase disposition (PD) technique will be selected as a unified carrier wave system in the proposed method as shown in Fig.4.

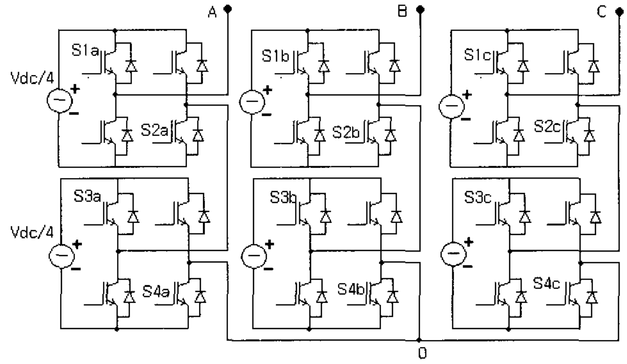

Fig. 2 Circuit diagrams of a five-level cascade inverter

Vector analysis has been used effectively to study the SVPWM control of multilevel inverters. In the *abc* coordinate system, the reference vector $\vec{V}^* = [v_a, v_b, v_c]^T$ can be analyzed as a linear combination of three pivot vectors $\vec{U}_1, \vec{U}_2$ and $\vec{U}_3$ as follows:

$$\vec{V}^* = K_1\vec{U}_1 + K_2\vec{U}_2 + K_3\vec{U}_3 \tag{1}$$

$$K_1 + K_2 + K_3 = 1; \quad 0 \le K_1, K_2, K_3 \le 1 \tag{2}$$

The reference $\vec{V}^*$ consists of an active component $\vec{V}_{12} = [v_{a12}, v_{b12}, v_{c12}]^T$ and a zero sequence component $\vec{V}_0 = v_0[1,1,1]^T$. Let's define a fundamental modulating function $(v_{ra(1)}, v_{rb(1)}, v_{rc(1)})$ in relation to the voltage vector amplitude and argument, and dc voltage as

$$\begin{aligned} v_{ra(1)} &= \frac{V_{12}}{V_{dc}/(n-1)}\cos\theta \\ v_{rb(1)} &= \frac{V_{12}}{V_{dc}/(n-1)}\cos(\theta - 2\pi/3) \\ v_{rc(1)} &= \frac{V_{12}}{V_{dc}/(n-1)}\cos(\theta + 2\pi/3). \end{aligned} \tag{3}$$

Let's define functions Max and Min the largest and smallest values from among $(v_{ra(1)}, v_{rb(1)}, v_{rc(1)})$ and function Mid as the value between the Max and

Min values. The parameters K_1 , K_2 and K_3 are proportional to the switching time durations T_1, T_2 and T_3 of the three pivot vectors and they can be calculated as follows [5]:

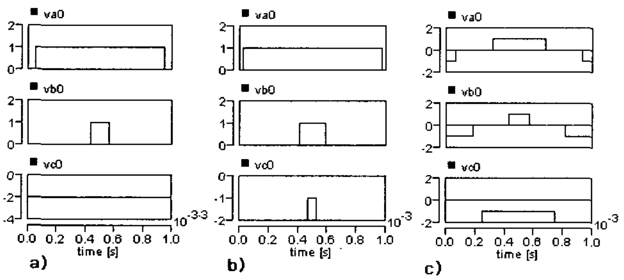

Fig. 3 Different sequences of voltage states va0,vb0 and vc0 with a) three switching states, b) four switching states and c) six switching states

$$\left.\begin{array}{l} K_1 = 1 + Int(Max - Min) - (Max - Min) \\ K_2 = -Int(Max - Mid) + (Max - Mid) \end{array}\right\} for \quad TVMINR-areas$$
$$\left.\begin{array}{l} K_1 = 1 + Int(Mid - Min) - (Mid - Min) \\ K_2 = 1 + Int(Max - Mid) - (Max - Mid) \end{array}\right\} for \quad TVMAXR-areas$$
$$K_3 = 1 - K_1 - K_2 \tag{4}$$

where the conditions for TVMINR (two vector with minimum level of redundancy) and TVMAXR (two vector with maximum level of redundancy) areas are:

$$S = Int(Max - Min) - Int(Max - Mid) - Int(Mid - Min)$$
$$\cdot \; S = \begin{cases} 0 & for \quad TVMINR \quad - areas \\ 1 & for \quad TVMAXR \quad - areas \; . \end{cases} \tag{5}$$

Under consideration of the existing redundancies of three pivot voltage vectors, a complete expression of the reference vector can be performed as follows:

$$\begin{aligned} \vec{V} = & K_1\left(\xi_{10}\vec{U}_{10} + \xi_{11}\vec{U}_{11} + ... + \xi_{1,lr1}\vec{U}_{1,lr1}\right) + \\ & K_2\left(\xi_{20}\vec{U}_{20} + \xi_{21}\vec{U}_{21} + ... + \xi_{2,lr2}\vec{U}_{2,lr2}\right) + \\ & K_3\left(\xi_{30}\vec{U}_{30} + \xi_{31}\vec{U}_{31} + ... + \xi_{3,lr3}\vec{U}_{3,lr3}\right) \end{aligned} \tag{6}$$

where the parameters l_{rj} , corresponding to the vectors $\vec{U}_j$, $j = 1,2,3$ termed as levels of vector redundancies are determined for an n-level inverter as follows:

$$\begin{aligned} l_{r1} &= n - 1 - Int(Max - Min) \\ l_{r2} &= n - 2 - Int(Mid - Min) - Int(Max - Mid) \\ l_{r3} &= l_{r1} - 1. \end{aligned} \tag{7}$$

The distribution of the switching time durations of redundant vectors defined by the parameters ξ_{jk} , $j = 1,2,3$; $k = 0,1,2,..,l_{rj}$ satisfies the following conditions as

$$\xi_{j0} + \xi_{j1} + \xi_{j2} + ... + \xi_{j,lrj} = 1 \;\; ; \xi_{jk} \geq 0 \, . \tag{8}$$

Three vectors $\vec{U}_{10}, \vec{U}_{20}$ and $\vec{U}_{30}$ termed as vectors with zero redundant factors (ZRF) satisfy the condition as

$$U_{a10} + U_{b10} + U_{c10} < U_{a20} + U_{b20} + U_{c20} < U_{a30} + U_{b30} + U_{c30} . \tag{9}$$

Any of the redundant vectors $\vec{U}_{j0}, \vec{U}_{j1}, ...\vec{U}_{jlrj}$, $j = 1,2,3$ can be expressed through ZRF vector as follows:

$$\vec{U}_{jk} = \vec{U}_{j0} + kV_{dc} / (n-1)\vec{I} \tag{10}$$

$\vec{I} = [1,1,1]^T$ is a unit vector and parameter k is a redudant factor.

Modulating pattern (MP) is defined as a set of three small phase signals, corresponding to voltage vector $\vec{U}_{jk}$ and derived from the dc-voltage source V_{dc} as follows:

$$\vec{P}_{jk} = \vec{U}_{jk}(n-1)/V_{dc} = \left[P_{ajk}, P_{bjk}, P_{cjk}\right]^T \tag{11}$$

Each component as P_{ajk}, P_{bjk} and P_{cjk} presents *a phase modulating pattern (PMP)*. All the MPs are presented in an MP vector diagram (Fig.1c). Three MPs with the lowest zero sequence $\vec{P}_{j0}$ can be determined as follows:

$$\begin{aligned} [P_{a10}, P_{b10}, P_{c10}]^T = & [P_{min}, P_{min}, P_{min}]^T + \\ & \left[Int(v_{ra(1)} - Min), Int(v_{rb(1)} - Min), Int(v_{rc(1)} - Min)\right]^T \end{aligned}$$

$$[P_{a20}, P_{b20}, P_{c20}]^T = [P_{a10}, P_{b10}, P_{c10}]^T + \begin{cases} [f_{\max a}, f_{\max b}, f_{\max c}]^T & for \quad S=0 \\ [f_{mida}, f_{midb}, f_{midc}]^T & for \quad S=1 \end{cases}$$

$$[P_{a30}, P_{b30}, P_{c30}]^T = [P_{a10}, P_{b10}, P_{c10}]^T + [f_{mida} + f_{\max a}, f_{midb} + f_{\max b}, f_{midc} + f_{\max c}]^T \tag{12}$$

where

$$f_{\max x} = \begin{cases} 1 & for \quad v_{rx(1)} = Max \quad ; \quad x = a,b,c \\ 0 & else \end{cases} \tag{13}$$

$$f_{midx} = \begin{cases} 1 & for \quad v_{rx(1)} = Mid \quad ; \quad x = a,b,c \\ 0 & else \end{cases} \tag{14}$$

The value $P_{\min}$ is constant and equal to the smallest PMP components in the MP diagram. For odd level n, $P_{\min} = -(n-1)/2$. From (10) and (11), any MP $\vec{P}_{jk}$ can be expressed through the corresponding ZRF MP and redundant factor as follows:

$$\vec{P}_{jk} = \vec{P}_{j0} + k\vec{I} \;; 0 \le k \le l_{rj}, j = 1,2,3 \tag{15}$$

Example 1: For area 2 in Fig.1, the parameters can be determined as follows:

S=0; $l_{r1} = 3$ and $l_{r2} = l_{r3} = 2$; $\vec{P}_{10} = [-1,-2,-2]^T$, $\vec{P}_{20} = [0,-2,-2]^T$, $\vec{P}_{30} = [0,-1,-2]^T$. It is satisfied, for instance: $\vec{P}_{12} = [1,0,0]^T = [-1,-2,-2]^T + 2[1,1,1]^T = \vec{P}_{10} + 2\vec{I}$

3. Correlation between the multi-carrier multi-modulation and SVPWM

3.1 Multi-modulating pattern

In multi-modulation, each phase voltage is performed by a set of p-modulating signals, p>1. Each modulating signal is used to control N_{sw} switching pairs. If N_{sw}=1, there are p=(n-1) signals per phase and the corresponding PWM is defined as a full multi-modulation. For 1<p<(n-1), the system is simpler- termed as partial multi-modulation (see Fig.4b), however its redundant capability is appropriately decreased. Unlike the unipolar PWM, which requires a limit modulating signal for producing the corresponding phase voltage (or PMP), the multi-modulation needs a p-modulating signal set for producing a PMP. Each standard p-modulating signal set for determining a phase voltage output is termed as a phase multi-modulating pattern (PMMP). The combination of three PMMP makes up a multi-modulating pattern (MMP), which generates a voltage vector.

The MMP can be considered as an extension of the MP, where vector elements in a CPWM equation are replaced by corresponding matrices. In a full multi-modulation, each MMP has a dimension of 3x(n-1) and fully determines the switching states of a multilevel inverter.

The matrix MMP $\lfloor Q_{jk} \rfloor$ is defined as follows:

$$\lfloor Q_{jk} \rfloor = \begin{bmatrix} Q_{ajk1}, Q_{ajk2}, & , Q_{ajkp} \\ Q_{bjk1}, Q_{bjk2}, \ldots, Q_{bjkp} \\ Q_{cjk1}, Q_{cjk2}, & , Q_{cjkp} \end{bmatrix} ; \begin{matrix} 1 \le p \le (n-1) \\ k = 0,1,2,..,l_{rj} \\ j = 1,2,3 \end{matrix} \tag{16}$$

where (Q_{ajk1} , Q_{ajk2} ,..., Q_{ajkp}), (Q_{bjk1} , Q_{bjk2} ,..., Q_{bjkp}) and (Q_{cjk1} , Q_{cjk2} ,..., Q_{cjkp}) are three *PMMP* sets, corresponding to three *PMP* s as P_{ajk}, P_{bjk} and P_{cjk} .

Full multi-modulation –in a five-level inverter, a full multi-modulation requires four modulating signals per phase. For instance, four A-phase signals as $v_{ra1}, v_{ra2}, v_{ra3}$ and v_{ra4} , which vary in the corresponding ranges of (1,2),(0,1),(-1,0), and (-2,-1), respectively are shown in Fig.4c Intersections between these signals with the carrier waves u_{p1} ($1 \le u_{p1} \le 2$), u_{p2} ($0 \le u_{p2} \le 1$), u_{p3} ($-1 \le u_{p3} \le 0$), and u_{p4} ($-2 \le u_{p4} \le -1$) will determine the switching states of the corresponding switching pairs S_{1a}, S_{2a}, S_{3a} and S_{4a} (see Fig.1 and Fig.2). For instance, to obtain the A-phase voltage equal to $V_{dc}/2$ (PMP=2), the states of the switching pairs will be $S_{1a} = S_{2a} = S_{3a} = S_{4a} = ON$. This can be satisfied by a *PMMP* set consisting of 4 signals as $v_{ra1} = 2, v_{ra2} = 1, v_{ra3} = 0$ and $v_{ra4} = -1$, or in short PMMP (2,1,0,-1). Similarly, the other *PMMP* s can be deduced and filled in Table 1a.

For a diode clamped inverter, there is only one set of PMMPs.

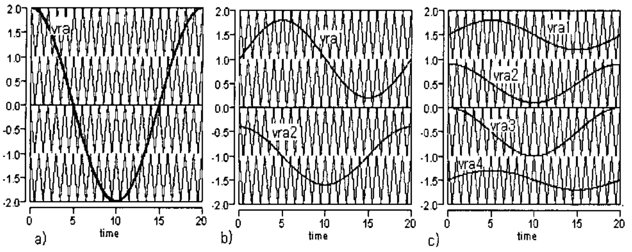

Fig. 4 Five-level inverter: the diagrams of carrier waves and A-phase modulating signals of a) unipolar PWM, b) partial multi-modulation, c) full multi-modulation.

Table 1 Five-level inverter: the *PMMP* sets for multi-carrier multi-modulation

a) For diode clamped inverter

PMP	-2	-1	0	1	2
PMMP set	1,0,-1,-2	1,0,-1,-1	1,0,0,-1	1,1,0,-1	2,1,0,-1

b) For cascade inverter

PMMP	1,0,-1,-2	2,0,-1,-2 1,1,-1,-2 1,0,0,-2 1,0,-1,-1	1,1,-1,-1 2,0,0,-2 2,0,-1,-1 2,1,-1,-2 1,1,0,-2 1,0,0,-1	2,0,0,-1 2,1,-1,-1 2,1,0,-2 1,1,0,-1	2,1,0,-1
Set 1	1,0,-1,-2	1,0,-1,-1	1,0,0,-1	1,1,0,-1	2,1,0,-1
Set 2	1,0,-1,-2	2,0,-1,-2	2,0,-1,-1	2,0,0,-1	2,1,0,-1
Set 3	1,0,-1,-2	1,1,-1,-2	1,1,-1,-1	2,1,-1,-1	2,1,0,-1
Set 4	1,0,-1,-2	1,0,0,-2	2,0,0,-2	2,1,0,-2	2,1,0,-1
…..					

For the cascade inverter, in a similar process, all possible *PMMP* s can be described in Table 1b. For example, there are four *PMMP* s for generating the *PMP* -1 . The MP $[-2,1,2]^T$ can be generated by one of four *MMP* s described as follows :

$$\begin{bmatrix}1,0,-1,-2\\2,0,0,-1\\2,1,0,-1\end{bmatrix},\begin{bmatrix}1,0,-1,-2\\2,1,-1,-1\\2,1,0,-1\end{bmatrix},\begin{bmatrix}1,0,-1,-2\\2,1,0,-2\\2,1,0,-1\end{bmatrix},\begin{bmatrix}1,0,-1,-2\\1,1,0,-1\\2,1,0,-1\end{bmatrix}$$

The *PMMP* set would be selected so that each $t-$ element (Q_{xjkt}) increases once while the *PMP* varies from minimum to maximum (from -2 to 2 in Table 1b). Therefore, four sets in Table 1b are applicable.

3.2 Correlation between the SVPWM and multi-modulation

The reference modulating signals in a multi-modulation can be expressed as follows:

$$[v_r]=\sum_{j=1}^{3}K_j\left(\xi_{j0}[Q_{j0}]+\xi_{j1}[Q_{j1}]+\ldots+\xi_{j,lrj}[Q_{j,lrj}]\right) \qquad (17)$$

where the reference modulating signals and MMP are expressed in matrix forms as

$$[v_r]=\begin{bmatrix}v_{ra1},v_{ra2},\ldots,v_{rap}\\v_{rb1},v_{rb2},\ldots,v_{rbp}\\v_{rc1},v_{rc2},\ldots,v_{rcp}\end{bmatrix};$$

$$[Q_{jk}]=\begin{bmatrix}Q_{ajk1},Q_{ajk2},\ldots,Q_{ajkp}\\Q_{bjk1},Q_{bjk2},\ldots,Q_{bjkp}\\Q_{cjk1},Q_{cjk2},\ldots,Q_{cjkp}\end{bmatrix};$$

$$j=1,2,3 \qquad k=0,1,2,..,l_{rj} \qquad (18)$$

$(P_{\min}+n-1-t)\leq v_{rxt}\leq(P_{\min}+n-t)$, t=1,2,..,p .

The combinations ($v_{ra1},v_{ra2}\ldots v_{rap}$), ($v_{rb1},v_{rb2}\ldots v_{rbp}$) and ($v_{rc1},v_{vc2}\ldots v_{rcp}$) are three reference p-modulating signal sets, corresponding to the A-, B- and C- phase voltages. For full multi-modulation, a maximum of $(l_{r1}+l_{r2}+l_{r3}+3)$ states can be involved in a sampling time period. The meaning of (17) is that: the reference modulating signals produced by (17) will generate the output voltages in a sequence of the related redundant vectors as $\vec{U}_{10},\vec{U}_{20},\vec{U}_{30},\vec{U}_{11},\vec{U}_{21},\ldots$ to $\vec{U}_{1,lr1},\vec{U}_{2,lr2}$, $\vec{U}_{3,lr3}$ for TVMAXR areas and $\vec{U}_{2,lr2},\vec{U}_{3,lr3},\vec{U}_{1,lr1}$ for TVMINR areas. Their switching time durations are proportional to the corresponding coefficients as $K_1\xi_{10}, K_2\xi_{20}, K_3\xi_{30}, K_1\xi_{11}, K_2\xi_{21},..$ to $K_1\xi_{1,lr1}$, $K_2\xi_{2,lr2}, K_3\xi_{3,lr3}$ for TVMAX areas and $K_2\xi_{2,lr2}$, $K_3\xi_{3,lr3}$, $K_1\xi_{1,lr1}$, for TVMINR areas.

The validity of (17) can be illustrated for area 5 (Fig.1) with the assumption that five MPs $\vec{P}_{10}, \vec{P}_{20}, \vec{P}_{30}, \vec{P}_{11}$ and $\vec{P}_{21}$ are in a switching sequence. Their corresponding time duties are subsequently $K_1\xi_{10}, K_2\xi_{20}, K_3\xi_{30}, K_1\xi_{11}$ and $K_2\xi_{21}$. From the given sequence and MP diagram in Fig.1, the related MP components P_{ajk}, P_{bjk} and P_{cjk} can be derived. Let's suppose that PMMP set 2 from Table 1b is selected, the PMMP diagrams as $Q_{ajk1} \ldots Q_{ajk4}$ in relation to the MPs P_{ajk} can be deduced. The reference modulating signals can be derived as $v_{ra1} = 2, v_{ra4} = -1$ and

$$v_{ra2} = K_1\xi_{10}Q_{a102} + K_2\xi_{20}Q_{a202} + K_3\xi_{30}Q_{a302} + K_1\xi_{11}Q_{a112} + K_2\xi_{21}Q_{a212} = K_2\xi_{21}$$

$$v_{ra3} = K_1\xi_{10}Q_{a103} + K_2\xi_{20}Q_{a203} + K_3\xi_{30}Q_{a303} + K_1\xi_{11}Q_{a113} + K_2\xi_{21}Q_{a213} = -K_1\xi_{10}$$

3.3 Characteristics of multi-carrier multi-modulation

From the definition of MMP, a phase MP can be derived from MMP components as

$$P_{xjk} = Q_{xjk1} + Q_{xjk2} + .. + Q_{xjkp} = \sum_{t=1}^{p} Q_{xjkt} \,; x = a,b,c \tag{19}$$

The common mode of pattern can be evaluated by :

$$CM_{Pjk} = (P_{ajk} + P_{bjk} + P_{cjk})/3 = (\sum_{x=a,b,c} \sum_{t=1}^{p} Q_{xjkt})/3 \tag{20}$$

The effective modulating signal v_{rxe} , $x = a,b,c$ which is proportional to the phase of the dc-neutral point voltages V_{x0}, that is $V_{x0} = v_{rxe}V_{dc}/(n-1)$; can be determined from the corresponding p-modulating set as follows:

$$v_{rxe} = (v_{rx1} + v_{rx2} + .. + v_{rxp}) = \sum_{t=1}^{p} v_{rxt} \,. \tag{21}$$

From (17)-(19) and (21), the signal v_{rxe} can be expressed through modulating MP and redundant factors as

$$v_{rxe} = \sum_{j=1}^{3} K_j (\xi_{j0}P_{j0} + \xi_{j1}P_{j1} + \ldots + \xi_{jlrj}P_{j,lrj}) \,. \tag{22}$$

In (22), the condition (8) is satisfied. The effective zero sequence function, proportional to the zero sequence voltage, can be derived as follows:

$$v_{r0e} = (v_{rae} + v_{rbe} + v_{rce})/3 = (\sum_{x=a,b,c} \sum_{t=1}^{p} v_{rxt})/3 \tag{23a}$$

$$v_{r0e} = P_{min} - Min + \sum_{j=1}^{3} K_j \left(\xi_{j1} + 2\xi_{j2} + \ldots + l_{rj}\xi_{j,lrj}\right) \tag{23b}$$

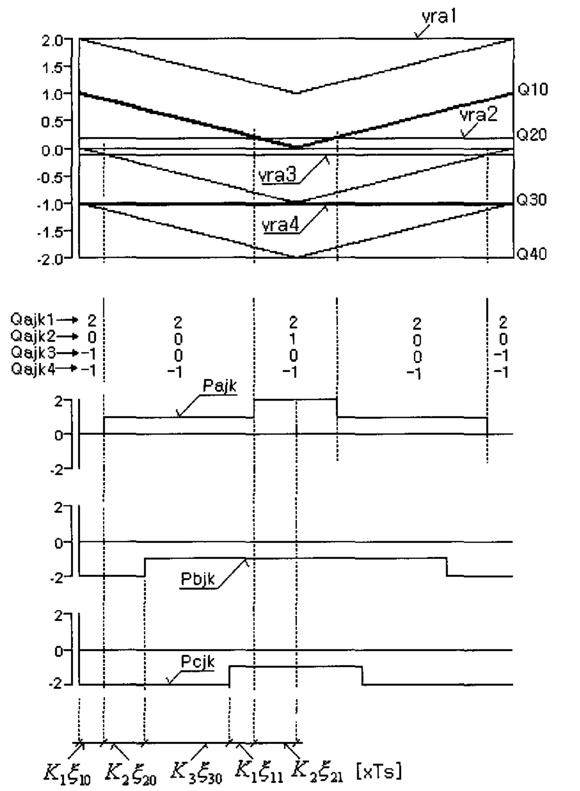

Fig. 5 Illustration of multi-modulation equation for area 5 in Fig. 1

4. Examples, simulation results

For the demonstration, the first *PMMP* set in Table 1b can be applied to both inverter topologies, consisting of the following *PMMP* s as (1,0,-1,-2), (1,0,-1,-1), (1,0,0,-1), (1,1,0,-1) and (2,1,0,-1). The remaining PMMP sets can be applied only for the cascade inverter.

Example 3: SVPWM control with the smallest zero sequence

The SVPWM method can be performed by directly putting the redundant parameters into (17). In this case, it is required to set $\xi_{10} = \xi_{11} = 0{,}5$ and $\xi_{20} = \xi_{30} = 1$, corresponding to a switching sequence of the vectors $\vec{U}_{10}, \vec{U}_{20}, \vec{U}_{30}$ and $\vec{U}_{11}$. Two active redundant vectors $\vec{U}_{10}$ and $\vec{U}_{11}$ are centered in a sampling period. Reference modulating signals are determined as

$$[v_r'] = 0.5K_1([Q_{10}]+[Q_{11}]) + K_2[Q_{20}] + K_3[Q_{30}] \quad (24)$$

Parameters K_1, K_2 and K_3 are determined using (4). To determine the matrices $[Q_{10}],[Q_{20}]$ and $[Q_{30}]$, first, one must calculate the related MPs as $\vec{P}_{10}, \vec{P}_{20}$ and $\vec{P}_{30}$, using (12). Then the transformation $\vec{P} \leftrightarrow [\vec{Q}]$ can be implemented by Table 1b. The A-phase modulating signals are shown in Fig. 6.

Example 4: Vector redundancy control- Multi-switching states

From the vector diagram in Fig.1, it can be deduced that for m<0.75, more than 7 switching states can be obtained in a sampling period. For demonstration, the parameters are set as $\xi_{10} = \xi_{11} = \xi_{20} = \xi_{21} = 0.5$ and $\xi_{30} = 1$, corresponding to a switching sequence of five vectors as $\vec{U}_{10}, \vec{U}_{11}, \vec{U}_{20}, \vec{U}_{21}$ and $\vec{U}_{30}$. From among them, two pairs of active redundant vectors are $\vec{U}_{10}, \vec{U}_{11}$ and $\vec{U}_{20}, \vec{U}_{21}$. The reference modulating signals can be determined as follows:

$$[v_r] = 0.5K_1([Q_{10}]+[Q_{11}]) + 0.5K_2([Q_{20}]+[Q_{21}]) + K_3[Q_{30}] \quad (25)$$

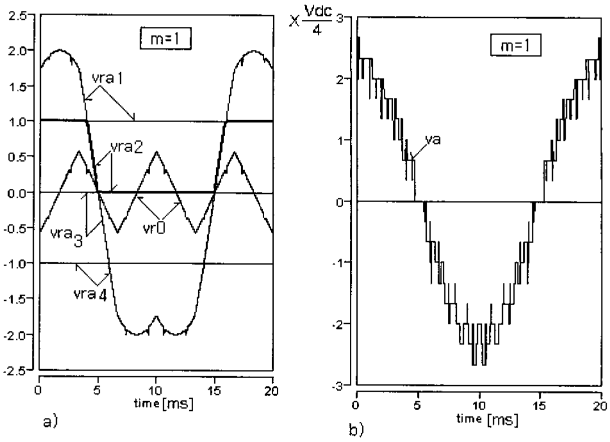

Fig. 6 Five-level inverter- Equally-centered PWM with four switching states: Diagrams of a) A-phase modulating signal set and effective zero sequence and b) A-phase voltage for m=1

The matrices $[Q_{10}],[Q_{20}]$ and $[Q_{30}]$ can be determined similarly as in the previous case. To determine the matrices $[Q_{11}],[Q_{21}]$, one must calculate the MP as $\vec{P}_{11}, \vec{P}_{21}$, which is related to the MP $\vec{P}_{10}, \vec{P}_{20}$ as follows: $\vec{P}_{11} = \vec{P}_{10} + [1,1,1]^T$ and $\vec{P}_{21} = \vec{P}_{20} + [1,1,1]^T$

From the obtained MP and Table 1b, the transformation $\vec{P} \leftrightarrow [Q]$ can be deduced. The diagrams of the reference A-phase modulating signals are shown in Fig.7.

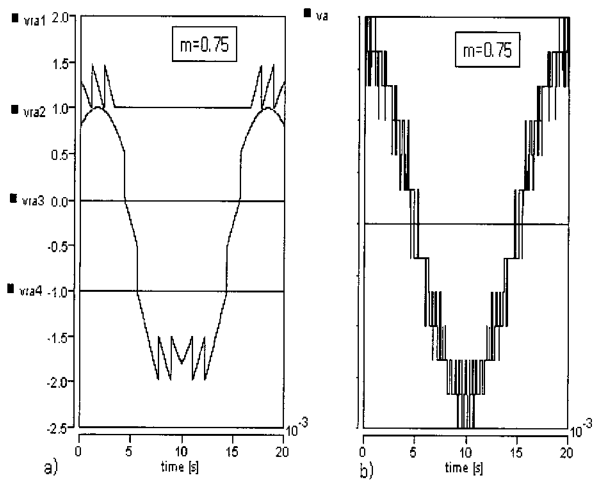

Fig. 7 Five-level inverter- Equally-centered PWM with five switching states: Diagrams of modulating signal set of the A-phase and output phase voltage for m=0.75

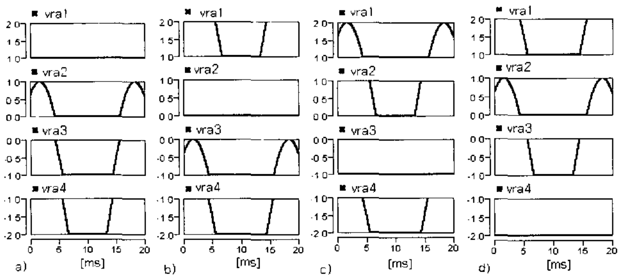

Fig. 8 Five-level inverter -- Discontinuous PWM: Diagrams of the A-phase modulating signal sets for various selected PMMP modulating patterns, m=0.75

Example 5: Phase redundancy control

Utilizing phase redundancies, the smallest zero sequence is required to implement a discontinous PWM. The modulating signals can be derived by equation as

$$[v_r]=K_1[Q_{10}]+K_2[Q_{20}]+K_3[Q_{30}] \tag{26}$$

In Fig.8, the diagrams illustrate a phase redundancy control by substituting subsequently four *PMMP* sets from Table 1b into CPWM equation (17). The discontinuous PWM mode occurs by using three vectors $\vec{U}_{10}, \vec{U}_{20}, \vec{U}_{30}$ $(\xi_{10} = \xi_{20} = \xi_{30} = 1)$ occurs. With different *PMMP* sets, the phase redundant control alternates switching pairs and redistributes the switching losses among them.

As can be seen in Fig.7 and Fig.8, the PD discontinuous PWM for cascade inverters described in[3],[4] can be understood as a special case of the full multi-modulation. In a PD discontinuous PWM, the switching loss among the devices is balanced by moving the reference waveform sections between $(n-1)/2$ cascaded inverters. For example, in Fig.2 reference waveform sections are moved between switching pairs S_{1a} and S_{3a} (or between S_{2a} and S_{4a}). This technique is effective for symmetrical reference waveforms in two half periods.

Unlike the PD discontinuous PWM, in multi-modulation each of the (n-1) phase legs functions equally and their waveform sections (corresponding to $(S_{1a}, S_{2a}, S_{3a}, S_{4a})$) can be swapped with each other. All these can be implemented using digital circuits. Therefore, multi-modulation is better than the PD discontinuous PWM because it can balance the switching loss among the devices over the whole modulation index range and for any reference waveform. The PMMP sets and the moving instants should be selected to minimize the number of extra switchings. Moreover, the PD discontinuous PWM is not able to obtain any arbitrary switching state combination.

5. Conclusions

In this paper, the generalized correlation between SVPWM and CPWM methods has been presented. It has been shown that the carrier based unipolar/multi- PWM methods can be described in a unified form using (multi)modulating patterns. Their difference is given by the number of modulating signals, which is related to the maximum number of voltage states in a switching sequence. Multi-modulation balances the switching losses of devices in a cascade inverter by exchanging the modulation pattern sets. Multi-modulation would be useful for balancing the neutral point voltage in a diode clamped inverter by capability to obtain an arbitrary vector from its redundancies. The main drawback of this method is the large number of modulating signals required. This can be improved by introducing single carrier multi-modulation with digital technique support. Another possible variation is to use partial multi-modulation.

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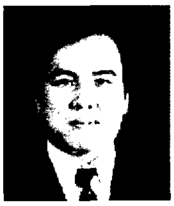

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