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A Dynamic Performance Study of an HVDC System using a Hybrid Simulator

Chan-Ki Kim†, Byeong-Mo Yang* Hahk-Sung Lee**

†Korea Electric Power Research Institute(KEPRI), Power System Research Laboratory,
Munji Dong 106-16, Yuseong-Gu, Daejon 305-380, Korea
**Hyosung Industrial

ABSTRACT

This paper deals with the development of a new type of simulator for the study of the dynamic performance of an HVDC scheme. The new simulator uses a digital model of the power equipment and an analogue model of the existing HVDC controller. This simulator is used to study the dynamic performance of the Cheju - Haenam HVDC system and to verify the control characteristics of the HVDC system. The paper discusses the simulator development requirements and criteria. The paper provides guidelines for the development of the simulator and presents the results of the simulation studies.

Keywords: HVDC, Hybrid Simulator

1. Introduction

Fast acting power equipment like HVDC, SVC and FACTS can be used to significantly improve the performance of an AC network. However, to ensure that such equipment is used to the maximum advantage of the ac network, an accurate simulator is required by planning engineers for system analysis and also for the training of system operators. For example, if an HVDC system is designed and operated with the sole objective of transmitting power between ac networks, it may under some conditions be detrimental to the operation and stability of the ac network. However, by taking full advantage of the characteristics of the HVDC system, and applying these appropriately, an HVDC system can enhance the operation and stability of the ac networks.

The CHEJU-HAENAN 300MW HVDC system was completed in Korea in 1998. The HVDC system transmits relatively cheap electric power by submarine DC cables from the Haenam substation on mainland Korea to the Cheju substation on Cheju Island, a distance of 100km. The power transmitted on the 12-pulse bipolar HVDC system is normally a maximum of 150 MW, which corresponds to 60% of the total load demand on Cheju Island. The control of the operation of the inverter at Cheju is normally current control (main control), with mean γ control used as the secondary control. DC voltage control is used as the main control at the rectifier at Haenam, with current control as the secondary control. For most other HVDC schemes in the world the main control for the rectifier is dc current control with the

Manuscript received June 13, 2005; revised August 9, 2005
†Corresponding Author: ckkim@kepri.re.kr, KEPRI
Tel: +82-42-865-5871, Fax: +82-42-865-5844
*Korea Electric Power Research Institute(KEPRI)
**Hyosung Industrial

inverter in dc voltage control. The unusual arrangement of the controls for the Cheju-Haenam HVDC scheme was developed to enable the scheme to operate as the sole power supply to Cheju, without the use of telecommunication [7]. Reactive power compensation for the Cheju side is provided by an ac harmonic filter and shunt capacitor banks in steady state while synchronous compensators provide dynamic reactive power compensation at the inverter terminal.

At present the power consumption on Cheju is increasing at 7% per year. To meet the increasing demand the construction of an additional HVDC system is planned, as well as the addition of renewable energy of about 100MW to the Cheju AC network.

The main objective of this paper is to describe the approach taken to develop an accurate simulator of the Cheju-Haenam HVDC system that can be used for detailed system analysis. The simulator will be used to simulate several HVDC faults and to study the HVDC modification. The simulator objective is to capture the system response for frequencies from DC to several kilo Hertz. Since we depended on the exact instantaneous wave-shapes for our analysis, we needed to use an RTDS (Real Time Digital Simulator) with the most detailed representation of electrical components and the HVDC valves.

2. The Simulator Approach

The approach taken usually depends on the simulation tool used and how the model is going to be used.

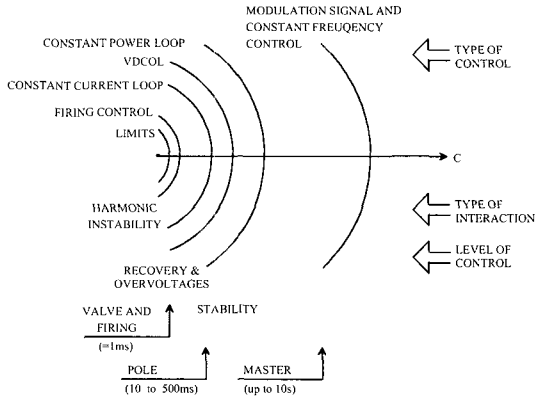


Fig. 1 Relation between simulation time and HVDC control level and interactions

The actual HVDC controls for the existing HVDC scheme are partly digital and partly analog (OpAmps, Transistors, Resistors and Capacitors).

At the outset, it was decided that the controls are going to be modeled exactly as in the actual system to represent its analog and digital behavior. The important factors in the simulator development are as follows:

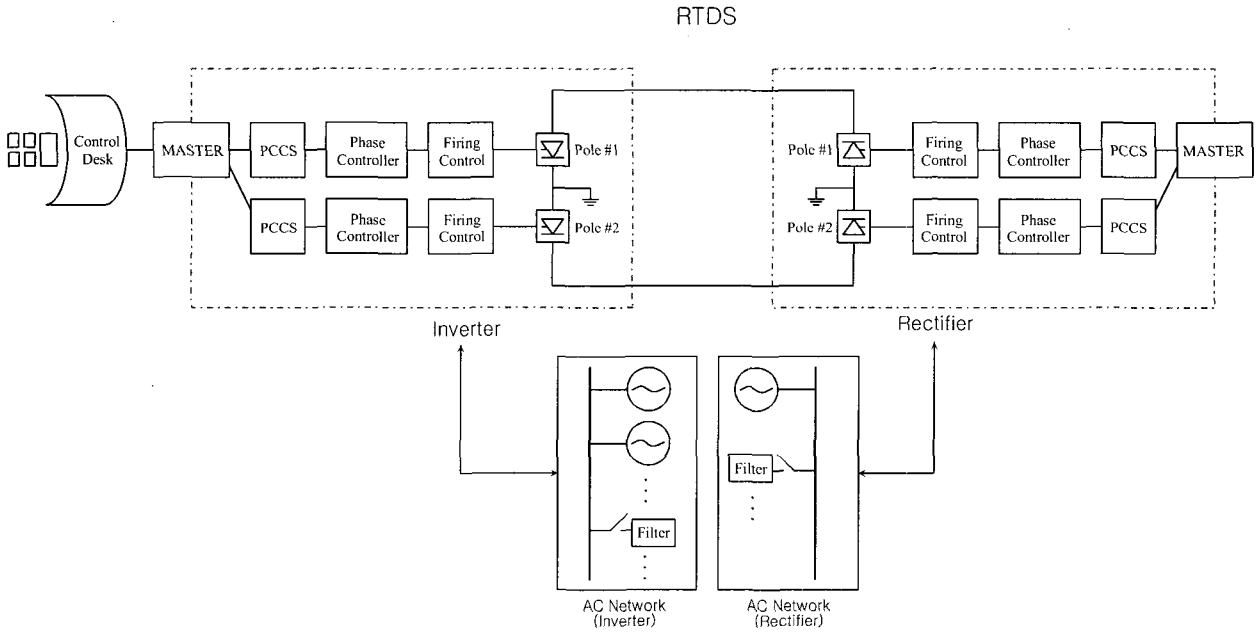
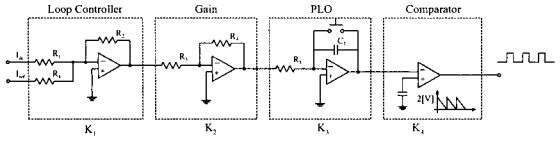
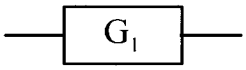


Fig. 2 HVDC simulator configuration



(a)

(b)



$$G_1 = K1 \cdot K2 \cdot K3 \cdot K4$$

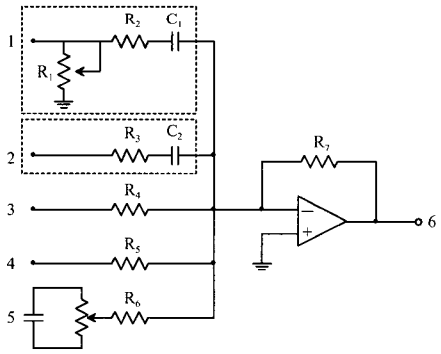
(c)

Where, K_1: *Loop Control gain* $1 = \left(-\frac{R_2}{R_1}\right)$

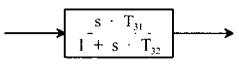
K_2: *Loop Control gain* $2 = \left(-\frac{R_4}{R_3}\right)$,

K_3: *The gain of PLO* $= \frac{1}{(12 \times f_o(60Hz) \times R_5 \times C_1)}$

K_4: *Comparator level* $= \frac{1}{2[V]}$



(d)



(e)

Where, $*Input \mid 1: V_{dc}, 3: \gamma_{ord}, 4: \gamma_{response}$

$*Output \mid 6: \gamma_{output}$

$$Output = -\frac{R_7}{R_5} \cdot \gamma_{response} + -\frac{R_7}{R_4} \cdot \gamma_{ord}$$

$$+(-A \cdot R_7)/(R_2 + \frac{1}{s \cdot C_1}) \cdot V_{dc}$$

$T_{31} = (A \cdot R_7) \cdot C_1$, $T_{32} = R_2 \cdot C_1$

$A = M_p 9 \cdot R_{35} / (R_{33} \cdot (-7.5 - M_p 9) + M_p 9 \cdot R_{35})$

= Setting gain due to variable resistance

Fig. 3 Reduced model of an HVDC controller

- Real time or non-real time
- Simulation time
- Simulation scope(Overvoltage/Harmonic stability)
- Software implementation or Hardware implementation
- Accuracy

Among the above factors, the simulation scope and the simulation time were determined by the relation between simulation time and the HVDC control level as shown in figure 1. In the HVDC control system, VBE (Valve Based Electronics) generates the pulse train by which the thyristors get gate signals. VBE does not have crucial effects on the transient performance of the HVDC system; hence, it is not represented in detail.

The selection of hardware implementation or software implementation was determined from the viewpoint of cost. Therefore, in this paper the AC network including generators, the HVDC valves, converter transformers and ac harmonic filters were implemented using an RTDS (Real Time Digital Simulator) and the HVDC controller was implemented using an actual system as shown in figure 2. The implementation of the HVDC controller was done in two ways. First, the performance of the HVDC system using the reduced control model as shown in figure 3 was analyzed mathematically. Using this method, we can estimate the system stability and the harmonic stability. Secondly, the signal waveform of the actual controller was measured by using an oscilloscope as shown in figure 4. The measured waveforms were compared with the waveform of the implemented simulator controller.

Where, 1. 3-phase voltage, 2. Firing pulse, 3. Alpha error, 4. Control reference, 5.Voltage controller error, 6.Current error, 7.Alpha max controller error, 8. Alpha response, 9. Gamma response

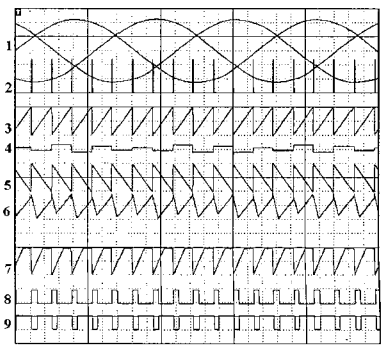


Fig. 4 Actual HVDC controller waveforms

3. Control Characteristics

• Master control

The master control is the uppermost control in the HVDC system, and it determines the filter switching mode, the power transfer direction, and the control mode. This control doesn't affect the transient performance of the HVDC system since the time constant of the master control is only a few seconds.

• Pole Control

Figure 5 shows the block diagram of the pole control. Pole control receives the signal of the control mode and power transfer direction from the master control, which sends the corresponding control signal to the phase control. Detailed descriptions of each part are as follows.

• Frequency Control

The frequency of the Cheju power system is controlled by regulating the power delivered from the dc line when the control mode is in frequency mode. It corresponds to the governor free operation of the turbine-generator. This control is based on the speed-droop characteristic of the HVDC system, and can be expressed like equation (1).

$$F_{order}(Hz) = F_{demand}(Hz) - \left[Pdc(MW) * Slope(\%) * \frac{0.6}{150} \left(\frac{Hz}{MW} \right) \right] \quad (1)$$

Where, F_{order} (Hz) is the frequency output value, F_{demand} (Hz) is the frequency order value, *Pdc* (MW) is the DC power, and *slope* (%droop) is the speed-droop characteristic of the system.

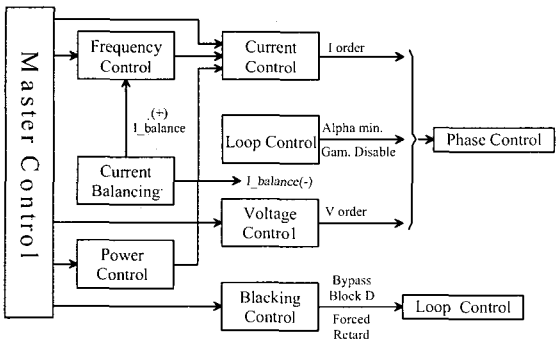


Fig. 5 Block diagram of the pole control HVDC simulator configuration

• Power Control

The HVDC line delivers a constant scheduled value of power to the Cheju system when this mode is selected. This control operation can be described as in equation. (2).

$$I_{order} = \frac{P_{order}}{V_{dc}} \quad (2)$$

Where I_{order} is the current order from the power control, P_{order} is the DC power order, and V_{dc} is the DC voltage value.

• Current Control

Current control generates the current order value, and is adopted as the main control on the Cheju side (Inverter). Input of the current control depends on the HVDC operation mode: For example, the current order is generated from current control when the HVDC system is in current control mode, and the output value of pole control or frequency control becomes the input for current control.

• Voltage Control

Voltage control acts as the main control on the Haenam side (Rectifier), while it is used as an overvoltage limiter on the Cheju side.

• Current Balancing

Current balancing is the function to minimize the current on the neutral line when the HVDC system is in bi-pole operation.

• Blocking Control

Blocking control issues control signals such as Block D, Bypass and forced retard signals when system failures occur.

• Auxiliary Loop Control - Pole Control

Loop control of the pole control blocks the HVDC system with the blocking control. In the loop control the α-min value is regulated to attain the fast restoration rate, and the control prevents the failure from being propagated.

A. Phase Control

Figure 6 shows the block diagram of phase control in the HVDC system.

• AC Voltage Measurement

This card generates a Y-Δ voltage signal with a 30 degree angle difference from the 3 phase signal of VT since measurements of the phase angle of the AC input voltage are required for the phase control system.

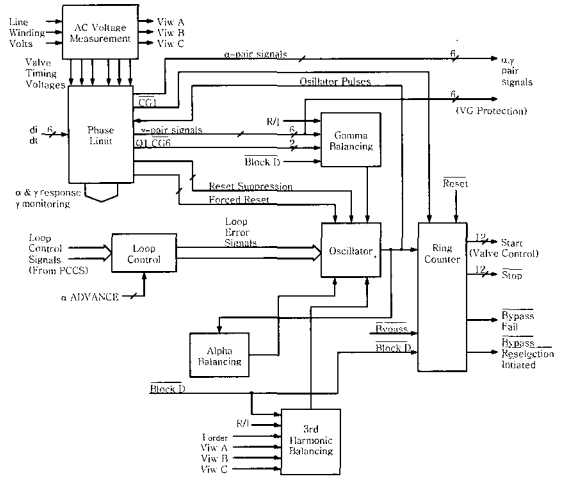


Fig. 6 Block diagram of the phase control

• Phase Limit

The phase limit card has the forced firing circuit which forces the firing angle to be between 2 and 182 degrees, and calculates the values of α and ɣ. The permission logic of the oscillator receives a signal from the phase limit.

• Gamma Balance

The values of the three-phase voltage are unbalanced in the strict sense although they are generally assumed to be balanced. Hence, the values of α and ɣ don't coincide in steady state. Instability of ɣ control is caused by ɣ gain ($\sin\alpha/\sin\gamma$); a trend in which $\partial\alpha/\partial\gamma$ becomes positive results in a repeated commutation failure. This problem can be resolved by igniting 12 valves at the same extinction angle using the closed loop.

• Alpha Balance

α balance is similar to ɣ balance, and it is used at the rectifier. Unbalance in the AC system changes the α value, and it enlarges the second harmonic of the AC system. The alpha balancing controls the gating time of the 2 valves at each phase.

• Loop Control

Loop control in phase control generates an error signal by comparing the order value with the measured value.

• Oscillator

The oscillator generates gate pulses at an equal interval.

The pulse depends on the maximum value of the error from the loop control. The Max./Min. selector or Permission Logic is built using AND/OR logic. The permission logic in Figure 8 is the Max/Min selector which determines the HVDC system mode. The oscillator has the forced reset signal from the phase limit and the reset suppression signal, and both signals related with the permission logic ensure that the gate signals are in the range of 2 – 180 degrees.

• Ring Counter

The ring counter converts the pulse from the oscillator into the gating signal, and it has a Block D command and a bypass command.

4. The System Performance

Figure 6 shows the control characteristics of the HVDC

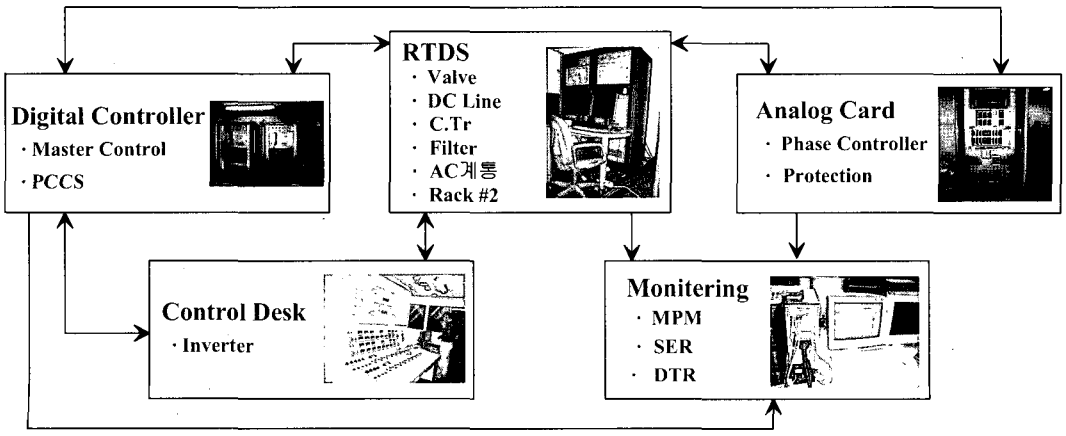


Fig. 7 HVDC simulator

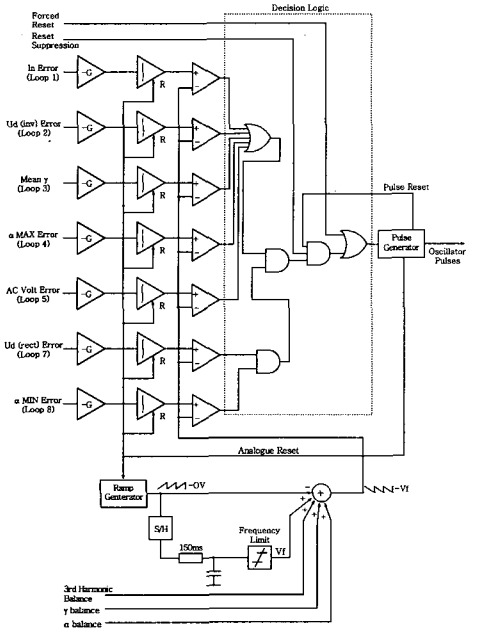


Fig. 8 Oscillator

Figure 6 shows the control characteristics of the HVDC system between Cheju and Haenam. ABCC'EF represents constant voltage control which is performed when the current is less than the rated current (1.0p.u). The control mode is changed to current mode when the voltage at the inverter drops or the current is over 1.3p.u. The line from B to C has the same slope as the YY'Y" line in order to ensure one operating point when the voltage of the inverter drops. This slope is determined by the % impedance of the transformer. The curve C'EF is known as the VDCL (Voltage Dependant Current Limit), and it limits the current according to the voltage drop due to the failure in the AC system. The curve Y"Y'YXW0 represents the characteristic of the inverter. The curve YX corresponds to current control, and the curve YY'Y" to average γ control. The curve XW0 is the VDCL, and the slope is determined by the AC system condition.

The slope of the curve XW0 is different from the curve CEF in the convertor, and it helps keep the system stable when the SCR of an AC system is small. The selection of current control or voltage control is performed at the Maximum Value Selector by comparing the output control values from both controls. In the inverter there is a current control loop and an average γ control loop, and the former is used in steady state and the latter is used in transient state. This selection is performed in the Minimum Value Selector, and the smaller value is chosen by comparing the control output of both controls.

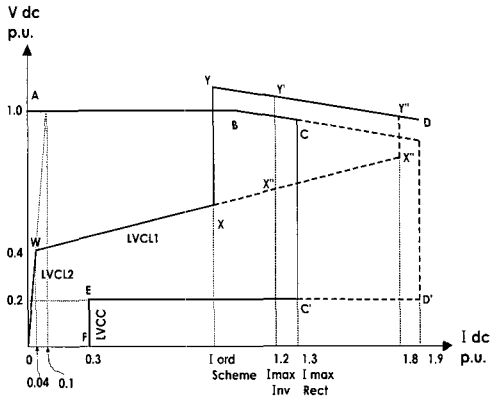


Fig. 9 Cheju-Haenam HVDC characteristics

5. Hvdc System Analysis

B. The Need for Simulation

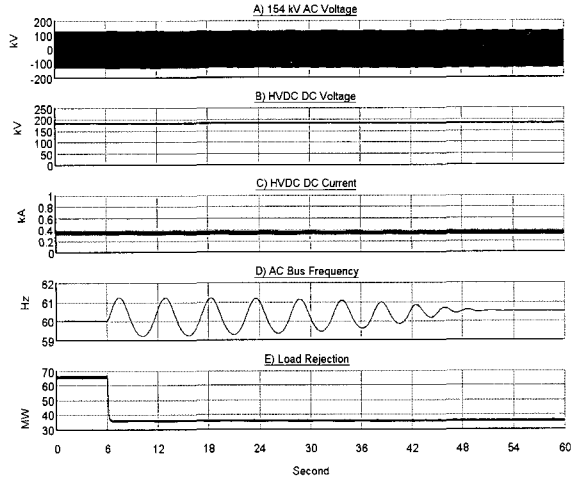
Every simulation requires system modeling, and the complexity of the model depends on the simulation purpose. In this paper, the purpose of the simulation is mainly the analysis of the transient performance of the system, so 50μs is used for the sampling time. RTDS, which is used in this paper, is a popular program to analyze transient and dynamic characteristic in power systems.

C. Simulation Results

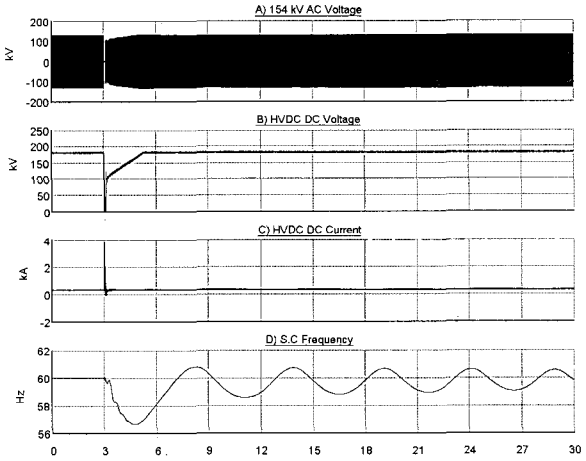
A simulation was performed for the condition where the rated voltage of a pole is 180 kV and the rated current is 416A. Saturation effects of transformers, harmonic characteristics of AC systems, and current unbalance between poles are not considered in this simulation.

The simulation scenarios are to analyze the performance of the power modes in the HVDC systems. The AC network condition of this scenario is the same as below

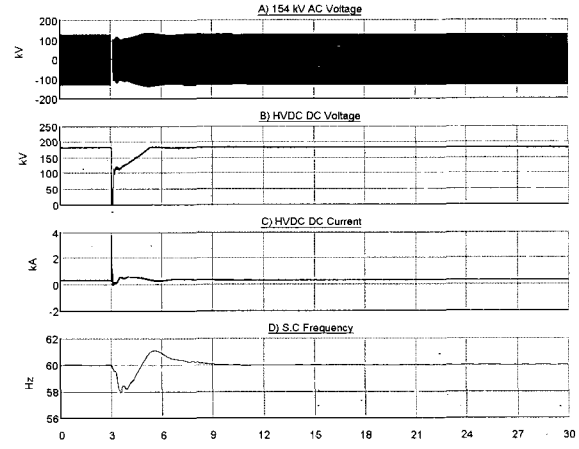
- AC network total load: 300MW,
- HVDC system power transfer: 150MW
- Local AC generator: 75 x 2
- Synchronous Compensator (S.C): 55MVA x 2
- Frequency source of HVDC is from S.C



(a) Load Rejection (power mode)

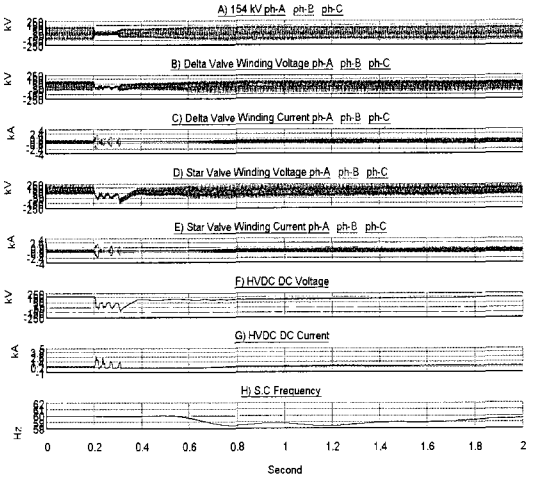


(b) 3-phase fault (power mode)

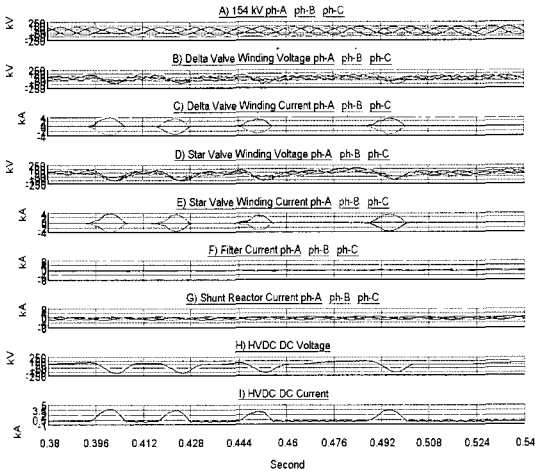


(C) 3-phase fault (frequency mode)

Fig. 10 Power mode operation and frequency mode operation of HVDC system



(a)



(c) Enlargement of (a)

Fig. 11 Remote fault of HVDC system (Commutation Failure)

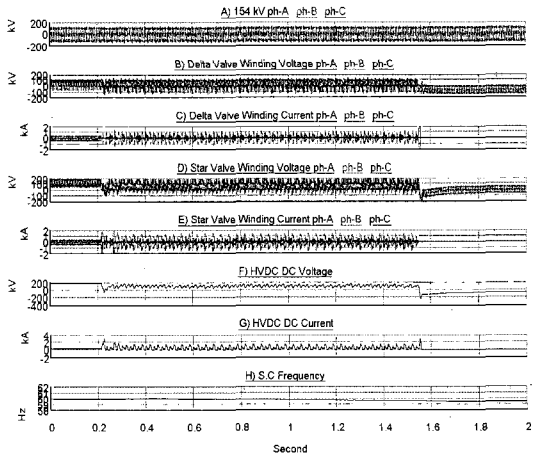
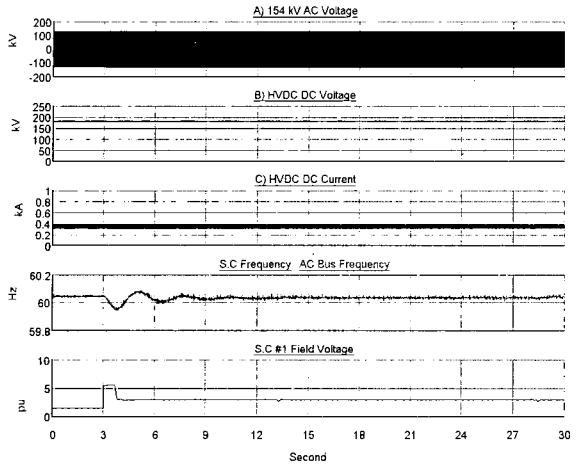
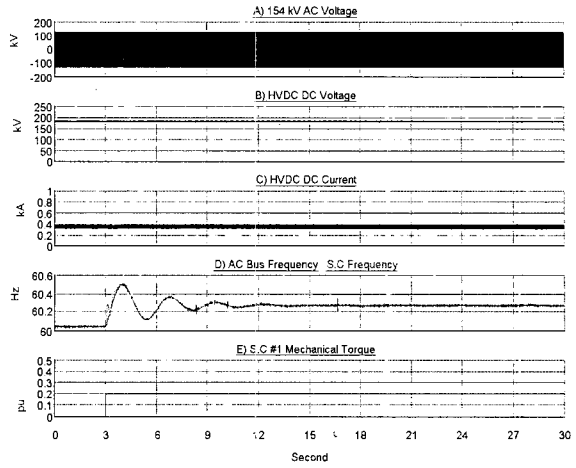


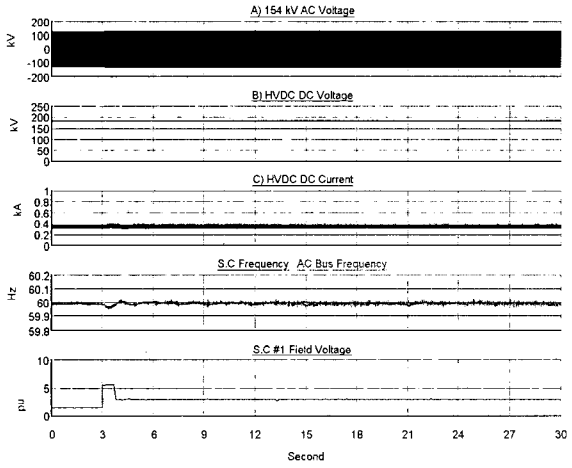
Fig. 12 1-valve fault of HVDC system



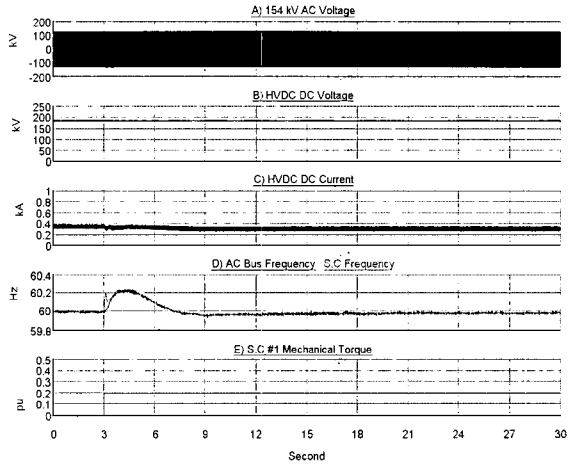
(a) Synchronous Compensator Shaft fed



(c) Synchronous Compensator Shaft fed



(b) AC voltage Bus fed



(d) AC voltage Bus fed

Fig. 13 HVDC operating characteristics according to a change in frequency source

The reason for this scenario is that the HVDC had black start capability originally, so the frequency source of HVDC comes from a synchronous compensator. But because of the increasing demand for power, an additional generator was constructed on Cheju Island. Therefore, the interactions between the HVDC and the local generator were simulated. Figure 10 shows the power operation, a) is the load rejection condition and b) is the condition of the 3-phase fault.

From figure 10, power mode generates the oscillation, otherwise frequency mode controls the AC network frequency and generator oscillation. Figure 11 shows the system response of frequency mode, the frequency measurement point of the HVDC controller is the shaft of the synchronous compensator; (b) is on the AC network bus. Fig 11 shows the commutation failure due to a remote fault. Figure 12 shows the HVDC system characteristics according to a 1-valve fault of the HVDC system. Figures 11 and 12 were compared with the actual fault cases and used to estimate the simulator accuracy. Figure 13 shows the comparison between the frequency sources that are on the AC bus and the Synchronous compensator shaft.

Before the simulation, SSR (Sub-Synchronous Resonance) due to the synchronous compensator was estimated. However, figure 13 show that the HVDC frequency controller can control the oscillation of the

synchronous compensator according to the changing of AVR reference or governor reference. Additionally, the synchronous compensator stated in this paper can do the governor control because the synchronous compensator has a turbine to do a black-start. From fig.13, the waveforms show that changing the frequency measurement point doesn't affect the transient performance of the HVDC system.

6. Conclusions

This paper deals with the development of an HVDC simulator with RTDS for the Cheju-Hanam HVDC system for transient analysis and operator training. Field record data were used to enhance the accuracy of the model. This simulator is valuable for analyzing characteristics of the HVDC system between Cheju and Haenam, and will be used to study various cases which are related to the HVDC system.

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Appendix

The Data of Cheju-Haenam HVDC

A1.Cable

Length of cable	101Km
Cu area	800mm²
Resistance	0.0221 Ω/km @20°C 0.0247 Ω/km @20°C
Inductance	0.1516mH/km @60Hz
Capacitance	0.53 μF/km
Range of cable resistance	2.23 – 2.25 ohms
Total Inductance	15.31mH @60Hz
Total Capacitance	53.53 μF

A2. Electrode Line/Electrode

Length of cable	15km(one side)
Resistance	0.06 Ohm/km
The total neutral resistance	0.7 Ohms
Total capacitance	0.21 μF
Total inductance (Soil Resistor = 200 Ω.m) (Soil Resistor = 500 Ω.m)	 26mH @60Hz 27mH @60Hz

A3. Direct Voltage, Current and Power Rating

HVDC voltage range	180 to 189kV dc
Nominal power transfer	300MW
DC current	840 A

2.4 Alpha and Gamma Limits

The minimum gamma angle	18°
The minimum alpha angle	2°

Chan-Ki Kim(M'1996) received his B.S., M.S, Ph.D. degrees in Electrical Engineering from Chung-Ang University, Korea in 1991, 1993, 1996 respectively. Currently he is P/L for HVDC at KEPRI that is the R & D center of KEPCO, fellow/editor of KIEE and a member of IEEE. His research interests are power system operation and control, HVDC and Power. He has published 150 papers in the electric field including KIEE and IEEE and submitted 20 patents and programs. He has received the Technical Award from the Ministry of Science & Technology of the Korean Government.

Byeong-Mo Yang was born in Chun-Buk, Korea, on June 09, 1969. He received his B.S. and M.S. degrees in electrical engineering from Yonsei University. Since 1997, he has worked in KEPRI. He is experienced with HVDC as well as power system grounds and simulations. His current research interests are power system simulation and HVDC.

Hahk Sung Lee was born in Korea in 1957. He received his B.S. and M.S. degrees from Seoul National University, Seoul, Korea in 1981 and 1983, respectively, and the Ph. D. degree from the University of Southern California in 1992. In 1992, he rejoined to R&D Institute of Hyosung, where he is currently the head of the Research & Development Center, as a senior vice president of Hyosung Corporation. His main research interests include FACTS application in large power grid and power automation systems, especially substation automation systems.