

# CDBA-Based Synthetic Floating Inductance Circuits with Electronic Tuning Properties

Ali Ümit Keskin and Erhan Hancioglu

**ABSTRACT**—This paper introduces two different current differencing buffered amplifier (CDBA)-based synthetic floating inductance circuits. Both configurations use a grounded capacitor. They are fully integrable and provide the advantages of electronic tuning.

**Keywords**—Synthetic floating inductance, CDBA, MOS resistive circuits, active filters.

## I. Introduction

Numerous synthetic floating inductance (FI) circuits using different active elements such as op-amps [1], current conveyors [2], [3], four terminal floating nullors [4], balanced output transconductors [5], translinear conveyors [6] and operational mirrored amplifiers [7], operational transconductance amplifiers [8], [9], and current feedback amplifiers [10] are reported in the technical literature. FI circuits with grounded capacitors are preferred in integrated circuit implementation. In some of the previously reported current mode designs of this kind, different types of active elements have been employed within the same FI circuit. For example, some [11], [12] require both negative and positive types of second-generation current conveyors. Another FI proposal [13] requires four current conveyors, one first-generation (CCI) and three second-generation (CCII) types, while current-controlled second-generation current conveyors (CCCII) together with conventional op-amps need to be implemented in the same circuit proposed in some of the more recent papers [14], [15]. However, from the point of ease of integrated circuit fabrication processes, it is advantageous to

realize an FI circuit by employing only one type and a minimum number of active elements.

Recently, a new active current mode element, called a current differencing buffered amplifier (CDBA), has received much attention in the electronics community [16]. However, to the authors' best knowledge, a floating inductance realization using this new active element has not been reported.

In this paper, two lossless CDBA-based FI circuits are presented. The circuits provide the advantages of an electronic tuning capability and full integrability. A circuit simulation example is also given to illustrate the feasibility of using the proposed synthetic FI configurations.

## II. Circuit Description

The circuit symbol of the CDBA is shown in Fig. 1. Its defining equations are

$$V_p = V_n = 0, \quad I_z = I_p - I_n, \quad \text{and} \quad V_w = V_z. \quad (1)$$

Here, a current through the z-terminal follows the difference of the currents through the p-terminal and n-terminal. Input terminals p and n are internally grounded [16].

On the other hand, in the so-called MOS resistive circuit (MRC) shown in Fig.2, both the even and odd nonlinearities are cancelled by subtraction of the drain-source currents of transistors operating in their triode region [17], [18]. Because the transistors have equal drain and source voltages,

$$I_a - I_b = g(V_i - V_2), \quad (2)$$

where the conductance term  $g$  is

$$g = K(V_a - V_b), \quad (3)$$

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where

$$K = \mu C_{ox} \frac{w}{l}, \quad (4)$$

and  $\mu$ ,  $C_{ox}$ ,  $w$ , and  $l$  stand for carrier effective mobility, gate oxide capacitance per unit area, width, and length of the channel, respectively.

In order to subtract the current of MOSFETs operating in the triode region, one can use the input terminals of the CDBA since both terminals are at virtual ground potential. Note that the value of the conductance term can be positive, zero, or negative, depending upon the choice of the gate control voltages  $V_a$  and  $V_b$ .

Figure 3 shows the first proposed CDBA-based circuit for an electronically tunable floating inductor.

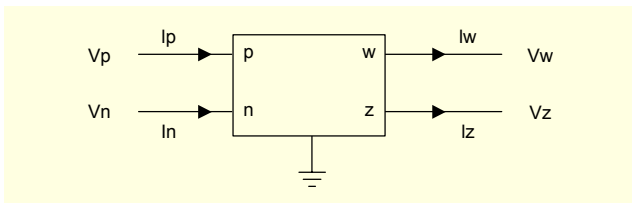


Fig. 1. Symbol for the CDBA.

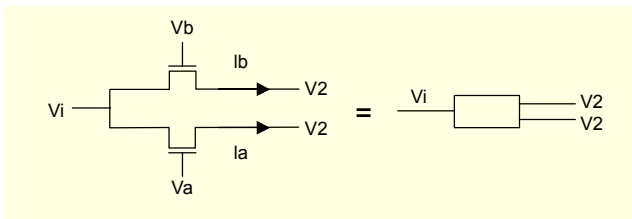


Fig. 2. MOSFET resistive circuit nonlinearity cancellation. Gate voltages  $V_a$  and  $V_b$  are not indicated on the equivalent schematic.

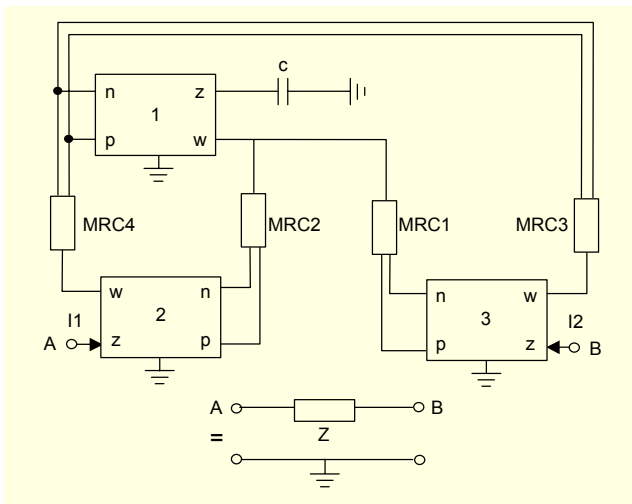


Fig. 3. Electronically tunable, floating inductor using three CDBAs,  $z=j\omega L$  where  $L$  is given in (7). Note that, if the capacitor is replaced by an external resistor  $R$ , the circuit acts as a resistance multiplier,  $Z=kR$ ,  $k>0$ .

In order to simplify the analysis, let the design parameters of MRCs be selected so that  $g_1$  and  $g_2$  represent the gyration conductances for  $MRC2 \equiv MRC4$  and  $MRC3 \equiv MRC1$ , respectively. Using (1) and (3), and by routine circuit computation, the short circuit admittance equation can be found as

$$[Y] = Z_5 g_1 g_2 \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}. \quad (5)$$

In (5), if  $Z_5 = I/(sC)$ , and for further simplification  $g_1 = g_2 = g$ , the admittance seen between the  $z$  terminals of CDBA2 and CDBA3 becomes

$$Y = \frac{g^2}{sC}. \quad (6)$$

Equation (6) indicates that the circuit simulates an inductance,

$$L = \frac{C}{(\mu C_{ox} (V_a - V_b))^2 \left(\frac{w}{l}\right)^2}, \quad (7)$$

which can be tuned electronically by adjusting the gate voltages of the respective MOSFETs in MRCs.

### III. Alternative CDBA -Based Tunable FI Circuit

Figure 4 shows another CDBA-based tunable FI configuration. Here, CDBA1 and CDBA2 along with MRC1 and MRC2 constitute a gyrator circuit [19]. Therefore, a floating inductor can be synthesized easily by cascading two identical gyrators and placing a grounded capacitor  $C$  at their connection terminal. This will yield a floating inductor whose inductance is also described by (7) and can be tuned

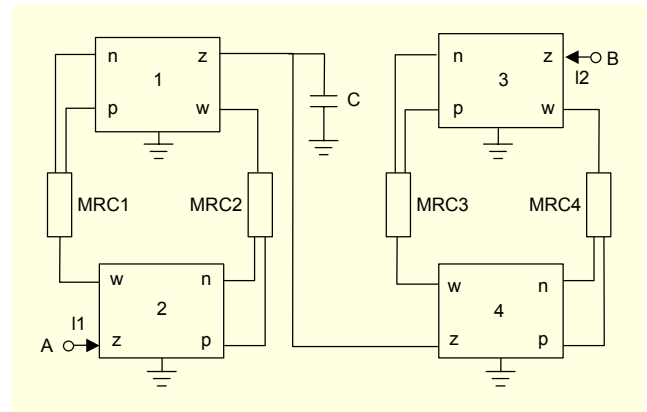


Fig. 4. Alternative tunable, floating inductor using four CDBAs.

electronically by adjusting the gate voltages of the respective MOSFETs in MRCs. However, this configuration requires four CDBAs.

#### IV. Simulation Results

A possible CMOS realization of a CDBA element is given in Fig.5, where a differential current stage is followed by a voltage buffer [20]. The FI configurations presented in this study are simulated using this CMOS-based CDBA circuit. For this purpose, the current in a series resonance circuit is investigated as shown in Fig. 6, and  $0.5\mu$  MIETEC real transistor model parameters are implemented for all MOSFETs in the circuit. Transistor aspect ratios are indicated in Table 1. MRCs are chosen to be n-channel MOS pairs with equal aspect ratios. Figures 7 and 8 demonstrate the results of series resonator circuit simulations using a three-CDBA-based FI configuration.

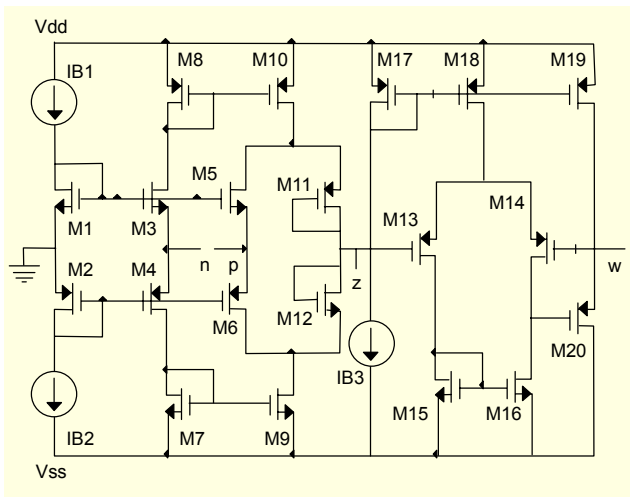


Fig. 5. The CMOS implementation of CDBA used in simulation studies. Bias currents of current differencing input section are  $I_{B1} = I_{B2} = 20 \mu A$ , while  $I_{B3} = 25 \mu A$ .  $V_{dd} = -V_{ss} = 2,5 V$ .

Table 1. Transistor aspect ratios used in circuit simulations.

Transistor	$w (\mu m) / l (\mu m)$
M1 - M10	150 / 1
M11, M12	4 / 2
M13, M14, M17, M18	5 / 1
M15, M16	100 / 1
M19	20 / 1
M20	200 / 1
MRC	5 / 10

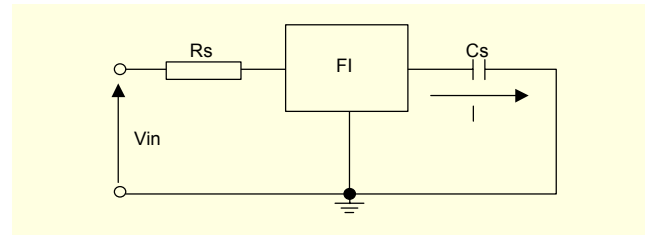


Fig. 6. Series resonance circuit using CDBA-based floating inductance.

#### V. Discussion and Conclusion

Although a cascaded gyrator-based FI configuration requires four CDBAs, the other FI circuit proposed in this study contains three CDBAs, saving one active element. In fact, FI circuits employing two active components can also be realized [2]; however, such circuits do not have grounded capacitors. In that sense, the proposed three CDBA-based FI circuit is optimal. Note also that the same circuit topology can be used as a tunable linear floating resistance scaling circuit by replacing the capacitor in Fig. 3 with an external resistor. Such circuits are very useful in integrated circuit design when large valued resistances cannot be integrated due to their excessive occupation of the silicon chip area and when the simple triode operation of an individual MOSFET as a resistor cannot provide sufficient linearity.

In this paper, CDBA-based FI simulator circuits are proposed. These circuits are fully integrable and have voltage tuning properties. Moreover, they can be easily converted into

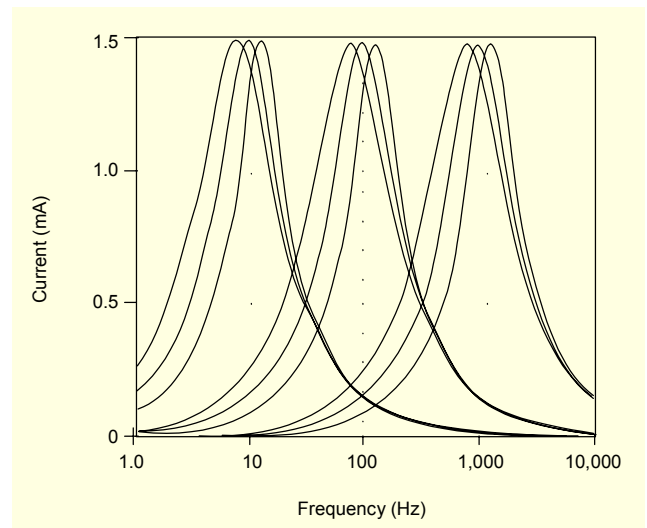


Fig. 7. The series resonance circuit responses. Left curves block:  $R_s = 10 \Omega$ ,  $C = 1 nF$ ,  $C_s = 25 \mu F$ , middle curves block:  $R_s = 10 \Omega$ ,  $C = 0.1 nF$ ,  $C_s = 2.5 \mu F$ , right curves block:  $R_s = 10 \Omega$ ,  $C = 0.01 nF$ ,  $C_s = 0.25 \mu F$ . Fine tuning is performed for all MRCs at  $V_a = 2.5 V$  when  $V_b = 3 V$  (leftmost curve of each group),  $V_b = 4 V$  (middle curve of each group), and  $V_b = 5 V$  (rightmost curve of each group of curves).

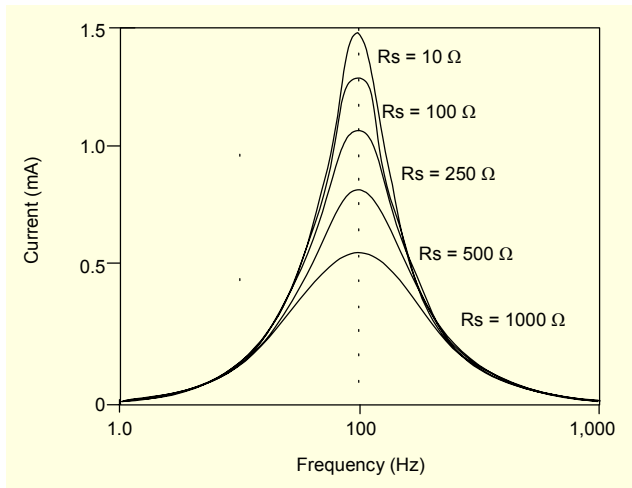


Fig. 8. The series resonance circuit behavior for different series resistor values:  $C = 0.1 \mu\text{F}$  and  $C_s = 2.533 \mu\text{F}$ .

fully integrable and linearly tunable resistance scaling circuits. Their defining equations are presented and circuit simulation results are introduced. The simulation results are in good agreement with theory. The proposed circuits are expected to be useful in analogue signal processing applications.

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