A Novel Grounded Inductor Realization Using a Minimum Number of Active and Passive Components

Erkan Yuce, Shahram Minaei, and Oguzhan Cicekoglu

In this study, we present a new topology for realizing a grounded inductor employing only a single current conveyor, called a negative-type modified inverting second-generation current conveyor (MICCII-), and a minimum number of passive components, two resistors, and one capacitor. The non-ideality effects of the MICCII- on a simulated inductor are investigated. To demonstrate the performance of the presented inductance simulator, we use it to construct a third order Butterworth high-pass filter and a parallel resonant circuit. Simulation results are given to confirm the theoretical analysis.

Keywords: Grounded inductance simulator, current conveyor, high-pass filter.

I. Introduction

Monolithic Si spiral inductors suffer from substrate resistive losses and capacitive couplings. In addition, process tolerances lead to component variations, which cannot easily be tuned in the passive case [1]. Thus active circuits, which simulate the characteristic of a passive inductor, have received considerable attention. This is attributed to their effective use of space, weight, cost, tunability, integrability, and the wide range of applications of such inductors especially when the value of the required inductance is relatively large. The most famous inductance simulator was proposed by Antoniou [2] and utilizes two op-amps and five passive elements to obtain a pure inductance. However, as an active element, a current conveyor (CC) provides many advantages such as greater linearity, wider bandwidth, and better dynamic range compared to the voltage mode counterparts, op-amps [3].

Many CC-based grounded synthetic inductor topologies have been proposed in the literature [4]-[15]. These topologies can be classified based on the number of active and passive elements employed and whether they realize a lossy or lossless kind of inductor. Most of these circuits employ two or more CCs to realize grounded inductance [6]-[8], [10]-[12], and [15]. The proposed topologies in [4], [9], [13], and [14] employ a single CC but they do not realize pure inductance. Although the circuit reported in [5] realizes pure inductance with only one positive type second-generation current conveyor (CCII+), it employs five passive elements.

On the other hand, new types of CCs such as the inverting second-generation current conveyor (ICCII) [16] have been proposed in the literature. Such kinds of current conveyors give a higher degree of freedom to analog designers, with respect to op-amp and CCII solutions, allowing the implementation of

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more functions using less active elements. A circuit with a minimum number of components is expected to simplify the design.

In this paper, we propose a grounded inductance simulator employing a minimum number of active and passive components including one modified inverting second-generation current conveyor (MICCII), two resistors, and one capacitor. The proposed topology ideally provides lossless inductor realization. By taking non-idealities of the MICCII (due to current and voltage gain) into account, several kinds of grounded immitances can be obtained. Finally, using the proposed grounded inductance simulator, a third-order Butterworth high-pass ladder filter and a parallel resonant circuit is constructed. Frequency domain and time domain responses are given to illustrate the performance of the proposed circuit.

II. Proposed Circuit

A symbolic representation of the MICCII is shown in Fig.1. The MICCII can be characterized by the following matrix equation

$$\begin{bmatrix} V_x \\ I_y \\ I_z \end{bmatrix} = \begin{bmatrix} -\beta & 0 & 0 \\ 0 & 0 & 0 \\ 0 & \pm 2\alpha & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}, \quad (1)$$

where α and β represent the non-ideal current and voltage gains of the current conveyor (ideally equal to unity), respectively.

Fig. 1. Symbol of the MICCII-.

Conventionally, the + or - signs of α in (1) denote the positive (MICCII+) and negative (MICCII–) type conveyors.

The proposed grounded inductor is shown in Fig. 2. It uses one MICCII– and three passive elements. To find the input admittance of the circuit, a voltage source V_{in} is connected to the *X*-terminal of the current conveyor of the proposed circuit. For the *Y*, *X* and *Z* terminals of the MICCII–, we can write

$$V_y y_2 = (V_z - V_y) y_3, \quad (2a)$$

$$I_{in} = (V_x - V_z) y_1 + I_x, \quad (2b)$$

and

$$-I_z = (V_z - V_x) y_1 + (V_z - V_y) y_3, \quad (2c)$$

respectively. Using the terminal characteristic equation of the MICCII- given in (1) and (2a) through (2c), we can obtain the following admittance:

$$Y_{in} = \frac{I_{in}}{V_{in}} = \frac{y_1 y_2}{2y_3} + y_1 - \frac{y_2}{2}. \quad (3)$$

If $y_1=G$, $y_2=2G$, and $y_3=sC$ in (3) are chosen, the following impedance is obtained:

$$Z_{in} = \frac{1}{Y_{in}} = sL_{eq} = \frac{sC}{G^2}. \quad (4)$$

Hence,

$$L_{eq} = \frac{C}{G^2}. \quad (5)$$

Thus, a lossless grounded inductor is realized using a minimum number of passive and active components.

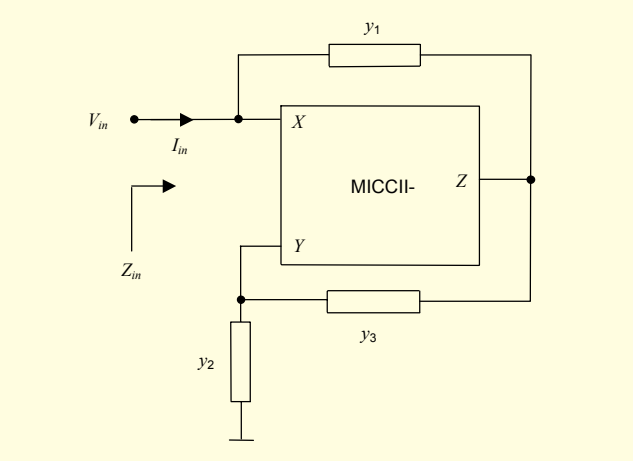

Fig. 2. The proposed inductor realization using MICCII- and passive components.

III. Non-ideality Effects

Taking into account the non-idealities given in (1), the equivalent non-ideal impedance of the circuit is found to be

$$Z_{in} = \frac{2sC\alpha\beta}{2G^2(2\alpha - 1) + sCG(2\alpha + 2\alpha\beta - \beta - 3)}. \quad (6)$$

From (6), the admittance of the circuit is calculated as

$$Y_{in} = \frac{1}{sL_p} + \frac{1}{R_p} = \frac{G^2(2\alpha - 1)}{sC\alpha\beta} + \frac{G(2\alpha + 2\alpha\beta - \beta - 3)}{2\alpha\beta}. \quad (7)$$

Therefore, the circuit simulates an inductor in parallel with a resistor calculated as

$$\left.\begin{aligned} L_p &= \frac{C\alpha\beta}{G^2(2\alpha - 1)} \\ R_p &= \frac{2\alpha\beta}{G(2\alpha + 2\alpha\beta - \beta - 3)} \end{aligned}\right\}. \quad (8)$$

In this case, the quality factor of the inductor is found to be

$$Q_L = \frac{R_p}{\omega L_p} = \frac{2G(2\alpha - 1)}{\omega C(2\alpha + 2\alpha\beta - \beta - 3)}. \quad (9)$$

Note that one can change the α parameter of MICCII- by adjusting bias voltages of the MICCII-, so considering β=1 and α as a variable, five types of inductors can be obtained:

a) For α>1, a lossless inductor in parallel with a positive resistance is obtained.
b) For α = 1, a pure (lossless) inductor as described in section II is realized.
c) For 0.5<α<1, a lossless inductor in parallel with a negative resistor is obtained.
d) For 0<α<0.5, a negative inductor in parallel with a negative resistor is obtained.
e) For α<0, a lossless inductor in parallel with a positive resistor is obtained. In this case, the MICCII- is converted to a MICCII+.

IV. Simulations

The MICCII- is constructed using the schematic implementation in Fig. 3 with DC supply voltages equal to ±2.5 *V* and bias voltages equal to V_B=−0.604 V and V_C=−0.25 V. The simulations are performed using SPICE based on 0.35 μm Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC) CMOS technology tabulated in Table 1. The dimensions of the MOS transistors used in the MICCII- implementation are given in Table 2. To investigate what is the frequency range for the designed MICCII-, AC simulations have been performed. The I_z/I_x and V_x/V_y frequency responses of the MICCII- are depicted in Fig. 4. The α and β values of the MICCII- are found to be 1.02 and 0.967, respectively. The frequency behavior reported in Fig. 4 suggests that for high frequency applications (frequencies of more than 77 MHz), a compensation is needed.

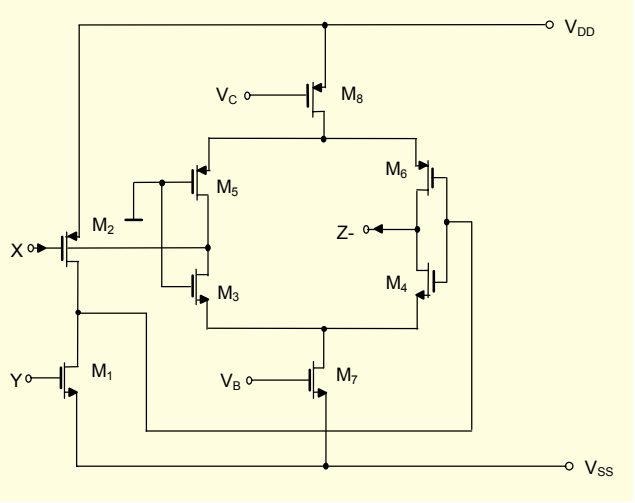

Fig. 3. The internal structure of the MICCII-.

Table 1. Parameters of the CMOS transistors used in SPICE simulations.

0.35μm TSMC CMOS parameters
.MODEL CMOSN NMOS (LEVEL = 3 + TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871 + PHI = 0.7 VTO = 0.5445549 DELTA = 0 + UO = 436.256147 ETA = 0 THETA = 0.1749684 + KN = 2.055786E-4 VMAX = 8.309444E4 KAPPA = 0.2574081 + RSH = 0.0559398 NFS = 1E12 TPG = 1 + XJ = 3E-7 LD = 3.162278E-11 WD = 7.046724E-8 + CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO = 1E-10 + CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504 + CJSW = 3.777852E-10 MJSW = 0.3508721)
.MODEL CMOSP PMOS (LEVEL = 3 + TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.4083894 + PHI = 0.7 VTO = −0.7140674 DELTA = 0 + UO = 212.2319801 ETA = 9.999762E-4 THETA = 0.2020774 + KP = 6.733755E-5 VMAX = 1.181551E5 KAPPA = 1.5 + RSH = 30.0712458 NFS = 1E12 TPG = −1 + XJ = 2E-7 LD = 5.000001E-13 WD = 1.249872E-7 + CGDO = 3.09E-10 CGSO = 3.09E-10 CGBO = 1E-10 + CJ = 1.419508E-3 PB = 0.8152753 MJ = 0.5 + CJSW = 4.813504E-10 MJSW = 0.5)

The proposed circuit shown in Fig. 2 is simulated with the following passive element values: G = 1 mS (y_1=G_1=1 mS and y_2=G_2=2 mS) and C = 50 pF, which results in L_{eq}= 50 μH. The power consumption of the designed grounded inductor is found to be 17.6 mW.

To evaluate the performance of the proposed inductance simulator, we use it in the structure of a third-order Butterworth high-pass ladder filter shown in Fig. 5. The passive elements

Table 2. Dimensions of the CMOS transistors.

PMOS transistors	$W(\mu m)/L(\mu m)$
M_2	28/28
M_5	24.85/0.35
M_6	19.6/0.35
M_8	57.75/1.05
NMOS transistors	$W(\mu m)/L(\mu m)$
M_1	8.75/28
M_3	9.8/0.35
M_4	9.8/0.35
M_7	27.65/1.05

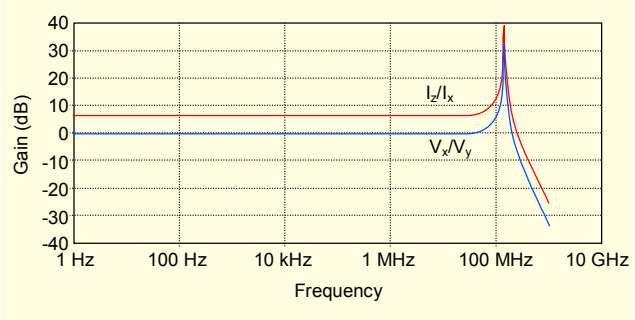

Fig. 4. The simulated frequency responses of the I_z/I_x and V_x/V_y for the MICCII-.

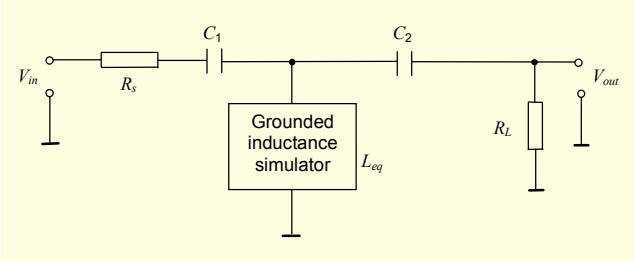

Fig. 5. Third-order high-pass ladder filter prototype.

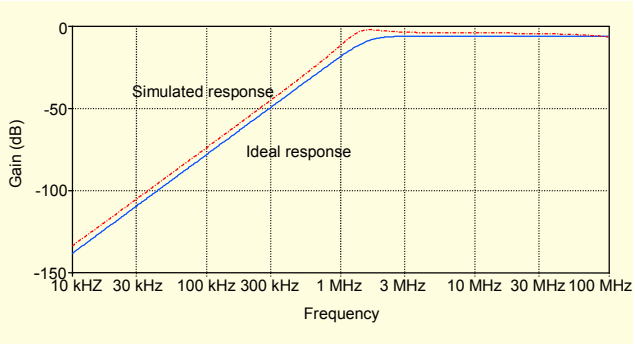

Fig. 6. The ideal and simulated frequency responses of the third-order Butterworth high-pass ladder filter.

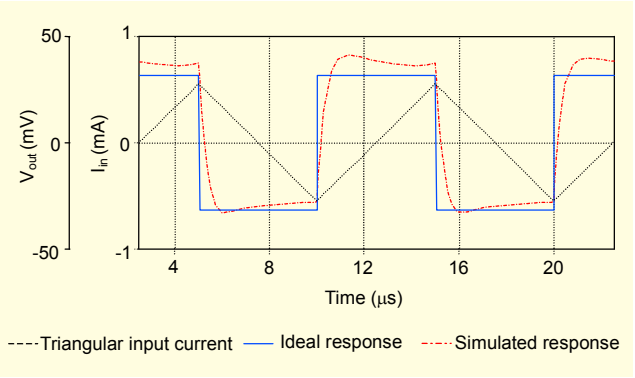

Fig. 7. The ideal and simulated time domain responses of the proposed inductor.

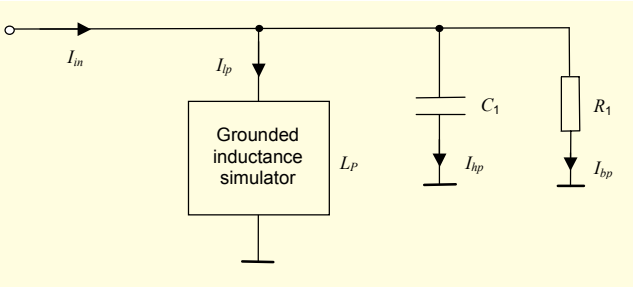

Fig. 8. Parallel resonant circuit.

are selected as $C_1=C_2=0.1$ nF, $R_L=R_s=1$ kΩ, and synthetic inductor L_{eq} = 50 μH, which results in a 3 dB frequency of 1.59 MHz. Both ideal and simulated high-pass ladder filter responses are shown in Fig. 6.

To exhibit the time domain performance of the proposed simulated inductor, a triangular input current with a 0.5 mA peak is applied to the proposed inductor (L_{eq}=175 μH, obtained by G = 1 mS and C = 175 pF) to obtain a square wave output voltage, as shown in Fig. 7.

Also, the proposed grounded inductance is used to construct a parallel resonant circuit as shown in Fig. 8. The element values are selected as $L_{eq}=L_P=100$ μH (G = 1 mS and C = 100 pF), C_1=0.1 nF, and R_1=5 kΩ. Ideal and simulated high-pass (I_{hp}) and low-pass (I_{lp}) responses of the parallel resonant circuit are given in Fig. 9. Moreover, both ideal and simulated band-pass (I_{bp}) responses are depicted in Fig. 10. From Fig. 10, we can see that a gain error exists at the resonance frequency, which is due to the parallel resistance (R_p) of the simulated inductance. Considering α=1.02 and β=0.967 for the designed MICCII-, from (8) and (9), one can calculate the simulated inductance and its parallel resistance as L_p= 94.8 μH and R_p= 43.18 kΩ, respectively. Therefore, the quality factor of the simulated inductance at a frequency of 1.59 MHz is found to be Q_L=45.5.

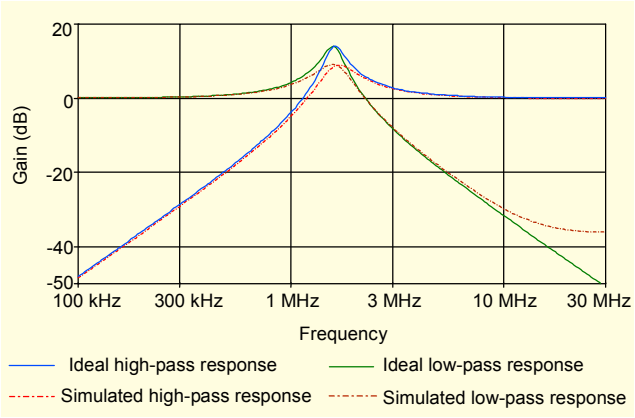

Fig. 9. Ideal and simulated high-pass and low-pass responses of the circuit in Fig. 8.

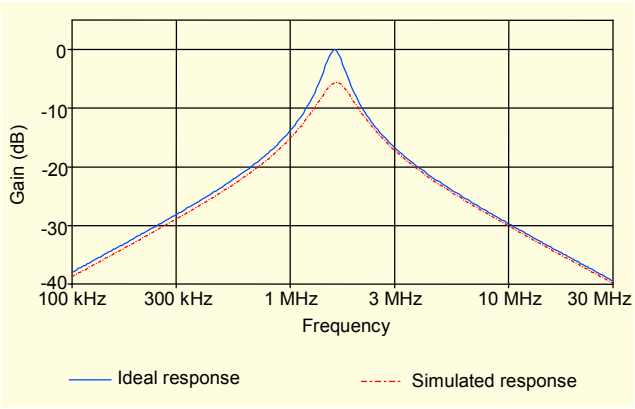

Fig. 10. Ideal and simulated band-pass responses of the circuit shown in Fig. 8.

From Figs. 6, 7, 9 and 10, we can see that the simulation results agree well with the theory.

V. Conclusion

In this paper, we presented a grounded inductor simulating topology. The proposed topology allows for a design with a minimum number of active and passive components, such as two resistors and one capacitor, and one MICCII-. We also investigated the non-ideality effects of the MICCII- on the proposed inductor. To demonstrate the frequency and time-domain behavior of the proposed inductor, we performed simulations with SPICE using 0.35 μm TSMC CMOS technology. The simulation results verify the theoretical analysis.

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