AC Modeling of the ggNMOS ESD Protection Device

Jin-Young Choi

From AC analysis results utilizing a 2-dimensional device simulator, we extracted an AC-equivalent circuit of a grounded-gate NMOS (ggNMOS) electrostatic discharge (ESD) protection device. The extracted equivalent circuit is utilized to analyze the effects of the parasitics in a ggNMOS protection device on the characteristics of a low noise amplifier (LNA). We have shown that the effects of the parasitics can appear exaggerated for an impedance matching aspect and that the noise contribution of the parasitic resistances cannot be counted if the ggNMOS protection device is modeled by a single capacitor, as in prior publications. We have confirmed that the major changes in the characteristics of an LNA when connecting an NMOS protection device at the input are reduction of the power gain and degradation of the noise performance. We have also shown that the performance degradation worsens as the substrate resistance is reduced, which could not be detected if a single capacitor model is used.

Keywords: ESD, AC modeling, equivalent circuit, ggNMOS, LNA.

Manuscript received Dec. 23, 2004; revised June 3, 2005 .

This work was supported by 2005 Hongik University Research Fund.

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I. Introduction

In recent years, there has been a strong trend to utilize standard CMOS processes for RF IC fabrication in order to benefit from their technological maturity and low cost. However, CMOS chips are more vulnerable to electrostatic discharge (ESD) due to the thin gate oxide used, and therefore protection devices such as NMOS transistors are required at the input pads. A large device size is essential for the devices to reduce the discharge current density and thereby to protect them against thermal-related problems, while providing ESD protection for internal circuits. Using large protection devices adds parasitics to the input nodes, which tend to generate other problems. Leroux and Steyaert claimed that the addition of excessive capacitance can cause serious problems in RF circuits such as low noise amplifiers in the RF receiver stage [1].

To reduce the added parasitics, various techniques have been suggested [1]–[5]. Recently, Choi and others proposed a thyristor-like pnpn device, which is a two-terminal device and can be fabricated in a standard CMOS process, and demonstrated a quantitative reduction in the added capacitance [6]. However, it is difficult to find publications dealing with detailed AC modeling of the parasitics added by ESD protection devices. Some researchers did AC modeling work based on measurements [7], but they have not fully examined the significance of the model. In several publications dealing with the characteristic changes in RF circuits incorporating ESD protection devices [1], [8], and [9], the added parasitics are modeled using a single capacitor to derive important characteristic expressions such as power gain and noise figure. The validity of this modeling, however, has not yet been confirmed.

In this paper, we present AC simulation results of the grounded-gate NMOS (ggNMOS) ESD protection device utilizing a two-dimensional device simulator and extract its AC equivalent circuit. The ggNMOS device is chosen since it has been the most popular protection device in use up to now.

Utilizing the extracted equivalent circuit, we examine the effects of the parasitics of the NMOS protection device on the characteristics of a low noise amplifier (LNA), which is one of the important RF circuits.

In section II, we explain the assumed structure of the ggNMOS ESD protection device, and present the extraction procedure and resulting equivalent circuit extracted from the AC device simulation results. In section III, assuming Bluetooth applications, we introduce an LNA in a 2.4 GHz range, and based on circuit simulations we examine the characteristic changes of the LNA when connecting the protection device on the input node or output node.

II. AC Simulation and Modeling of the ggNMOS Protection Device

Figure 1 shows an example of a human-body model (HBM) ESD protection scheme, where one ggNMOS protection transistor (M_1) is connected between the input node and the ground V_{SS}, and the other (M_2) is connected between V_{DD} and V_{SS} as a clamp device. When a positive ESD voltage is applied to the input pin with the V_{SS} pin grounded, the parasitic npn bipolar transistor in M_1 provides a discharging path and limits the voltage applied to the gates of the internal circuits protecting them against ESD. When a negative ESD voltage is applied to the input pin with the V_{SS} pin grounded, the forward-biased pn (p-sub/n$^+$ drain) diode in M_1 provides a discharging path and limits the voltage. When a positive ESD voltage is applied to the input pin with the V_{DD} pin grounded, the parasitic npn bipolar transistor in M_1 in series with the forward-biased pn diode in M_2 provides the protection. When a negative ESD voltage is applied to the input pin with the V_{DD} pin grounded, the npn bipolar transistor in M_2 in series with the forward-biased pn diode in M_1 provides the protection.

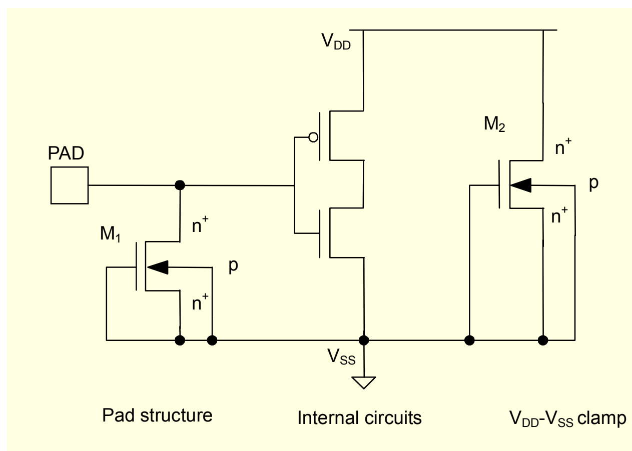

Fig. 1. An example of HBM ESD protection schemes utilizing NMOS protection transistors.

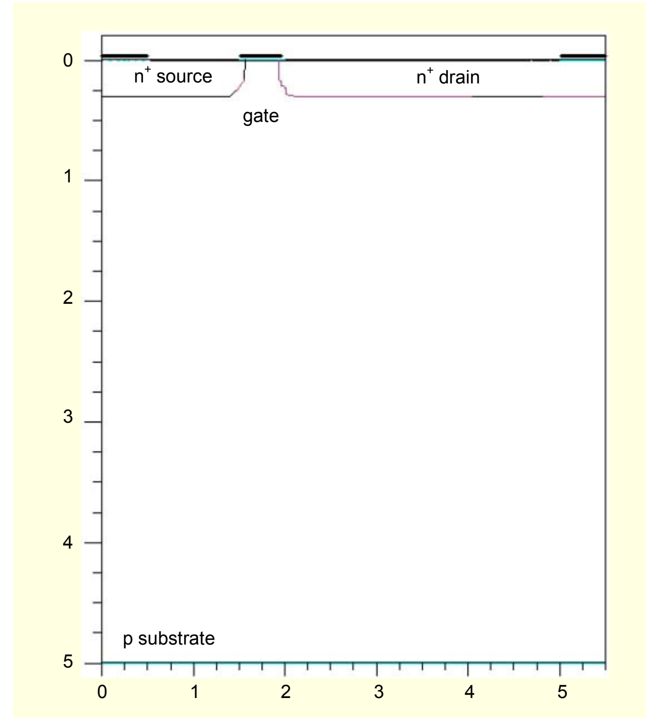

Fig. 2. Cross section of the NMOS protection transistor.

Table 1. Principal structure parameters of the ggNMOS protection transistor.

Parameters	Values
Effective channel length	0.45 μm
Gate oxide thickness	75 Å
Substrate and channel doping	10^{16}cm^{-3}, 10^{17}cm^{-3}
n$^+$ drain depth, length	0.3 μm, 3.38 μm
n$^+$ source depth, length	0.3 μm, 1.38 μm
Gate-drain contact spacing	3 μm
Gate-source contact spacing	1 μm

Therefore, the protection scheme shown in Fig. 1 protects the internal circuits against all possible HBM ESD combinations.

Figure 2 shows the NMOS protection device structure chosen in this work. The units of the two axes are in micrometer (μm). The structure represents a conventional protection device incorporating n$^+$ source and drain ESD implants, which is implied by the relatively deep junctions. Considering the fact that lattice heating during the most critical ESD incident peaks around the region near the gate side of the drain junction, gate-drain contact spacing is chosen to be as large as 3μm, which is still regarded as a minimal spacing [10], in order to alleviate drain-contact melting problems. We note that the added parasitic capacitance with this protection device

attached to an input node is mainly the large n^+-drain/p-sub junction capacitance. Table 1 summarizes the principal structure parameters. The n^+ junctions shown in Fig. 2 are assumed to have a Gaussian doping profile with 10^{20} cm^{-3} of peak concentration.

AC simulation of the device in Fig. 2 was performed using the 2-dimensional device simulator ATLAS [11], which is a commercial version of PISCESIIB. When the NMOS transistor is used as a protection device for an input of RF IC's, the gate and the source are connected to the ground, and the drain is connected to the input node to form the ggNMOS. Therefore, for AC simulations, the gate, source, and substrate were connected together to serve as a cathode, while the drain node alone served as an anode. The DC voltages for the anode and the cathode were assumed to be zero, and the AC voltage source was applied between the anode and the cathode. An additional series lumped resistor R_{Lumped} of 100 kΩμm was connected between the substrate node, shown in Fig. 2, and the cathode to consider the resistance of the substrate region, which was not included in Fig. 2. Practically, the value of R_{Lumped} can be reduced by increasing the number of substrate p^+ ground contacts. Notice that, as the value of R_{Lumped} increases, the ESD protection characteristics of the ggNMOS device improves since triggering of the parasitic bipolar transistor is getting easier [6].

When the ggNMOS device is used as a protection device, it is expected that the large n^+-drain/p-sub junction capacitance is the main parasitic capacitance. However, from the fact that there also exists the gate/drain overlap capacitance in parallel, the AC equivalent circuit can be expressed as shown in Fig. 3. In Fig. 3, C_{JD} and R_{SUB} are the drain/sub junction capacitance and the distributed substrate resistance including R_{Lumped}, respectively, and C_{GD} and R_G are the gate/drain overlap capacitance and the distributed gate resistance, respectively. Resistance R_P in Fig. 3 represents the additional resistance in parallel across the anode and the cathode, the origin of which should be mainly the leakage current through the drain/substrate pn junction. If the leakage is negligibly small, the value of R_P becomes too large to be considered. The AC model in Fig. 3 includes virtually all the physical parameters present in the device and is different from the one in [7], which is simpler. Here we note that the values of all the physical parameters in Fig. 3 should be frequency-independent if the model is correct.

The AC device simulation results in ATLAS are given as conductance G and capacitance C by assuming a parallel RC equivalent circuit. However, as shown in Fig. 3, the equivalent circuit of the ggNMOS protection device is different. With the improper equivalent circuit assumed in the simulator, the simulated G and C values denoted as the circles and the triangles in Fig. 4, respectively, appear to vary with frequency. We note that the G and C values in Fig. 4 are for 1μm of the device width.

By transforming the equivalent circuit in Fig. 3 to a parallel R circuit, we derived the corresponding frequency-dependent G and C expressions using the parameters in Fig. 3. To fit the modeled values of G and C to the simulated ones, we set C_{JD}= 3.27 fF/μm, R_{SUB}= 100 kΩμm, C_{GD}= 0.06 fF/μm, R_G= 1 kΩμm, and R_P= 6.95×10^8 Ωμm, and numerically calculated the G and C values from their frequency-dependent expressions. We plotted them in Fig. 4 as solid lines. As can be seen in Fig. 4, the fitting is quite excellent and verifies the adequacy of the modeling with the equivalent circuit in Fig. 3 for the given frequency range.

We also examine the possibility of representing the equivalent circuit in a simpler form. In Fig. 4, the dotted lines represent the modeled G and C values assuming a simple series RC equivalent circuit with R = 100 kΩμm and C = 3.33 fF/μm. As can be seen in Fig. 4, it is difficult to get a good fitting for a wide frequency range with this simplified model. Through

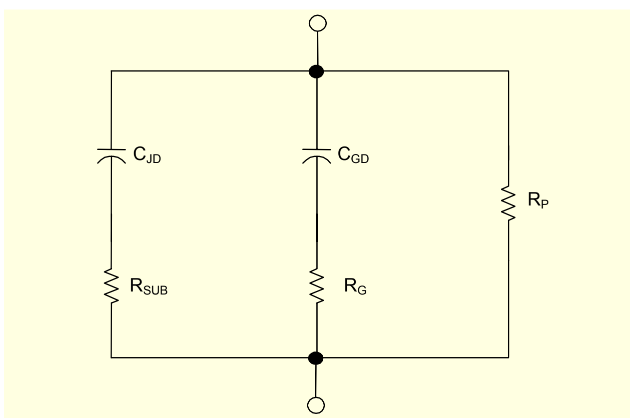

Fig. 3. An AC equivalent circuit of the NMOS protection transistor.

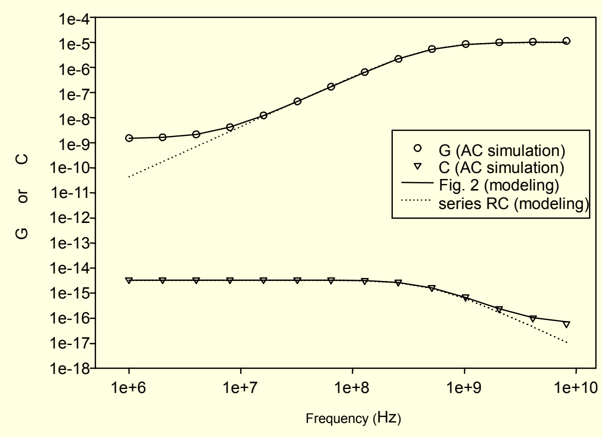

Fig. 4. Small-signal G and C values of the ggNMOS protection device in Fig. 2. R_{Lumped} = 100 kΩμm.

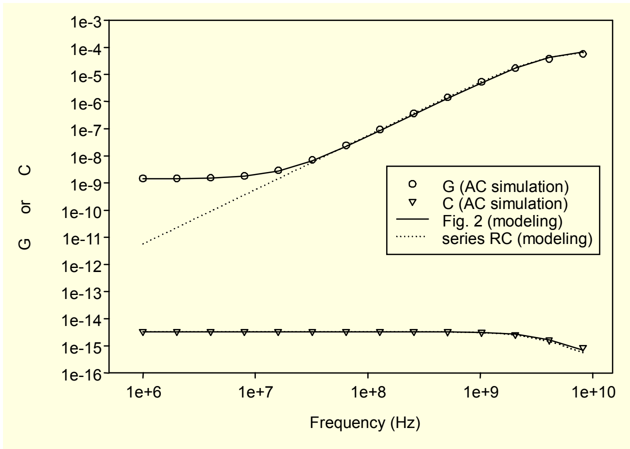

Fig. 5. Small-signal G and C values of the ggNMOS protection device in Fig. 2. R_{Lumped} = 10 kΩμm.

additional examinations, we confirmed that considerations of R_P and C_{GD} are necessary for good fitting in the lower and higher frequency ranges, respectively.

Figure 5 shows a similar graph as Fig. 4, with a smaller lumped resistor R_{Lumped} of 10 kΩμm connected in series to the substrate node. This work was intended to examine a case with reduced substrate resistance by increasing the number of substrate contacts, for example. The circles and triangles represent G and C values from the AC device simulation results, and the solid lines represent the modeled G and C with C_{JD}= 3.27 fF/μm, R_{SUB}= 12 kΩμm, C_{GD}= 0.06 fF/μm, R_G= 1 kΩμm, and R_P= 6.95×10^8 Ωμm. Notice that only the value of R_{SUB} is reduced compared to the case in Fig. 4. In Fig. 5 again, the fitting between the AC device simulation and the modeling is quite excellent. In Fig. 5, the dotted lines again represent the modeled G and C values assuming a simple series RC model with R = 13 kΩμm and C = 3.33 fF/μm. Through additional examinations, we confirmed again that considerations of R_P and C_{GD} are necessary for good fitting in the lower and higher frequency ranges, respectively.

Here we check that the assumed R_{SUB} value of 100 kΩμm and 12 kΩμm are practical ones. The extracted substrate resistances from the measurements were 1.044 kΩ for an NMOS device with L = 0.8 μm and W = 100 μm [12], and 90 Ω for an NMOS device with L = 0.35 μm and W = 160 μm [13], which correspond to R_{SUB}= 104 kΩ and R_{SUB}= 14.4 kΩ for a 1 μm device width, respectively. We assumed that the parasitic resistance of the NMOS protection device is inversely proportional to the device width W. Certainly, the assumed R_{SUB} values are approximately within a practical range.

From the results presented up to now, we can conclude that it can be inadequate to express the AC equivalent circuit of the ggNMOS protection device by a single capacitor as in [1], [8], and [9].

III. Effects of the Parasitics on LNA Characteristics

In this section, we introduce an LNA for narrow-band impedance matching in a 2.4 GHz range, and examine the LNA characteristics by simulations based on the Bsim3v3 model parameters for a standard 0.25 μm CMOS process. The effects of connecting the ggNMOS protection device at the input node or at the output node are examined.

Figure 6 shows an LNA circuit incorporating inductive source degeneration. It has a conventional structure used for narrow-band impedance matching, and all the components considered in the simulations are shown in the figure. For input and output isolation, a cascode topology was chosen. Inductor L_S is used to generate a real component for 50 Ω impedance matching as shown in (1), which is an expression of the input impedance looking into the gate of M_1 in Fig. 6, and L_G is the inductor to cancel out the capacitive reactance for impedance matching [14]. In (1), C_{gs} and ω_T are the gate-source capacitance and the cutoff frequency of M_1, respectively. The two inductors were assumed to be implemented by bond wires. Capacitor C_B is an off-chip capacitor for DC blocking. In this topology, while obtaining the impedance matching by adjusting the L_S and L_G values, we can get noise matching simultaneously by adjusting the device size of M_1 and the current through it [14].

$$Z_{in} = sL_S + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_S \approx sL_S + \frac{1}{sC_{gs}} + \omega_T L_S, \qquad (1)$$

In the output portion of the circuit in Fig. 6, L_T and C_T were intended to achieve resonance while R_T secures circuit stability. The series capacitor C_S and bond wire inductor L_B are included for output impedance matching. Current-mirror biasing was chosen as shown in the figure. The model parameters from a

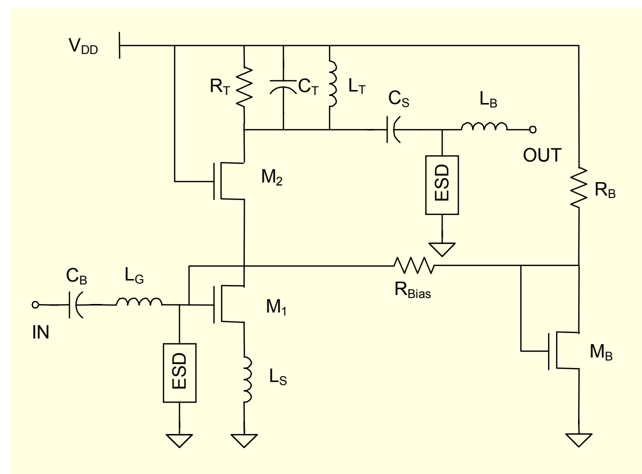

Fig. 6. An LNA circuit for narrow impedance matching.

0.25 μm standard CMOS process were used for the transistors in the circuit, and the capacitors and inductors were assumed as ideal components without considering the parasitics. The power supply voltage V_{DD} was assumed to be 2.5 V.

Figure 6 indicates that ESD devices can be connected at the input and output pads. The ESD devices are connected right next to the bond wire inductors L_G and L_B. We present the simulation results with a ggNMOS ESD protection device connected at the input pad first. Table 2 summarizes and compares the simulation results. In Table 2, Case (1) is for a circuit without the ESD protection device. Case (2) and Case (3) are for circuits with the multi-finger-type 400 μm width NMOS protection device in Fig. 2 connected at the input. For Case (2), the equivalent circuit in Fig. 3 was used for the simulation with C_{JD} = 1.308 pF, R_{SUB} = 250 Ω, C_{GD} = 24 fF, R_G = 2.5 Ω, and R_P = 1.74 MΩ, which were calculated considering width W from the parameter values obtained in the case of R_{Lumped} = 100 kΩμm in section II. We assumed that the parasitic capacitance and resistance of the NMOS protection device are proportional to device width W and 1/W, respectively. For Case (3), the simple series RC equivalent circuit was used for the simulation with C = 1.332 pF and R = 250 Ω, which were calculated similarly considering W. Here we note that the principal parameters in Table 1 for the ggNMOS device in Fig. 2 can be different from those for the device which would be formed in the assumed 0.25 μm standard CMOS process. However we believe that this does not critically affect the results in this work focusing on the trends of the characteristic changes of the circuit.

For each case, the L_S and L_G values were adjusted somewhat to get proper impedance matching. The bias current value for Case (2) in Table 2 is somewhat smaller since the bias condition changes somewhat due to the parallel resistor R_P in the equivalent circuit of the NMOS protection device.

Table 2. Comparison of LNA simulation results: W = 400 μm, R_{Lumped} =100 kΩμm.

Parameters	Case (1) No ESD device	Case (2) Model in Fig. 3	Case (3) Series RC model
I_{BIAS}	5.85 mA	5.75 mA	5.85 mA
S_{11}	-47.3 dB	-54.1 dB	-31.6 dB
S_{22}	-18.6 dB	-16.8 dB	-16.8 dB
S_{21}	19.2 dB	16.8 dB	16.8 dB
S_{12}	-41.5 dB	-44.3 dB	-44.3 dB
NF	0.55 dB	2.37 dB	2.37 dB
NF_{min}	0.52 dB	1.76 dB	1.76 dB
Input P_{1dB}	-14.4 dBm	-11.9 dBm	-11.9 dBm
Output P_{1dB}	3.8 dBm	3.9 dBm	3.9 dBm

In Table 2, the noise characteristics of the LNA without any ESD device are quite excellent and seem to be well optimized since the noise figure (NF) value is quite low and very close to NF_{min}, which is the lowest NF value attainable in this design.

Table 2 shows that, when connecting the large ggNMOS protection device at the input node, there is no difficulty in getting proper impedance matching, but S_{21} representing the power gain reduces, and the NF value representing the noise characteristics degrades a great deal. The reduction in power gain seems to be caused by the power loss to ground through the parasitics of the ESD device. The degradation of the noise characteristics seems to occur since a parallel path possessing the resistive component is added to the input node. We note that the larger the value of the series resistor and/or the smaller the value of the parallel resistor in the signal path, the severer the degradation of noise characteristics [15]. Due to the reduction of power gain, the input P_{1dB} seems to improve to some extent; however, the output P_{1dB} remains unchanged. This indicates that the effect on the linearity is negligible in this circuit.

For Case (3) in Table 2, we gave no change to the matching elements compared to Case (2). The overall characteristics of each are almost identical. It seems that using the simple series RC equivalent circuit is good enough for designing this LNA. The reason for this can be explained by the fact that, as shown in Fig. 4, the characteristics of the series RC equivalent circuit are almost the same with those of the equivalent circuit in Fig. 3 at 2.4 GHz of assumed frequency, even though the difference can be significant at lower and higher frequency ranges. However, the significance of using the simple series RC equivalent circuit in analyzing LNA characteristics should be emphasized since the input pad is connected to an LNA in most RF circuits. Considering the characteristic discrepancies between the complete model and the simple series RC model in Fig. 4, we can say that using the simple series RC equivalent circuit may cause some errors when designing circuits in higher frequency ranges and also when designing circuits performing frequency transformation, for example, mixers. This has not been demonstrated in this work, however.

We also performed circuit simulations for the LNA with a single C model by setting R = 0 in the simple RC equivalent circuit of the NMOS protection device. When the device width was 400 μm, it was impossible to get impedance matching in an acceptable level in this matching topology. When the device width was 200 μm, it was possible to get impedance matching in the level of S_{11}=-5.3 dB at best, which is still not sufficient. S_{21} was 15.3 dB, NF was 0.88 dB, and NF_{min} was 0.58 dB, which compare well with the results of S_{21} = 18.0 dB, NF = 1.77 dB, and NF_{min}=1.31dB for the same circuit with the complete model in Table 3. This implies that the effects of the

parasitics in the ggNMOS protection device can appear exaggerated for the impedance matching aspect, and the noise contribution of the parasitic resistances cannot be counted if the NMOS protection device is modeled by a single capacitor, as in prior publications [1], [8], and [9].

In Table 3, we compare the LNA characteristics with the ggNMOS device connected at the input but with varying device width W. We also show the LNA characteristics with the ggNMOS device connected at the output. The equivalent model in Fig. 3 was used for the simulations. For a W = 200 μm device, we set C_{JD} = 0.654 pF, R_{SUB} = 500 Ω, C_{GD} = 12 fF, R_G = 5 Ω, and R_P = 3.48 MΩ, considering W.

In Table 3, it is noticeable that degradation of the noise characteristics are significant even with the W = 200 μm device connected at the input. When connecting the ggNMOS protection device at the output node, the power gain reduces somewhat due to the power loss to ground through the parasitics of the ESD device, and the linearity degrades somewhat due to linearity degradation of the output portion of the circuit. However, even though the parasitics are added to the output, there is only a negligible increase in the noise figure since there is no power gain along the path between the noise source and the output node.

In Table 4, we compare the LNA characteristics with the W = 400 μm NMOS device connected at the input or output with varying substrate resistances of the device, which can be practically realized by changing the number of the substrate contacts, for example. For the case of R_{Lumped} = 100 kΩμm, R_{SUB} was 250 Ω again. For the case of R_{Lumped} = 10 kΩμm, we simply reduced the R_{SUB} value to 30 Ω, which was calculated considering the device width from the result in section II.

Consider the case when the protection device is connected at the input first. From the data in Table 4, we can see that as the substrate resistance is reduced, it becomes more difficult to get proper impedance matching, and the power gain reduces further due to the increase of power loss to ground. The noise characteristics also degrade further, which is easily expected from the related discussion in this section. We note again that the smaller the value of the parallel resistor in the signal path, the severer the degradation of noise characteristics [15].

We did more simulations with varying the R_{SUB} value and found out some interesting characteristics. As the substrate resistance decreases from 250 Ω, the noise figure increases, peaks at 4.08 dB when the R_{SUB} value is around 40 Ω, and then decreases. This behavior can be explained as follows. As the substrate resistance decreases, the noise figure degrades since the value of the parallel resistor in the signal path decreases. However, as the substrate resistance decreases further, the signal path starts to become unable to see the substrate resistor if the 3 dB frequency corresponding to the RC time constant of the series RC is getting well above the operating frequency. Therefore, the 2.4 GHz component of the noise generated from the substrate resistor starts to become decoupled from the signal path. Certainly this behavior becomes more prevalent as the R_{SUB} value decreases further, and therefore the noise figure decreases further. This behavior explains why we obtained the decent noise figure of 0.88 dB for the device width of 200 μm with R_{SUB} = 0 Ω in the previously mentioned discussions. For the same reason explained earlier, the power gain decreases first and then increases as the R_{SUB} value decreases. Here, we note that practically the substrate resistance cannot be reduced below a certain point [12], [13].

When the protection device is connected at the output, as the substrate resistance is reduced, the power gain reduces further due to the increase of power loss to ground. However, the noise characteristics remain almost unchanged due to the reason

Table 3. Comparison of LNA simulation results with varying device widths. R_{Lumped} =100 kΩμm.

Parameters	No ESD device	400 μm at input	200 μm at input	400 μm at output
I_{BIAS}	5.85 mA	5.75 mA	5.80 mA	5.85 mA
S_{11}	-47.3 dB	-54.1 dB	-44.3 dB	-34.3 dB
S_{22}	-18.6 dB	-16.8 dB	-17.4 dB	-17.1 dB
S_{21}	19.2 dB	16.8 dB	18.0 dB	18.4 dB
S_{12}	-41.5 dB	-44.3 dB	-43.1 dB	-42.3 dB
NF	0.55 dB	2.37 dB	1.77 dB	0.56 dB
NF_{min}	0.52 dB	1.76 dB	1.31 dB	0.53 dB
Input P_{1dB}	-14.4 dBm	-11.9 dBm	-13.2 dBm	-15.9 dBm
Output P_{1dB}	3.8 dBm	3.9 dBm	3.8 dBm	1.5 dBm

Table 4. Comparison of LNA simulation results with varying substrate resistance values: W = 400 μm.

Parameters	No ESD device	R_{SUB}=250Ω NMOS at input	R_{SUB}=30Ω NMOS at input	R_{SUB}=250Ω NMOS at output	R_{SUB}=30Ω NMOS at output
I_{BIAS}	5.85 mA	5.75 mA	5.75 mA	5.85 mA	5.85 mA
S_{11}	-47.3 dB	-54.1 dB	-8.5 dB	-34.3 dB	-31.6 dB
S_{22}	-18.6 dB	-16.8 dB	-15.2 dB	-17.1 dB	-27.2 dB
S_{21}	19.2 dB	16.8 dB	5.8 dB	18.4 dB	16.5 dB
S_{12}	-41.5 dB	-44.3 dB	-46.0 dB	-42.3 dB	-44.2 dB
NF	0.55 dB	2.37 dB	3.93 dB	0.56 dB	0.59 dB
NF_{min}	0.52 dB	1.76 dB	3.19 dB	0.53 dB	0.56 dB
Input P_{1dB}	-14.4 dBm	-11.9 dBm	0.2 dBm	-15.9 dBm	-13.9 dBm
Output P_{1dB}	3.8 dBm	3.9 dBm	5.7 dBm	1.5 dBm	1.6 dBm

explained previously.

In the simulations up to now, we used the equivalent circuits assuming 0 V for DC voltage between the anode and the cathode. However, the applied DC voltage can change depending on the type of circuits and the location of the protection device in them. Actually, the DC voltages at the input node and output node in our LNA circuit were about 0.7 and 0 V, respectively. In the case of the input, the drain/substrate junction of the NMOS protection device becomes reverse biased by 0.7 V, and therefore the value of C_{JD} in Fig. 3 should be decreased somewhat for this case. To make the analysis simpler we neglected this effect, which does not seem to affect the analysis in this work seriously, and can be easily solved by setting the initial bias conditions for AC device simulations to the proper values.

IV. Summary

From the AC analysis results utilizing a 2-dimensional device simulator, the AC equivalent circuit of the ggNMOS ESD protection device was extracted. The extracted equivalent circuit was utilized to analyze the effects of the parasitics in the ggNMOS protection device on the characteristics of an LNA.

We showed that the effects of the parasitics can appear exaggerated for the impedance matching aspect, and the noise contribution of the parasitic resistances cannot be counted if the ggNMOS protection device is modeled by a single capacitor as in prior publications.

We also showed that the AC equivalent circuit of the ggNMOS protection device can be simplified to a simple series RC circuit in analyzing the effects of the protection device on the LNA characteristics for the assumed frequency range.

We confirmed that the major changes in the characteristics of the LNA when connecting the ggNMOS protection device at the input are reduction of the power gain and degradation of the noise performance. We also showed that the performance degradation worsens as the substrate resistance is reduced. This behavior could not be detected if the single capacitor model is used.

References

[1] P. Leroux and M. Steyaert, "High-Performance 5.2GHz LNA with On-Chip Inductor to Provide ESD Protection," *Electronics Lett.*, vol. 37, Mar. 2001, pp. 467-469.

[2] M.-D. Ker, T.-Y, Chen, C.-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin with Very Low Input Capacitance for High-Frequency or Current-Mode Applications," *IEEE J. Solid-state Circuits*, vol. 36, Aug. 2000, pp. 1104-1199.

[3] B. Kleveland, T.J. Maloney, I. Morgan, L. Madden, T.H. Lee, and S.S. Wong, "Distributed ESD Protection fro High-Speed Integrated Circuits," *IEEE Electron Devices Lett.*, vol. 21, Aug. 2000, pp. 390-392.

[4] H. Feng, K. Gong, and A.Z. Wang, "A Comparison Study of ESD Protection fro RF IC's: Performance vs. Parasitics," *IEEE MTT-S Digest*, 2000, pp. 143-146.

[5] S. Hyvonen, S. Joshi, and E. Rosenbaum, "Cancellation Technique to Provide ESD Protection for Multi-GHz RF Inputs," *Electronic Lett.*, vol. 39, issue 3, Feb. 2003, pp. 284-286.

[6] J.-Y, Choi, W.S, Yang, D. Kim, and Y. Kim, "Thyristor Input-Protection Device Suitable for CMOS RF IC's," *Analog Integrated Circuits and Signal Processing*, vol. 43, no. 1, Apr. 2005, pp. 5-14.

[7] J. Li, S. Joshi, and E. Rosenbaum, "A Verilog-A Compact Model for ESD Protection NMOSTs," *Proc. of the 2003 Custom Integrated Circuits Conf.*, Sept. 2003, pp. 253-256.

[8] V. Chandrasekhar and K. Mayaram, "Analysis of CMOS RF LNAs with ESD Protection," *Proc. of the 2002 IEEE Int'l Symp. on Circuits and Systems*, vol. 4, May 2002, pp. IV-799 - IV-802.

[9] S. Sridharan, G. Nayak, and P.R. Mukund, "LNA Design Optimization with Reference to ESD Protection Circuitry," *Proc. of the 2003 IEEE Int'l Symp. on Circuits and Systems*, vol. 1, May 2003, pp. I-203 - I-208.

[10] S. Aur, A. Chatterjee, and T. Polgreen, "Hot-Carrier Reliability and ESD Latent Damage," *IEEE Trans. Electron Devices*, vol. 35, Dec. 1988, pp. 2189-2193.

[11] ATLAS Ⅱ Framework, Version 5.0.0.R, Silvaco International, 1999.

[12] S. Lee, C.S. Kim, and H.K. Yu, "A Small-Signal RF Model and Its Parameter Extraction for Substrate Effects in RF MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, July 2001, pp. 1374-1379.

[13] J.-J. Ou, X. Jin, I. Ma, C. Hu, and P.R. Gray, "CMOS RF Modeling for GHz Communication IC's," 1998 Symp. of VLSI Technology, *Digest of Technical Papers*, June 1998, pp. 94-95.

[14] T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, New York: Cambridge University Press, 1998.

[15] B. Razavi, Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2000.

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