Voltage-Mode 1.5 Gbps Interface Circuits for Chip-to-Chip Communication

Kwang-Jin Lee, Tae-Hyoung Kim, Uk-Rae Cho, Hyun-Geun Byun, and Suki Kim

In this paper, interface circuits that are suitable for point-to-point interconnection with an over 1 Gbps data rate per pin are proposed. To achieve a successful data transfer rate of multi-gigabits per-second between two chips with a point-to-point interconnection, the input receiver uses an on-chip parallel terminator of the pass gate style, while the output driver uses the pullup and pulldown transistors of the diode-connected style. In addition, the novel dynamic voltage level converter (DVLC) has solved such problems as the access time increase and valid data window reduction. These schemes were adopted on a 64 Mb DDR SRAM with a 1.5 Gbps data rate per pin and fabricated using a 0.10 μm dual gate oxide CMOS technology.

Keywords: Signaling, chip-to-chip communication, interface schemes.

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I. Introduction

As process technologies and design techniques advance, the operation frequency of microprocessors is reaching a multi-gigahertz level. Therefore, memories such as main memory and cache memory should be required to have a much higher data transfer rate [1]-[4]. However, interface standards such as stub series transceiver logic and Rambus signal level inevitably confront the bandwidth limit of data transfers because they use a bus-type interconnection. To break through the problems, interface standards such as high-speed transceiver logic, which is a point-to-point type connection, have been adopted because they can cover a 2 to 3 Gbps data transfer rate per pin owing to their much lighter loading. However, as data transfer rates have increased over multi-gigahertz, the input capacitance of the receiving stage, the slew rate of transfer signals, and signal integrity have been fatal bottlenecks in cases of point-to-point connections [4].

In this paper, signaling schemes that are suitable to point-to-point interconnection with a multi-gigahertz data rate are presented. The schemes were adopted for 64 Mb DDR SRAMs with a 1.5 Gbps data rate per pin, which are fabricated using a 0.10 μm dual-gate oxide CMOS technology.

II. Circuit Design

Until now, most point-to-point interconnection schemes have used voltage mode signaling because of the backward compatibility for conventional interface standards such as low-voltage CMOS and low-voltage TTL. Therefore, the proposed interface schemes in this paper are focused on voltage mode signaling.

1. On-Chip Input Termination

As the data transfer rate between two integrated circuit (IC) chips has increased, the input capacitance of the receiving stage and the slew rate of transfer signals have become fatal bottlenecks. These bottlenecks can be improved by using input parallel terminations [7]. Recently, as the data width increases, on-chip termination is becoming increasingly preferred. Figure 1 shows various types of input stages.

The results of SPICE simulations on the different input termination types are shown in Fig. 2, where the simulation conditions are T_{cycle} = 1 GHz, C_{load} = 4 pF, Z_{drive} = 40 Ω, and Z_0 = 50 Ω. In this figure, we confirm that the on-chip input termination type has the best signal integrity.

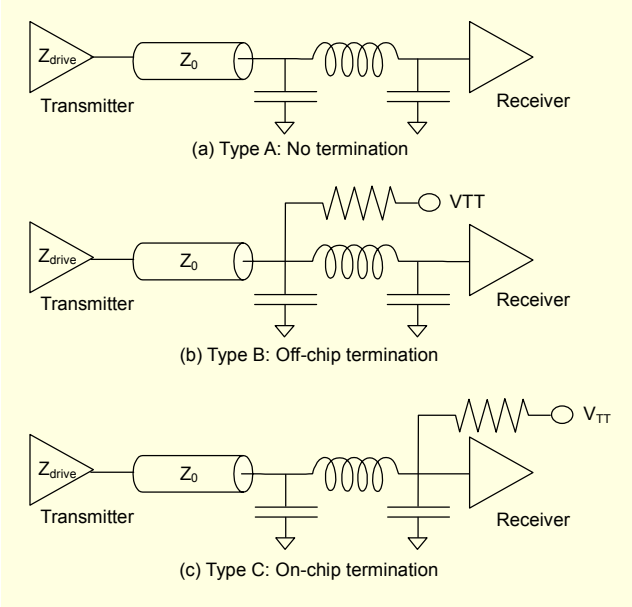

Fig. 1. Input termination types.

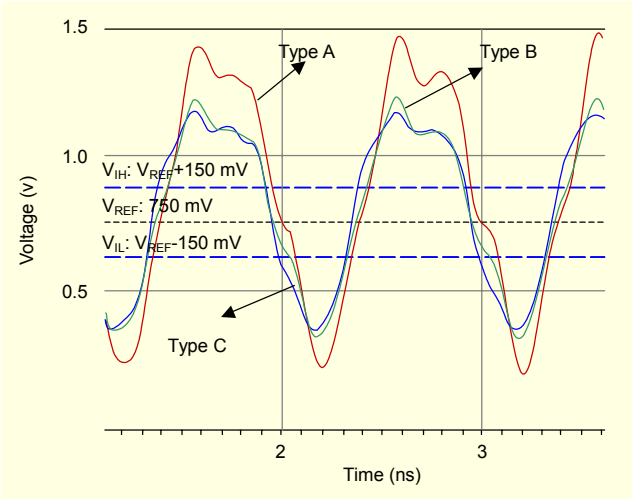

Fig. 2. Waveforms of input termination types.

The on-chip input parallel termination types are classified into three types depending on the manner of implementing them, as shown in Fig. 3. Type A is an ideal resistor case, type B is a simple one-transistor style, and type C is a CMOS pass gate style. Though type A is superior in terms of linearity, fixed resistors cannot compensate the process, voltage, and temperature (PVT) variations of resistance. In the case of type B, it is possible to adjust the impedance control for PVT variations. However, it has a large linearity error. To improve the linearity problem of type B, type C is adopted.

Figure 4 shows the I-V characteristic curves of the on-chip input parallel terminators in Fig. 3. The resistance of type C is almost similar to the ideal resistor, where the simulation conditions are interface voltage (V_{DDQ}) = 1.8 V, temperature = 80 °C, and R_{th} = 80 Ω.

Therefore, type C is suitable for the on–chip input terminator to improve signal integrity. The on-chip input terminator acts as an output driver at read operations and as an input terminator at non-read operations to minimize the increase of input capacitance at the input terminators.

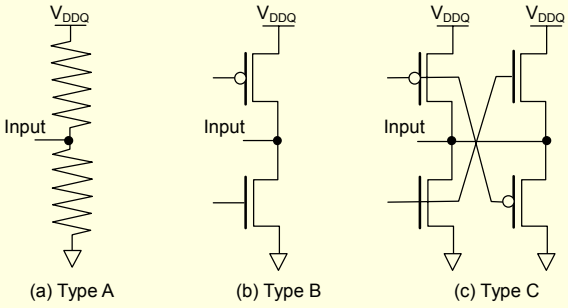

Fig. 3. On-chip input parallel termination types.

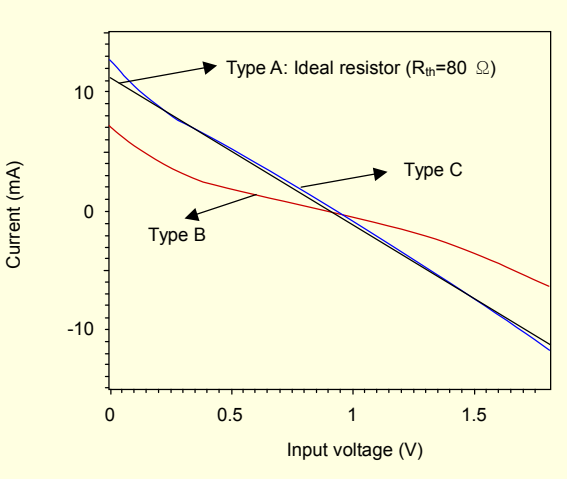

Fig. 4. I-V characteristics curves of on-chip input parallel terminators.

2. Off-Chip Driver

The interface voltage (V_{DDQ}) has been isolated from the internal core voltage (V_{DD}) in most high-speed IC chips to minimize undesirable influences such as switching noise, signal reflections, power supply ripples, and ground bouncing. While the interface voltage is maintained at the same voltage level, the internal core voltage has been lowered because the design rule of the fabrication process has been scaled down to meet the needs of high-speed, low-power, and high-density chips. However, the ohmic region of the transistor has decreased as the operation voltage (V_{DD}) has been lowered, as shown in Fig. 5. This means that the linearity of the off-chip driver (OCD) has been very poor.

Therefore, the poor linearity of the conventional OCD shown in Fig. 6(a) will cause a reflection of the transmitted signal.

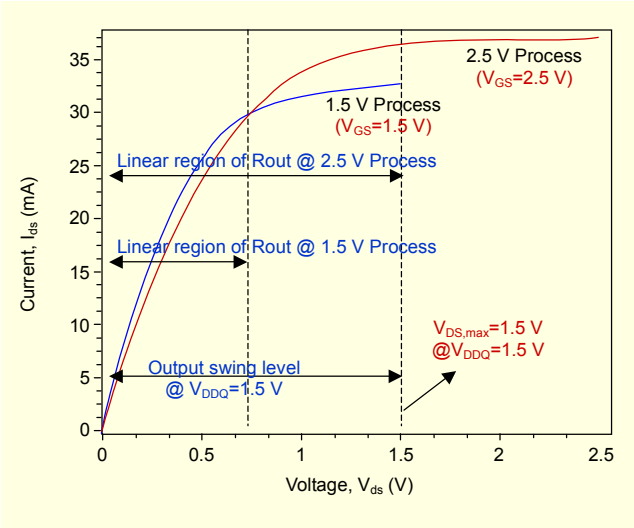

Fig. 5. Characteristic curves of V_{ds} vs. I_{ds} according to the process with different operation voltage levels.

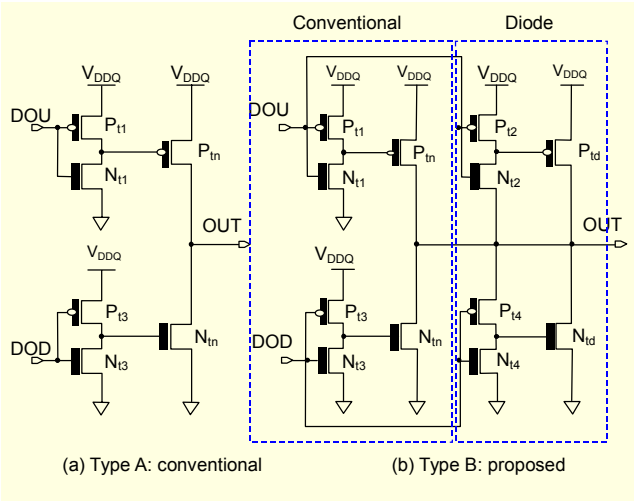

Fig. 6. Off-chip driver types.

To solve the problem, the pullup and pulldown transistors of the diode-connected style as a part of the output driver shown in Fig. 6(b) are added. This proposed type uses both an NMOS diode for pulldown and a PMOS diode for pullup, whereas the previous types with a diode connection use only one between the pullup and pulldown; these types are usually used to control the slew-rate of the output signal [8], [9].

The I-V characteristic DC curves in Fig. 7 show that the linearity of the diode-connected type is much better than that of the one-transistor type [5], [6]. The diode-connected transistors form another current path which provides or drains current depending upon the pad voltage and makes the I-V characteristics of the output driver linear.

To remove or reduce the effect of the reflected waves, the impedance of an OCD should be retained as constant over a wide-pad voltage range. This is because the voltage level of the output driver becomes different depending upon the termination type and the driven signals. Therefore, because of the effect of linearity, the reflection at the OCD stage is expected to be greatly decreased in the case of the diode-connected style. The increase of output capacitance by using a diode is not large since output capacitance is mainly determined by the pad and printed circuit board of the package.

Figure 8 shows which of the OCD types has better signal integrity. The simulation is performed during a mismatch condition to compare the conventional type with the proposed type in terms of signal integrity, with simulation conditions of T_{cycle} = 1 GHz, Z_{load} = open, Z_{out} = 50 Ω, Z_0 = 60 Ω. The waveforms of Fig. 8(b) show that type B, the diode-connected style, has better signal integrity.

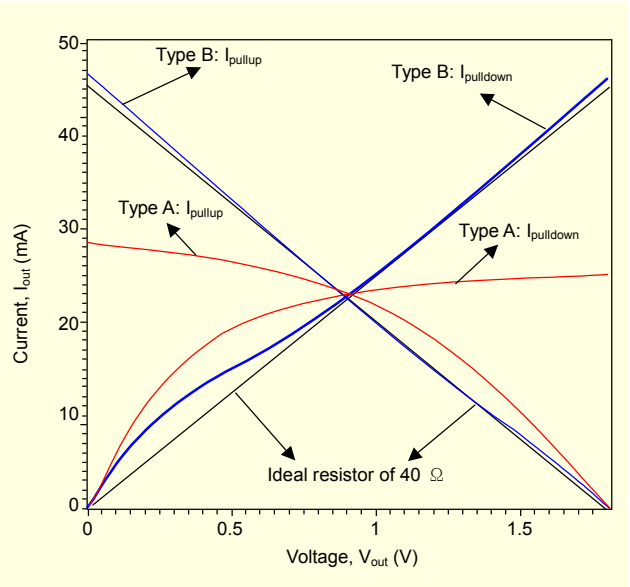

Fig. 7. I-V characteristic curves of OCD types.

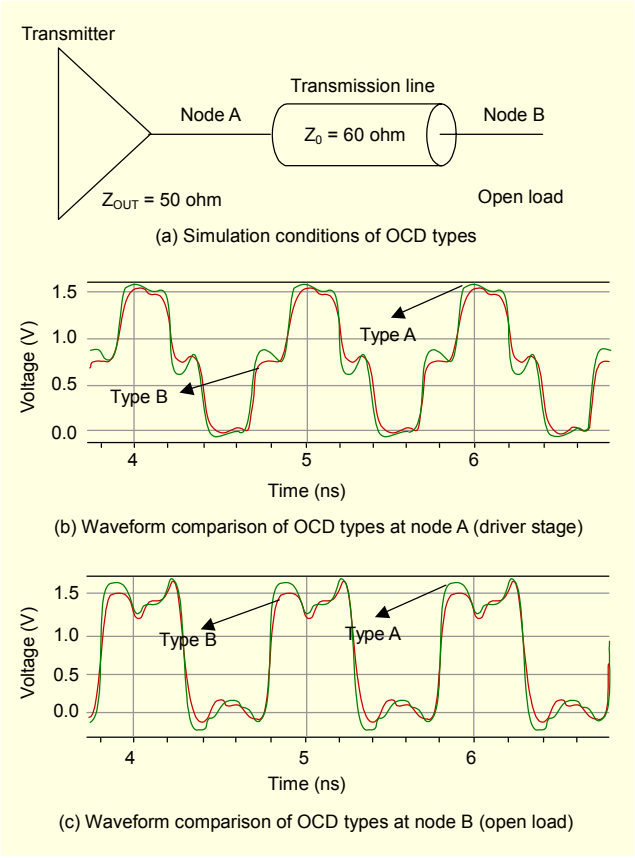

Fig. 8. Signal integrity according to OCD types.

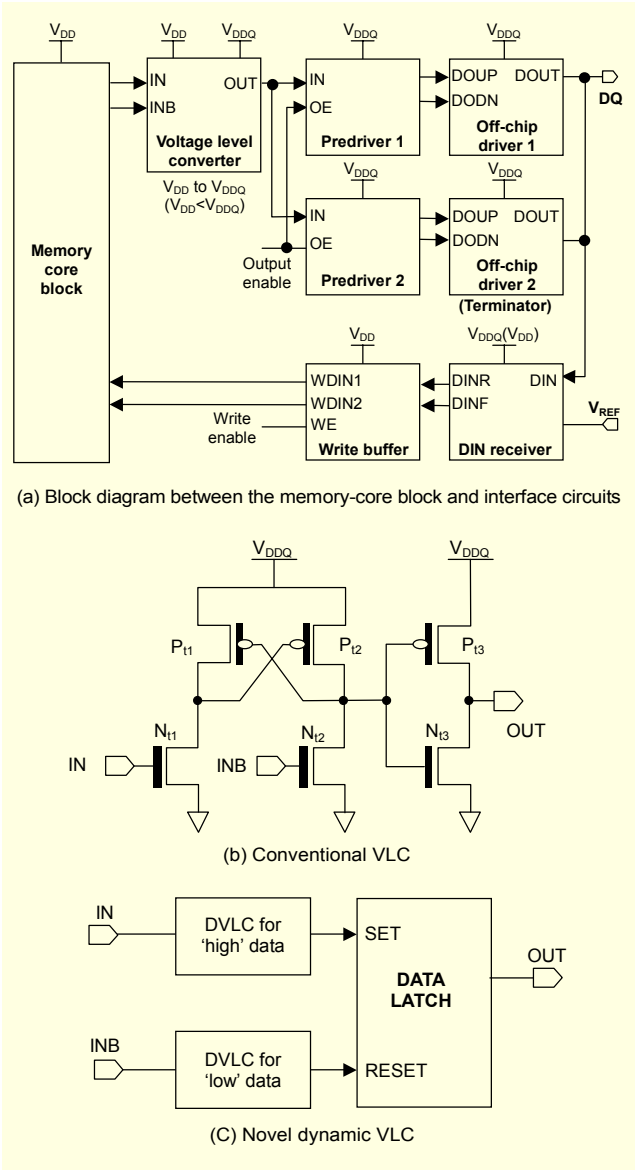

Fig. 9. Voltage level converter circuits.

3. Dynamic Voltage Level Converter

As process technology has advanced, the V_{DD} level has become lower than the V_{DDQ} level. Therefore, a voltage level converter (VLC) circuit should be used to transmit the internal operation signals to an OCD circuit as shown in Fig. 9(a), which is a block diagram of a simplified data path within a memory.

The VLC circuit converts the voltage level (V_{DD}) of the internal signals into the V_{DDQ} level to prevent a short circuit of the currents and to swing the reduction of the output signals. Figure 9(b) shows the conventional VLC circuit [6]. It consists of a differential amplifier with loads of cross-coupled PMOS transistors and an inverter. The duty cycle of a level-converted signal of the VLC is distorted since the transition time of 'GND' to 'V_{DDQ}' is larger than that of 'V_{DDQ}' to 'GND' at an output node of the differential amplifier. Also, the conventional VLC has a relatively large delay due to both the short path from V_{DDQ} to GND during transitions of stored levels and the large threshold voltage of the transistors with a thick gate oxide. This causes problems such as an access time increase and valid data window reduction.

The novel dynamic voltage level converter (DVLC) in Fig. 9(c) has solved the problems of the conventional VLC. It is composed of a set path, a reset path, and a latch. The set path generates an enable short pulse in the case when an 'IN' signal goes from GND to V_{DD}, and the reset path generates an enable pulse in the case when an 'INB' signal goes from GND to V_{DD}.

Both the set and reset paths are implemented by dynamic logic which is suitable for high-speed ICs as shown in Fig. 10(a). The dynamic logic has over-sized transistors about the enable path and under-sized transistors about the disable path, which minimizes propagation delay. Also, the activation timing of the enable and disable paths are different, which alleviates a short circuit in the current of the V_{DDQ} to GND path. As a result, the dynamic logic is faster than conventional static gates. In addition, the DVLC can maintain an almost 50% duty cycle

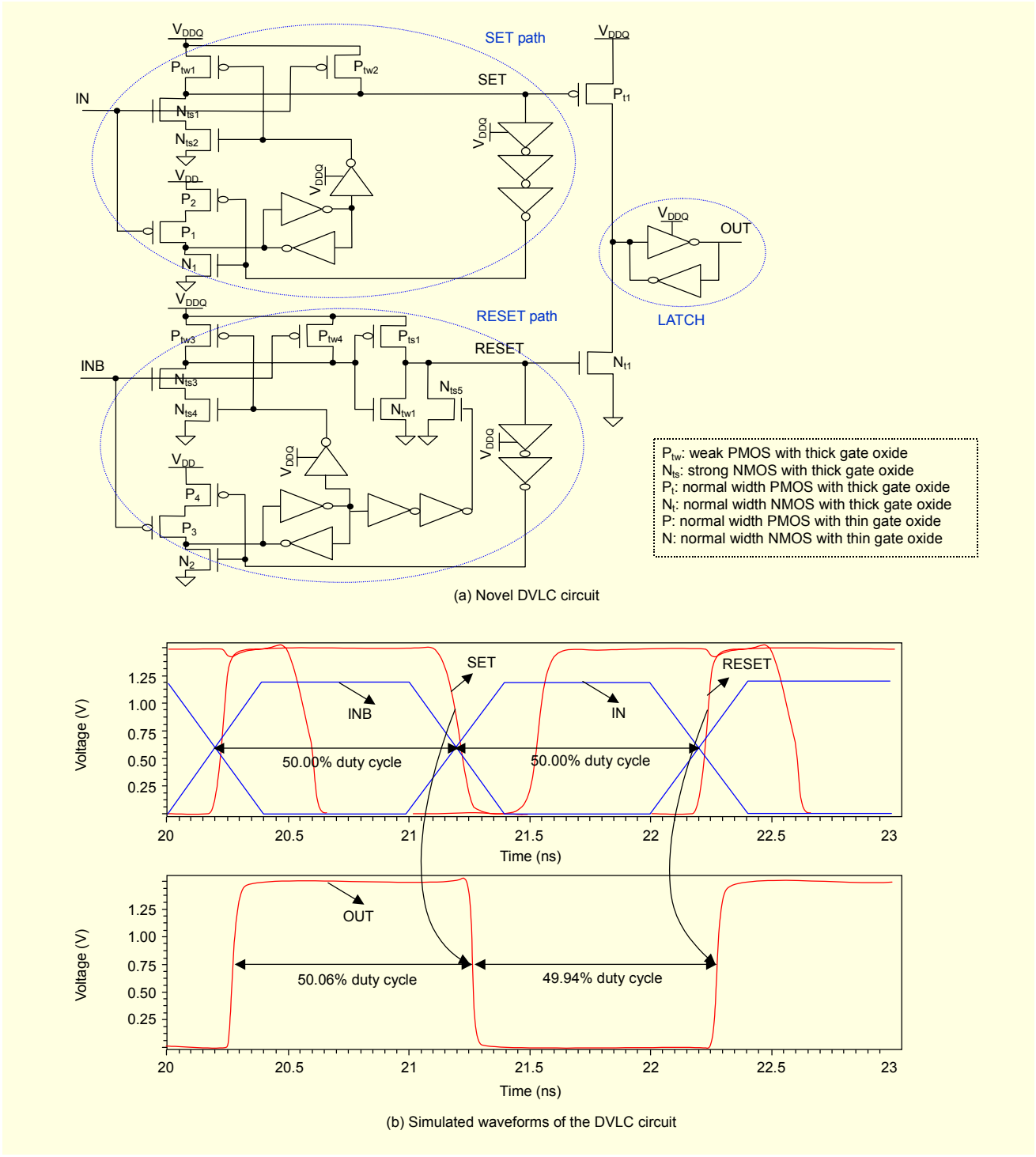

Fig. 10. The novel DVLC.

for the voltage-level-converted signal since it has set and reset paths with equal propagation delays, as shown in Fig. 10(a). Figure 10(b) shows simulated waveforms of the DVLC circuit. If the 'IN' signal goes from GND to V_{DDQ}, a 'SET' pulse signal is activated and the 'SET' pulse signal makes an 'OUT' signal in the GND level. If the 'INB' signal goes from GND to V_{DDQ}, a 'RESET' pulse signal is activated, and the 'RESET' pulse signal makes an 'OUT' signal V_{DDQ} level. As a result, an 'OUT' signal with an almost 50% duty cycle of the V_{DDQ} level is generated.

Figure 11 shows the duty cycle distortion of a DVLC with various V_{DDQ} values. In a conventional VLC, as the difference

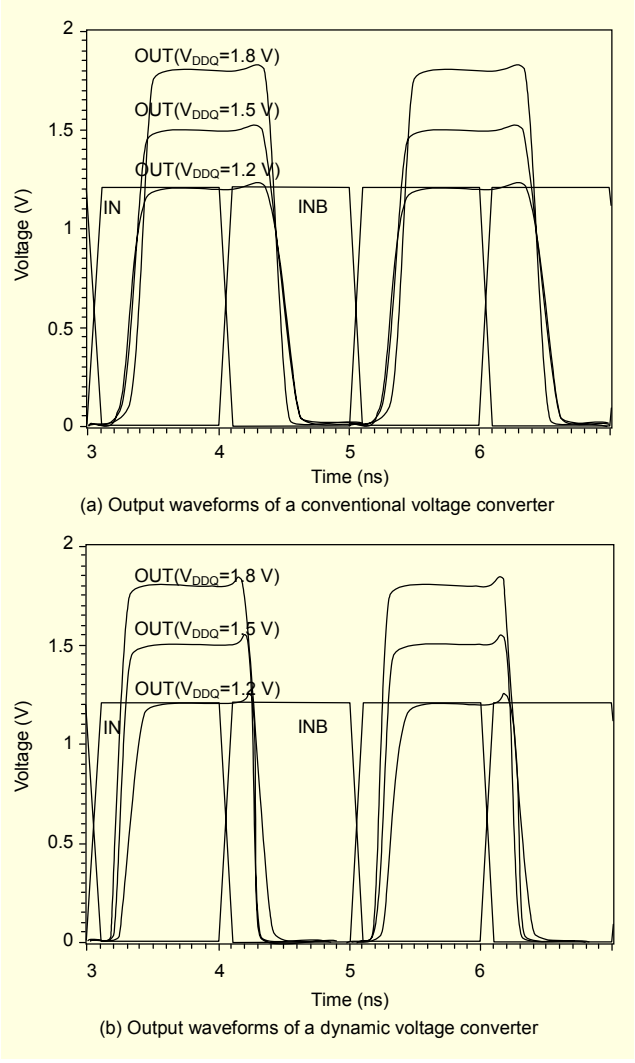

Fig. 11. Duty cycle distortion of VLC.

Table 1. Comparison of voltage level converters, with simulation conditions of load cap = 0.4 pF and temp = 80°C.

	VDD	VDDQ	Delay	Power	Duty cycle
Conventional VLC	1.2 V	1.2 V	290 ps	272 μW	59.11 %
	1.2 V	1.5 V	**330 ps**	491 μW	**55.04 %**
	1.2 V	1.8 V	380 ps	1040 μW	52.57 %
Novel DVLC	1.2 V	1.2 V	260 ps	328 μW	50.11 %
	1.2 V	1.5 V	**200 ps**	630 μW	**50.06 %**
	1.2 V	1.8 V	170 ps	982 μW	49.96 %

between input and V_{DDQ} increases, the duty cycle distortion also increases. However, the proposed DVLC has a nearly constant duty cycle.

Table 1 summarizes the simulation results of the VLC types using a SPICE parameter of a 0.10 μm dual-oxide CMOS technology. As V_{DDQ} increases, the delay time of a conventional VLC increases due to the larger contention by the short path from V_{DDQ} to GND during transitions of stored levels, whereas the delay time of the DVLC decreases owing to both the improvement of the current drive ability of the transistors and no short path between V_{DDQ} and GND. Also, the duty cycles of DLVC maintain a level of almost 50% at any operational condition. In other words, the novel DVLC has a better time delay and duty cycle than the conventional VLC at any V_{DD} and V_{DDQ} conditions as shown in Table 1. This means that the DVLC is adequate for high-speed devices with a multi-Gigahertz data rate per pin.

4. Eye Diagram

The valid eye window of transferred data can be maximized through proposed interface schemes such as the on-chip parallel terminator, output driver with the diode-connected style, and dynamic voltage level converter.

Figure 12 shows an eye diagram of output data with a data rate of 1.5 Gbps and a power supply of 1.5 V. The valid data window is about 525 ps at 750 mV±150 mV when the driver and terminator impedances are 25 and 50 ohm. The duty cycle of the eye window is about 50%.

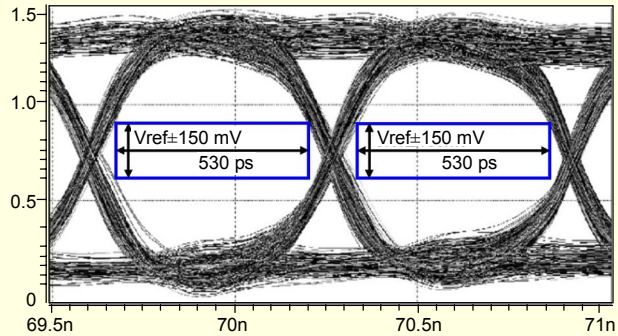

Fig. 12. Simulation results of the eye window.

III. Hardware Results

The proposed signaling schemes of this paper were adopted in 64 Mb DDR SRAMs. Figure 13 shows the layout of an IO buffer module of a 64 Mb DDR SRAM with a 1.5 Gbps data rate per pin which includes the interface schemes. The layout area of the module is about 360 μm × 360 μm.

Figure 14 shows a chip micrograph of the 64 Mb DDR SRAM with a 1.5 Gbps data rate per pin. The chip size is about 18.8 mm × 8.01 mm, which includes the IO buffer modules.

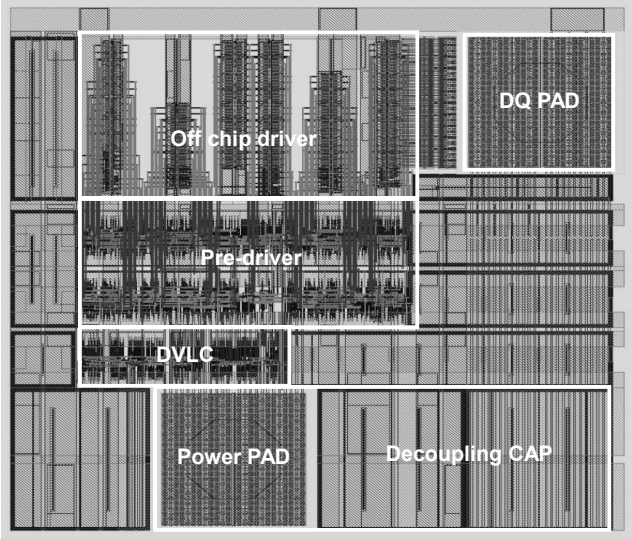

Fig. 13. Layout of an IO buffer module.

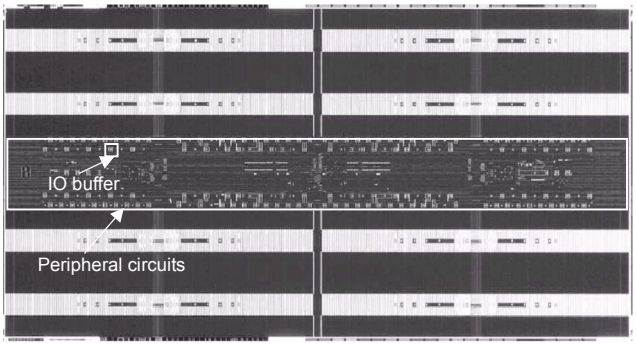

Fig. 14. Chip micrograph of a 64 Mb DDR SRAM.

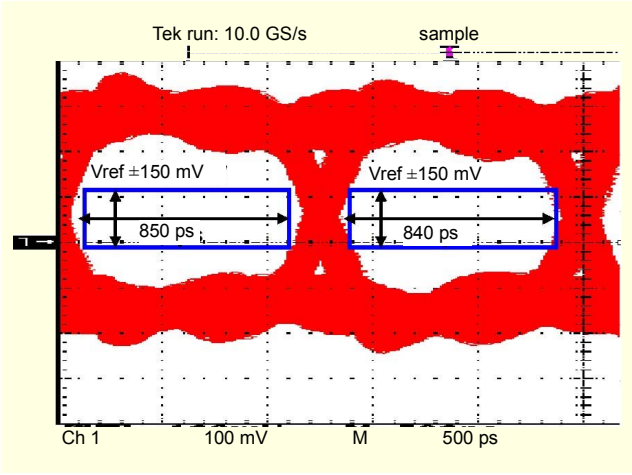

Fig. 15. A measured eye pattern in a 64 Mb DDR SRAM.

The SRAM chip is fabricated using a 0.10 μm dual gate oxide CMOS technology.

Figure 15 shows a test waveform of the output data of the implemented 64 Mb DDR SRAM with a 1.0 Gbps data rate per pin. The main noise source in the test result of the eye window comes from power noise of the memory test equipment, where power is supplied through large inductive lines. The valid data window is about 840 ps at 750 mV±150 mV, which verifies that the memory interface schemes of this paper for point-to-point inter-connection with a multi-gigahertz data rate guarantee good signal integrity. The duty cycle distortion of the designed IO is only 10 ps which is about 1.2%.

IV. Conclusion

This paper proposes the signaling schemes for chip-to-chip communication with a multi-gigabits per-second data rate per pin. To achieve a successful data transfer of multi-gigabits per-second between two chips with a point-to-point interconnection, the input receiver uses an on-chip parallel terminator of the pass gate style, and the output driver uses the pullup and pulldown transistors of the diode-connected style. In addition, a dynamic voltage level converter, which has a smaller delay and lower duty-cycle distortion than the conventional VLC, is also used. These schemes were adopted for 64 Mb DDR SRAMs with a 1.5 Gbps data rate per pin. The SRAM is fabricated using a 0.10 μm dual gate oxide CMOS technology.

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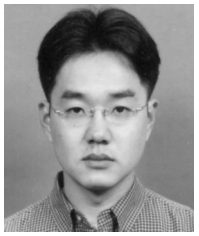
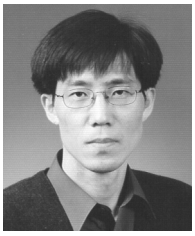


Tae-Hyoung Kim was born in Cheongju, Korea, in 1973. He received the BS and MS degrees in the School of Electrical Engineering from Korea University, in 1999 and 2001. In 2001, he joined the Digital Solution Network Division, Samsung Electronics Company, Hwa-sung, Korea. Since 2001, he has been working on the design of high-speed SRAM memories. His research interests are in analog circuits and high-speed I/O interface.



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