A Comparative Study of a Dielectric-Defined Process on AlGaAs/InGaAs/GaAs PHEMTs

Jong-Won Lim, Ho-Kyun Ahn, Hong-Gu Ji, Woo-Jin Chang,
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We report on the fabrication of an AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistor (PHEMT) using a dielectric-defined process. This process was utilized to fabricate 0.12 μm × 100 μm T-gate PHEMTs. A two-step etch process was performed to define the gate footprint in the SiN_x. The SiN_x was etched either by dry etching alone or using a combination of wet and dry etching. The gate recessing was done in three steps: a wet etching for removal of the damaged surface layer, a dry etching for the narrow recess, and wet etching. A structure for the top of the T-gate consisting of a wide head part and a narrow lower layer part has been employed, taking advantage of the large cross-sectional area of the gate and its mechanically stable structure. From s-parameter data of up to 50 GHz, an extrapolated cut-off frequency of as high as 104 GHz was obtained. When comparing sample C (combination of wet and dry etching for the SiN_x) with sample A (dry etching for the SiN_x), we observed an 62.5% increase of the cut-off frequency. This is believed to be due to considerable decreases of the gate-source and gate-drain capacitances. This improvement in RF performance can be understood in terms of the decrease in parasitic capacitances, which is due to the use of the dielectric and the gate recess etching method.

Keywords: GaAs, PHEMT, gate, recess, cut-off frequency, maximum oscillation frequency.

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I. Introduction

With the recent development of wireless LAN systems and satellite communications, one of the main objectives of modern microelectronics is the fabrication of devices with an increasing cutoff frequency. The improvement of the frequency performance of the devices must achieve not only the highest possible values of f_T and f_{max}, but also the lowest possible noise levels. A state-of-the-art high-frequency and low-noise performance are achieved by unipolar devices, mainly high electron mobility transistors (HEMTs). These devices provide better performances than metal-semiconductor field effect transistors, which in the past were the most popular high-frequency and low-noise devices [1]-[3]. One way of improving the HEMT performance is to use InGaAs as the two-dimensional electron gas channel material instead of GaAs. The benefits of using a thin InGaAs layer as the pseudomorphic channel in an HEMT include the enhanced electron transport in InGaAs as compared to GaAs.

Pseudomorphic high electron mobility transistors (PHEMTs) are promising devices for millimeter-wave and optical communications systems due to their excellent high frequency and low-noise performance. The PHEMTs are capable of operating well into the millimeter wave frequency range with excellent power and efficiency. The GaAs-based PHEMT has stimulated great interest for high-speed and high-frequency, low-noise, power application, and phase control devices [4]. In order to further improve the performance of the devices, their gate length must be reduced down to the technological limit [5]. Simultaneously, a small gate resistance must be realized. However, shorter gates involve an increase of short channel effects that limit the microwave performance of the HEMTs.

In order to reduce the gate resistance, T-shaped gates with large cross-sectional areas are required [6]-[8]. Their fabrication can be either based on electron beam lithography (EBL) with multiple resist layers [9] or on optical stepper lithography combined with sidewall spacers. The shape of the T-gate, the gate footprint length L_g, and the thickness of the passivation all have a major impact on the gate capacitance C_{gs}, which is a key parameter for the RF performance of the device. The wider head of the T-gate decreases the gate resistance R_g, but at the same time the gate capacitance increases. Therefore the width of the T-gate head must be chosen as a trade-off value between low resistance and low capacitance [10].

In this study, we demonstrate a plasma-enhanced chemical vapor deposited SiN_x-defined process. It will be shown that 0.12 μm gate-length AlGaAs/InGaAs/GaAs PHEMTs fabricated using this process exhibit good DC and microwave characteristics. We report the results on using the different dielectric etching technique to obtain T-gates with 0.12 μm gate lengths. Additionally, we shall prove that based on this process a mechanically stable T-gate can be formed. To achieve a low gate resistance and a low parasitic capacitance for the bottom of the T-gate, the dielectric etch and gate recess processes have been modified to include two separate steps.

II. Experimental Details

The PHEMT epitaxial structure was grown by molecular beam epitaxy on a semi-insulating GaAs substrate and consists of the following layers: 5000 Å GaAs buffer, 30 periods of the AlGaAs/GaAs superlattice buffer, an undoped $Al_{0.23}Ga_{0.77}As$ buffer, silicon planar doping (1×10^{12} cm^{-2}), a 20 Å $Al_{0.23}Ga_{0.77}As$ spacer, a 120 Å $In_{0.2}Ga_{0.8}As$ channel, a 35 Å $Al_{0.23}Ga_{0.77}As$ spacer, silicon planar doping (4.5×10^{12} cm^{-2}), and a 250 Å $Al_{0.23}Ga_{0.77}As$ Schottky contact layer. Finally, a 400 Å thick undoped GaAs cap layer was grown to protect the active layer from the oxidation causing the creation of defects [11]. The sheet carrier density of two-dimensional electron gas and the electron mobility measured at room temperature were 3.4×10^{12} cm^{-2} and 5750 $cm^2/V{\cdot}s$, respectively.

The mesa was defined by conventional photolithography. The AlGaAs/InGaAs/GaAs was etched down to the buffer layer using a nonselective etchant, $H_3PO_4 : H_2O_2 : H_2O = 4 : 1 : 50$. The ohmic contact patterns were defined using a lift-off technique. A AuGe/Ni/Au metal system was used for the source and drain since it is widely used as an ohmic contact to GaAs materials. Prior to the contact deposition, the GaAs wafers were cleaned by dipping into an $HCl : H_2O$ solution; they were then rinsed in deionized water and blown dry with nitrogen. They were loaded into a thermal evaporation system, and the vacuum system was pumped to $5{\times}10^{-7}$ Torr before contact deposition. Then, the AuGe/Ni/Au ohmic contact structure was deposited on the undoped GaAs cap layer. The AuGe/Ni/Au layer thicknesses were 1000, 300 and 1200 Å. These ohmic contacts were heat-treated by rapid thermal annealing in a nitrogen atmosphere. The ohmic contact alloying was performed by two-step annealing, first at 340℃ and then at 380℃, for 20 s each. The heat treating of the ohmic alloy at 340℃ is a step for the metallurgical stability of the grain structure. The contacts were then examined electrically using transmission line model measurements. The specific contact resistivity ρ_c was $1.1 \times 10^{-6}\ \Omega{\cdot}cm^2$.

To investigate the influence of parasitic capacitances, three samples were processed. The steps of the fabrication of T-gates using a dielectric-defined layer are outlined schematically in Fig. 1. A 400 Å silicon nitride layer was deposited by plasma-enhanced chemical vapor deposition at 260℃ to protect the device and to support the gate. The gate footprint patterning was done by electron beam lithography using a Leica EBPG 5000 plus system operating at an acceleration voltage of 100 kV.

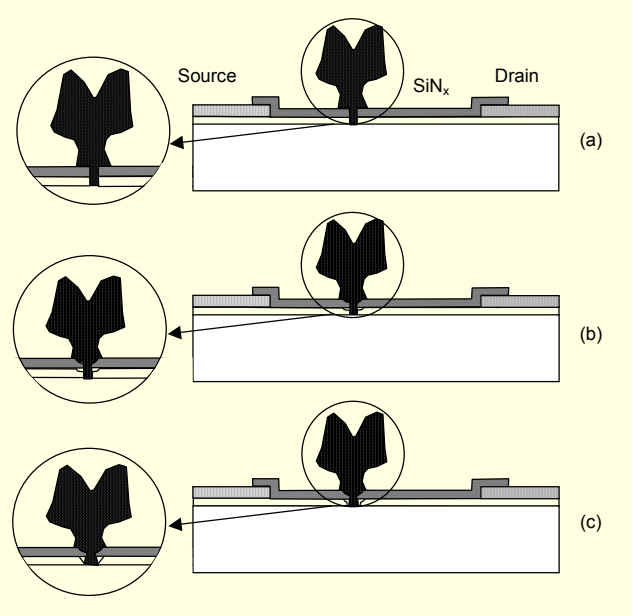

Fig. 1. Cross-sectional schematic view of the dielectric-defined process for a 0.12 μm planar-doped PHEMTs: (a) sample A: SiN_x was etched by RIE alone, (b) sample B: SiN_x was etched by using a combination of 40% wet etching and RIE, and (c) sample C: SiN_x was etched by using a combination of 60% wet etching and RIE.

A 2500 Å thick layer of polymethylmethacrylate (PMMA) resist was used and developed using a mixed solution of MIBK (metylisobutylketone) and IPA (isopropylalcohol).

After development of the resist, the SiN_x was etched by RIE alone (sample A), using a combination of 40% wet etching and RIE (sample B), and by a combination of 60% wet etching and

RIE (sample C). For sample A, the SiN_x layer was etched using CF_4 plasma alone to create a 0.12 μm gate footprint. For sample B, the two-step etch process consisted of a combination of 40% wet and dry etching, and the 0.12 μm gate footprint was also created. For sample C, the two-step etch process consisted of a combination of 60% wet and dry etching. The wet chemical etches SiN_x isotropically, resulting in a lateral undercut, whereas the anisotropic RIE maintains the SiN_x opening dimension in the resist. First, a buffered oxide etch solution was used to widen the top of the SiN_x layer defined by the photoresist. The target was to remove about 40 to 60% of the SiN_x thickness to give enough lateral undercut. The buffered oxide etch was diluted to slow down the etch rate in order to have a better etch depth control. The residual SiN_x was etched off anisotropically by RIE in CF_4 plasma. The top of the T-gate was defined by using electron beam exposure of a tri-layer resist: PMMA (2500 Å)/co-polymer /PMMA (1400 Å). The top of the T-gate structure, which consists of a wide head part and a narrow lower layer (0.3 μm), has been employed taking advantage of its large cross-section area of the gate and mechanically stable structure. After the development of the tri-layer resist, the gate recess was etched. To achieve high uniformity and reproducible gate recess processing, the GaAs cap layer was selectively etched by electron cyclotron resonance (ECR) dry etching. The GaAs cap layer was selectively etched using a BCl_3/SF_6 gas mixture. Etch uniformity was less than 4% across a 4-inch wafer. The gate recessing of sample A was performed using an ECR etching process, and that of sample B was carried out in two steps including a wet etching for the removal of the RIE damaged surface layer and a dry etching for the narrow recess. A H_3PO_4 : H_2O_2 : H_2O (4 : 1 : 180) solution was used to etch off approximately 20% of the GaAs cap layer. After the wet etching, the sample was then loaded into an ECR chamber for further etching in a BCl_3/SF_6 gas. The gate recessing of sample C was carried out in three steps including a wet etching for the removal of the damaged surface layer, a dry etching for the narrow recess, and a wet etching. The gate recess is stopped when a predetermined source-drain current is reached. After the gate recess, Ti/Pt/Au layers (6000 Å) were deposited and lifted-off. Figure 2 shows an SEM image of the cross-section of a fabricated T-gate taken from an actual device.

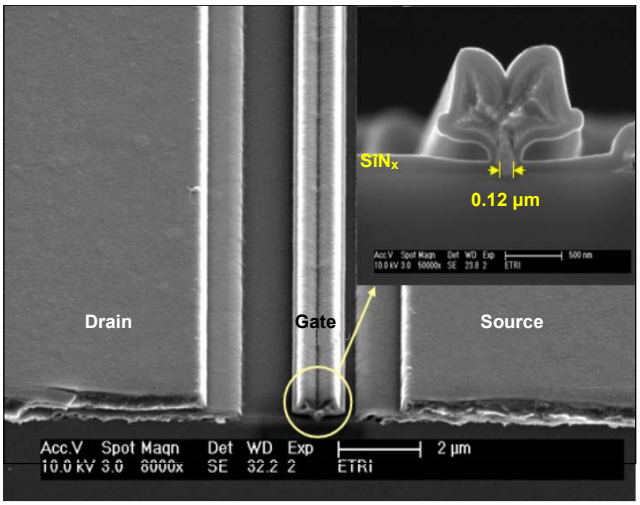

Fig. 2. SEM photograph of the cross section of a recessed T-gate PHEMT.

III. Results and Discussion

PHEMTs with source-to-drain spacings of 2.5 μm, source-to-gate spacings of 0.79 μm, gate-to-drain spacings of 1.59 μm, unit gate widths of 50 μm and two gate fingers, and gate lengths of 0.12 μm were fabricated using the tri-layer resist on the PHEMT structure described earlier. This asymmetric source and drain structure with shorter gate-to-source separation than gate-to-drain can be applied for reducing the

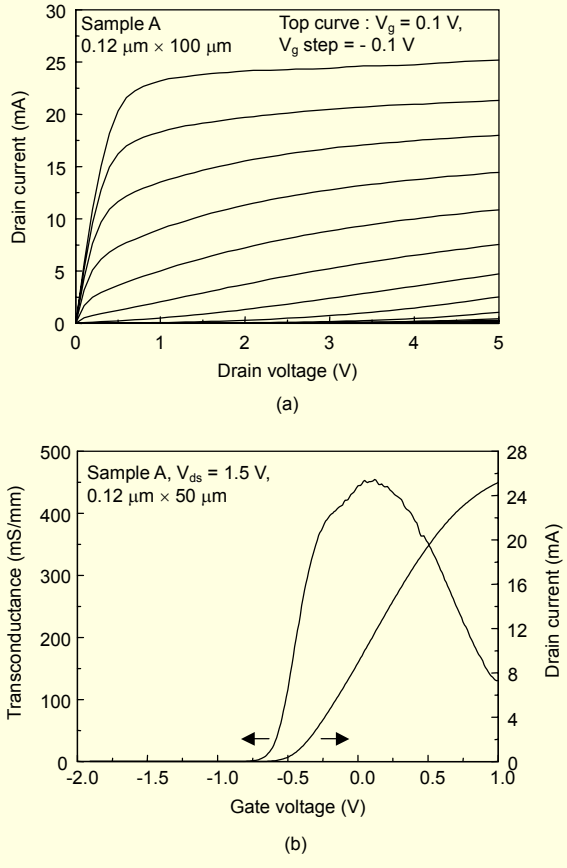

Fig. 3. (a) Drain current as a function of source-to-drain voltage and (b) the extrinsic transconductance and drain current as a function of source-to-gate voltage for the 0.12 μm PHEMT devices fabricated by RIE alone and dry gate recess (sample A).

source resistance. In the tri-layer process, the gate recessing was performed, then the wet etching followed by the dry etching. The gate-length dimensions were verified by examining the cross-sectional profile of the gates in a scanning electron microscope. The DC and RF characteristics were evaluated by measuring the devices in an HP 4156B DC parameter analyzer and an HP 8510C network analyzer, respectively.

Figure 3(a) shows the drain current as a function of source-to-drain voltage V_{ds} for the 0.12 μm PHEMT device fabricated by RIE alone with a dry gate recessing (sample A). The device exhibited good pinch-off characteristics. We obtained a pinch-off voltage of $V_p = -0.61$ V and a drain-source saturation current I_{dss} of 21 mA at $V_{gs} = 0$ V and $V_{ds} = 5$ V. The extrinsic transconductance g_m and drain current I_{ds} as a function of source-to-gate voltage V_{gs} at a drain voltage of 1.5 V were measured and shown in Fig. 3(b). The maximum g_m was measured as 455 mS/mm at $V_{gs} = 0.12$ V.

Figure 4(a) shows the drain current as a function of source-to-drain voltage V_{ds} for the 0.12 μm PHEMT device fabricated by the combination of 40% wet etching and RIE (sample B). The device also exhibited good pinch-off characteristics. We obtained a pinch-off voltage of $V_p = -0.8$ V and a drain-source saturation current I_{dss} of 28 mA at $V_{gs} = 0$ V and $V_{ds} = 5$ V. The extrinsic transconductance g_m and drain current I_{ds} as a function of source-to-gate voltage V_{gs} at a drain voltage of 1.5 V were measured and are shown in Fig. 4(b). The maximum g_m was measured as 435 mS/mm at $V_{gs} = 0.05$ V.

Figure 5(a) shows the drain current as a function of source-to-drain voltage V_{ds} for the 0.12 μm PHEMT device fabricated by the combination of 60% wet etching and RIE (sample C). The device also exhibited good pinch-off characteristics. We obtained a pinch-off voltage of $V_p = -0.66$ V and a drain-source saturation current I_{dss} of 32 mA at $V_{gs} = 0$ V and $V_{ds} = 5$ V.

The extrinsic transconductance and drain current I_{ds} as a function of source-to-gate voltage V_{gs} at a drain voltage of 1.5 V were measured and are shown in Fig. 5(b). The maximum g_m was measured as 610 mS/mm at $V_{gs} = 0.13$ V.

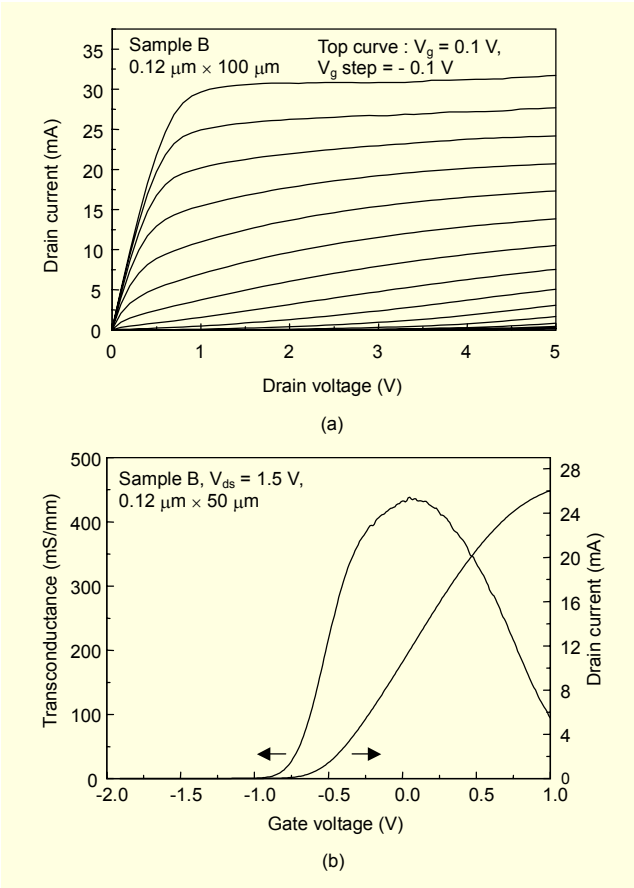

Fig. 4. (a) Drain current as a function of source-to-drain voltage and (b) the extrinsic transconductance and drain current as a function of source-to-gate voltage for the 0.12 μm PHEMT devices fabricated by a combination of 40% wet etching and RIE (sample B).

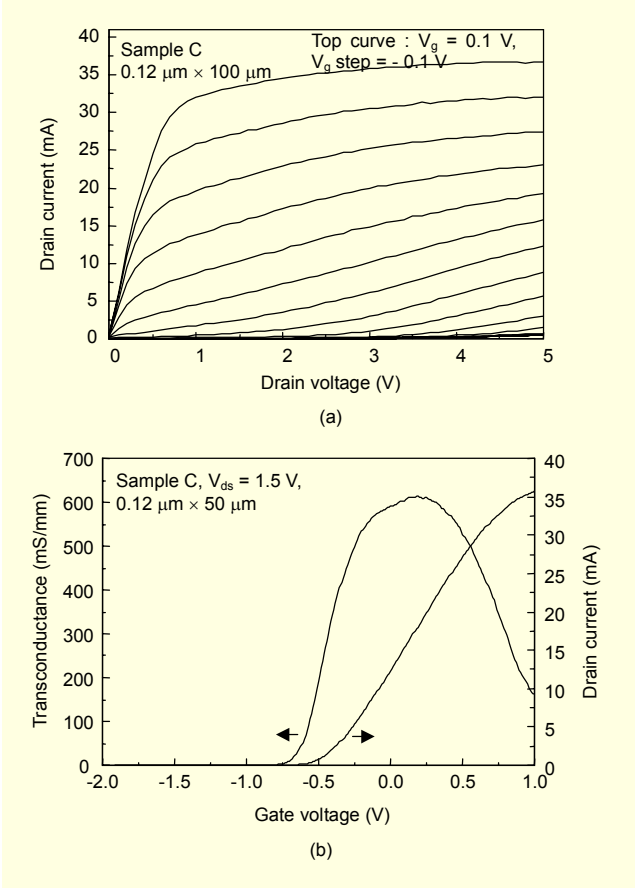

Fig. 5. (a) Drain current as a function of source-to-drain voltage and (b) the extrinsic transconductance and drain current as a function of source-to-gate voltage for the 0.12 μm PHEMT devices fabricated by a combination of 60% wet etching and RIE (sample C).

From Figs. 3 and 4, the low value of extrinsic transconductance for sample B is due to the increase in source resistance as a result of undercutting by the wet etching prior to the dry etching. It can be seen that, relative to sample B, sample A has a 0.19 V positive shift in pinch-off voltage. The dry etching time of sample A is higher than that of sample B using a two-step recess etching. Because the GaAs cap layer was selectively etched using an SF_6 and BCl_3 gas mixture, it is believed that the plasma-induced damage of sample B is less than that of sample A. From the above results, the positive shift is probably due to a negative charge resulting from plasma-induced defects. When the recess depth is increased, the effective distance between the gate and the channel decreases. This results in an increase of the transconductance with recess. The consideration of short channel effects also leads to an expected increase of the transconductance with a recess.

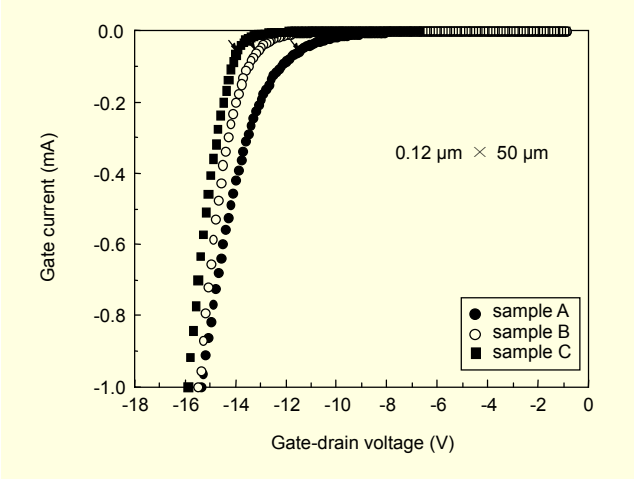

Fig. 6. Gate to drain breakdown characteristics for the samples .

Gate-to-drain breakdown voltage BV_{gd} measurements were made on the samples. The gate-to-drain breakdown voltage curves are shown in Fig. 6. Sample A has a gate-to-drain breakdown of – 11.4 V. Sample B and sample C have a gate-to-drain breakdown of – 13.3 V and – 13.9 V. The breakdown voltage is defined at a drain-to-gate current of 1 mA/mm and is measured by biasing the drain at 0 V and sweeping the gate bias with the source floating. As the side-etching length is increased, BV_{gd} increases due to a reduction of the maximum electric field strength at the drain side [12].

The RF properties of the fabricated PHEMTs were measured by on-wafer probing from 0.5 to 50 GHz using a Cascade microwave probe station and an HP8510C network analyzer. Typical current gain h_{21} and maximum stable and available gains (MSG/MAG) as a function of frequency for sample A are shown in Fig. 7(a). The drain and gate voltages applied in the RF measurements were 1.5 and 0.1 V, respectively. From

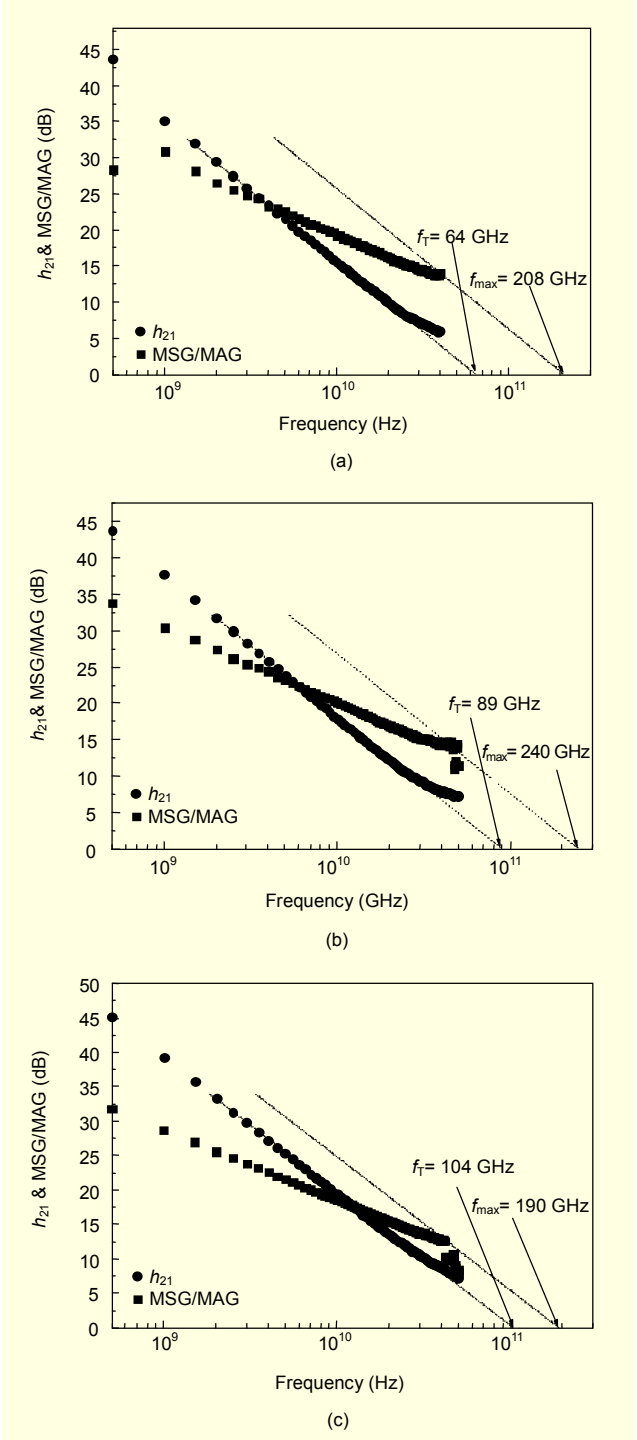

Fig. 7. Measured current gain and maximum available gain as a function of frequency for (a) sample A, (b) sample B and (c) sample C.

the measured S-parameters, the small-signal equivalent circuit was extracted using a direct extraction technique, and the corresponding f_T and f_{max} were estimated. Both f_T and f_{max} were calculated using the h_{21} and MSG/MAG values by an

Table 1. Small signal equivalent circuit parameters at V_{ds} = 1.5 V and V_{gs} = 0.1 V. The parameters were obtained by equivalent circuit analysis.

Device	L_g (μm)	W_g (μm)	No. of fingers	g_m (mS)	C_{gs} (fF)	C_{gd} (fF)	C_{ds} (fF)	R_g (Ω)	R_s (Ω)	R_i (Ω)	R_d (Ω)	τ (ps)
Sample A	0.1	50	2	53	127.5	9.3	44.1	1.3	1.4	3.7	3.5	0.99
Sample B	0.1	50	2	54	95.7	7.6	43.7	0.8	1.9	5.9	7.4	0.73
Sample C	0.1	50	2	69	81.2	7.0	41.3	0.7	5.0	8.0	10.8	0.65

L_g: gate length, W_g: gate width, g_m: transconductance, C_{gs}: gate-source capacitance, C_{gd}: gate-drain capacitance, C_{ds}: drain-source capacitance, τ: transit time, R_g: gate resistance, R_s: source resistance

extrapolation of a –20 dB/decade slope. The current gain cut-off frequency f_T was 64 GHz and the maximum oscillation frequency f_{max} was 208 GHz.

Current gain h_{21} and MSG/MAG as a function of frequency for sample B are shown in Fig. 7(b). The extrapolated cut-off frequency f_T and the maximum oscillation frequency f_{max} were 89 GHz and 240 GHz, respectively. And current gain h_{21} and MSG/MAG as a function of frequency for sample C are shown in Fig. 7(c). The extrapolated cut-off frequency f_T and the maximum oscillation frequency f_{max} were 104 GHz and 190 GHz, respectively.

This result was comparable to the previously reported value for a conventional PHEMT process [13], [14]. In order to investigate the increase of cut-off frequency, the parameters in the small signal equivalent circuit model were extracted at the maximum transconductance bias point and are shown in Table 1. The most prevalent method for obtaining equivalent circuit parameters is fitting by circuit simulation. In Table 1, we see that sample A has the largest R_g and sample C has the smallest. This can be understood by the fact that the wet process in the SiN_x etching ensures better connectivity of the footprint of the T-gate to the top. On the other hand, sample A has the smallest R_s and R_d, whereas sample C has the largest due to the lateral etching in the wet process of the recess etching. The value of C_{ds} is similar for samples A, B and C since this parameter represents the coupling between source and drain that takes place mainly through the carriers in the buffer, which practically are not affected by the inclusion of the T-gate. However, important differences appear in the values of C_{gs} and C_{gd}. Sample C shows a more significant decrease in these values than samples A and B. This effect becomes clearly apparent when the small signal circuit parameters are calculated, revealing that gate-drain and gate-source capacitances are increased due to the capacitive coupling between the head of the gate and the semiconductor. The head of the T-gate provokes a capacitive coupling between gate and semiconductor. This affects considerably the distribution of the electric field inside the device. The main difference appearing when the T-gate geometry is considered is a decrease in the potential in the semiconductor regions under the flanks of the T-gate head due to the influence of the negative gate potential applied to the gate, which is not completely shielded by the presence of the dielectric between the gate head and the semiconductor. This effect takes place mainly in the regions below the part of the recess that is not in contact with the gate electrode. The capacitive coupling between the head of the T-gate and the semiconductor must have some influence on the capacitive elements of the small signal equivalent circuit associated with the gate. In the case of sample A, the values of C_{gs} and C_{gd} are 127.5 and 9.3 fF, respectively. In the case of sample B, the values of C_{gs} and C_{gd} are 95.7 and 7.6 fF, respectively. And, in the case of sample C, the values of C_{gs} and C_{gd} are 81.2 and 7.0 fF, respectively. These results show that parasitic capacitances are essentially localized between the top of the T-gate and the cap layer through the dielectric coating layer. By avoiding the presence of passivation under the T-gate, parasitic capacitances can be reduced and high-frequency parameters can then be improved. A way to reduce the average dielectric constant in the space between the semiconductor surface and the contacts is to decrease the thickness of the dielectric layer, such that this space is partially filled with air [15]. From the above results, the improvement in RF performance can be understood in terms of the decrease in parasitic capacitances due to dielectric and gate recess etching method. This method is promising in solving the problem of decreasing the parasitic capacitance for short gate lengths as well as obtaining a mechanically stable T-gate structure. A dielectric-defined process has been successfully used to fabricate 0.12 μm gate length planar-doped AlGaAs/InGaAs/GaAs PHEMTs. Good DC and microwave performances are achieved by these devices, demonstrating the suitability of the process for fabricating short gate length devices. And this process can be implemented on sub-100 nm devices since the e-beam lithography is separated. Compared to the conventional process, this process protects the active channel area and prevents the device characteristics from drifting over a long time period. Moreover, it is shown that the process offers the possibility of decreasing the resistance and capacitance of short

gate fingers by forming mechanically stable T-gates.

IV. Conclusion

The fabrication of a 0.12 μm T-gate by means of a dielectric-defined process has been described. The gate footprint pattern is transferred into the silicon nitride layer by a two-step etching process which consists of wet etching in a diluted buffered oxide etch followed by RIE in CF_4 plasma. The gate recessing was carried out in three steps including wet etching for removal of the damaged surface layer, dry etching for the narrow recess, and wet etching. We observed the increase of cut-off frequency f_T from 64 to 104 GHz. The improvement in RF performance can be understood in terms of the decrease in parasitic capacitances due to the use of SiN_x and the gate recess etching method. This method is a promising process in terms of decreasing the parasitic capacitance for short gate lengths as well as obtaining a mechanically stable T-gate structure.

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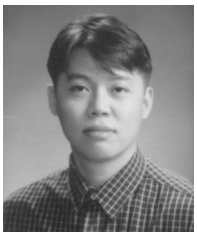

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